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Vacuum nanoelectronics: Back to the future?—Gate insulated nanoscale vacuum channel transistor

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A gate-insulated vacuum channel transistor was fabricated using standard silicon semiconductor processing. Advantages of the vacuum tube and transistor are combined here by nanofabrication. A photoresist ashing technique enabled the nanogap separation of the emitter and the collector, thus allowing operation at less than 10 V. A cut-off frequency f_T of 0.46 THz has been obtained. The nanoscale vacuum tubes can provide high frequency/power output while satisfying the metrics of lightness, cost, lifetime, and stability at harsh conditions, and the operation voltage can be decreased comparable to the modern semiconductor devices. © 2012 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4717751>]

Early electronics centered around the vacuum tube used to amplify, switch, or modulate electrical signals. It has been many decades since the vacuum tubes have been replaced by solid-state devices such as the metal-oxide-semiconductor field-effect transistor (MOSFET) and diode.¹ Nevertheless, the vacuum tubes are still used in niche applications such as premier sound systems and high-power radio base stations.^{2,3} The transition from the vacuum tube to the solid-state device was not driven by the superiority of the semiconductor as a carrier transport medium but by the ease of fabrication, low-cost, low-power consumption, lightness, long lifetime, and ideal form factor for integrated circuits (ICs). The vacuum tubes were fabricated by mechanical machining and used as discrete components, whereas modern solid-state devices are batch processed in assembling the integrated circuits. The vacuum device is more robust than solid-state devices in extreme environments involving high temperature and exposure to various radiations. The critical tradeoff is that the vacuum tubes yield higher frequency/power output but consume more energy than the MOSFET. The vacuum is intrinsically superior to the solid as carrier transport medium since it allows ballistic transport while the carriers suffer from optical and acoustic phonon scattering in semiconductors. The velocity of electrons in vacuum is theoretically 3×10^{10} cm/s, but is limited to about 5×10^7 cm/s in semiconductors. As the cathodes of vacuum tubes need to be heated for thermionic emission of electrons, the energy for heating adversely overwhelms the energy required for field emission. The vacuum device is, therefore, not suitable for low power devices. For high power amplification (e.g., >50 W), however, the solid state device needs a complex circuit architecture including many transistors, microstrips, and thermal management systems.

The advantages of both devices can be achieved together if the macroscale vacuum tube is miniaturized to the nanometer scale. The nano vacuum tubes can provide high frequency/power output while satisfying the metrics of lightness, cost, lifetime, and stability at harsh conditions.

More importantly, further downscaling can allow a cold cathode because the electric field itself is strong enough to emit electrons. Also, an ultimate downscaling in conjunction with low workfunction materials may decrease the turn-on gate and drain voltages to less than 1 V, thus enabling these devices to be competitive with modern semiconductor technology. These benefits can be attained by the use of matured IC technology to fabricate nanoscale vacuum tubes and facilitate circuit integration.

The most common design of vacuum microelectronic is a vertical field emitter consisting of the emitter, gate, and collector as shown in Fig. 1(a). The emitter is a sharp conical tip, the gate is a circular aperture, and the collector is flapped at the top. The movement of electrons between the emitter (cathode) and the collector (anode) is controlled by the gate. An array of vertical field emitters forms a large-area flat electron source.^{4,5} Unfortunately, the vertical structure may be undesirable for circuit implementation due to the difficulties in achieving geometrical dimensions such as gap spacing to be identical over all devices on the substrate. In contrast,

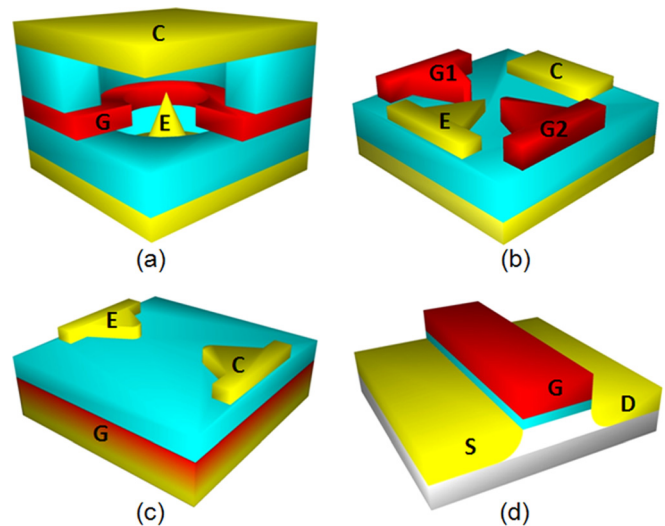


FIG. 1. Structures of vacuum devices and analogues to conventional MOSFET. (a) Vertical field-emitter, (b) planar lateral field-emitter, (c) MOSFET, and (d) gate-insulated air channel transistor.

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the geometry of the planar structure (Fig. 1(b)) is defined by photolithography enabling practical integration.^{6,7} However, as the distance between the emitter and the gate shrinks, processing becomes difficult. In addition, a fraction of the emitted electrons can be easily swept into the gate, as well as the electrons at the gate can be emitted to the collector, both of which are detrimental in circuit design. Herein, we have implemented a gate-insulated planar lateral triode to reduce the gate leakage similar to silicon dioxide in MOSFET preventing the gate leakage current. Figures 1(c) and 1(d) show the structural analogy between the back-gate MOSFET and our nano vacuum channel transistor. The device was fabricated via conventional semiconductor fabrication techniques. The space between the emitter and the collector was defined less than the lithography limit, achieved by photoresist ashing.⁸ As the channel distance becomes less than the mean free path of electrons in air, the vacuum requirement itself is relaxed, and the field emission voltage is reduced to a value smaller than the ionization potential of molecules in air.^{9,10} As such, the present device can be referred to as the vacuum channel transistor even though it operates at atmospheric conditions.

A silicon-on-insulator wafer with a buried oxide (100 nm) and top silicon (120 nm) was the starting material, and the top silicon was thinned to 50 nm by thermal oxidation and removal. The silicon was degenerately doped ($1 \times 10^{20}/\text{cm}^3$) with phosphorous ion implantation, and the ions were activated by rapid thermal annealing at 1000 °C for 10 s. Next, the photoresist lines fanned out at both ends were defined by 193 nm KrF stepper. Figure 2 shows the scanning electron microscopy (SEM) images of the photoresist. An initial line width of 180 nm was subsequently reduced by oxygen plasma treatment until the line was discontinued, forming two separated electrodes. This technique, referred to as resist trimming or thinning, is commonly used for reducing the linewidth, but we have utilized it here to completely discontinue the line pattern. Since plasma ashing reduces the photoresist isotropically, the ashing should be finished before its height is completely consumed, and therefore, the maximum ashing thickness should be less than the height of the resist. While the height of the photoresist was fixed at 400 nm, the width was varied by the layout. In prac-

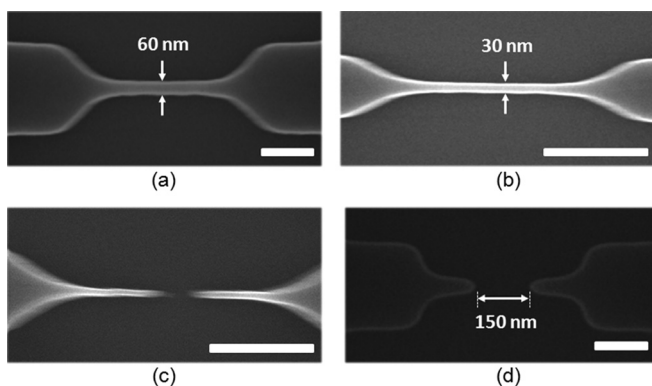


FIG. 2. Top view of SEM images of the photoresist. Initial resist with a line width of 180 nm was trimmed down to (a) 60 nm and (b) 30 nm. (c) Further trimming resulted in two separated patterns with a sharp concave tip. (d) Subsequent resist reflow process softened and rounded by the thermal reflow.

tice, ashing of about 150 nm was done so that lines with a width of under 300 nm were disconnected with a height of 250 nm remaining. The remaining height guaranteed the etch selectivity tolerance between the photoresist and the silicon. The distance between the electrodes can be varied by the layout and the ashing conditions. An initial line width of 180 nm was subsequently reduced by oxygen plasma treatment until the line was discontinued, forming two separated electrodes with 150 nm gap. Though the limit of the optical lithography tool was 180 nm, a sub-lithographic width of 150 nm was achieved by the ashing. The geometrical factors of the emitter, such as aperture and radius, influence the performance and reliability.¹¹ Two different shapes were assessed here: sharp concave and softened convex tips. The needle-like apex can be softened and rounded by the thermal reflow of the photoresist. The sharp apex was rounded at 160 °C for 60 s, and the top silicon was etched, followed by the photoresist removal, leaving a rounded tip with a 14 nm radius of curvature.

Whereas the carrier transport of solid-state transistors is dominated by a drift-diffusion mechanism, the vacuum channel transistor relies on thermionic emission and tunneling. Figure 3 shows the energy band diagram of the vacuum channel transistor at on- and off-states. When the gate voltage is less than the turn-on voltage, some electrons are emitted over the barrier due to thermal energy, but the current is limited since the electrons surmounting the barrier are fewer than electrons at ground level. As the gate voltage increases beyond the turn-on voltage, the vacuum energy level bends downward, thus enabling electron tunneling through a narrow barrier and leading to the on-state of the device.

The field emission capabilities of both emitter shapes mentioned above can be compared in terms of the electric field around the tip. The sharp apex can show a stronger electric field than the rounded counterpart since the electric field tends to be intensified around the sharp corner like a lightning antenna. Unfortunately, the sharp tips ruptured after a single measurement, which can be explained by the local evaporation of the cathode. The higher electric field at the sharp tip involves larger discharge energy, and then arcing can form craters or induce localized melting of silicon. Therefore, the tip rounding process is essential unless the material is reinforced to withstand the thermal and mechanical stresses. The field emission performance tends to degrade if the emitter tip becomes blunt which can be mitigated as the spacing gets narrower. In order to elucidate the field emission performance, simulations were performed using

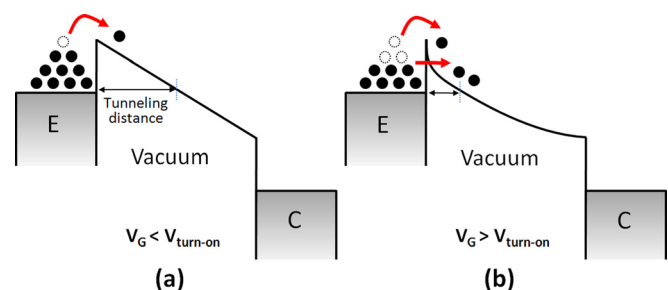


FIG. 3. Energy band diagram of the vacuum channel transistor for (a) $V_G < V_{\text{turn-on}}$ and (b) $V_G > V_{\text{turn-on}}$.

COMSOL simulator¹² for a set of face-to-face electrodes and two different shapes of the tips. Figure 4(a) displays the computed turn-on voltage versus the spacing from the simulations. The turn-on voltage is defined as the voltage required to obtain an electric field of $1 \text{ V } \mu\text{m}^{-1}$ around the tip.^{14,15} As the spacing decreases, the turn-on voltages for the two types of tips converge. A simple electrostatic model supports the findings from the simulation. The field enhancement factor, β , is modeled with the tip radius and the distance between the emitter and the collector. As a high β enables low turn-on voltage and high emission current, the model can provide an intuition on how the design and size affect the performance. The model suggests that $\beta \propto d^{-1}$ and $\beta \propto r^{-1/2}$, where d is spacing and r is the radius of the emitter apex.¹³ A decrease in spacing increases β linearly, whereas a decrease in curvature increases β with a power of 0.5, which implies that the space scaling might be more efficient than sharpening the tip. In other words, a blunt tip can be deployed if the space is sufficiently scaled down.

The characteristics of the vacuum channel transistor are analogous to the solid-state transistor. At a given V_g , the collector voltage (V_c) triggers the field-emitted I_c . Figures 4(b) and 4(c) show transfer (V_g vs. I_c) and output (V_c vs. I_c) characteristics, respectively. The threshold voltage obtained by linear extrapolation is around 8.9 V and the subthreshold slope is 4.2 V/dec. The drive current is of the order of $10 \mu\text{A}$, and the collector leakage current is the order of 10 pA . The on/off current ratio is 10^6 , and the measured transconductance ($g_m = dI_c/dV_g$) at $V_c = V_g = 10 \text{ V}$ is $0.2 \mu\text{S}$. Thanks to the ballistic transport in vacuum, the frequency response is simply limited by the transconductance and input capacitance. The cut-off frequency (f_t) is $f_t = g_m/2\pi C_{ge}$, where C_{ge}

is gate to emitter capacitance. Since C_{ge} is less than the measurement limit of the commercial LCR meter, the overlap capacitance between back-gate and emitter is estimated to be $C_{gc} = 0.069 \text{ aF}$ for an emitter overlap area of $0.01 \mu\text{m}^2$, and thus, the f_t is estimated to be 0.46 THz .

During device operation, no electrons are emitted from the emitter until the V_c reaches the turn-on voltage and then I_c increases exponentially with respect to V_c , according to Fowler-Nordheim tunneling theory. The output characteristic of MOSFET is distinguished by a linear region at low drain voltage and a saturation region beyond the pinch-off condition. Similarly, the I_c - V_c of vacuum devices can also be divided into two distinct regions, except that the I_c versus V_c has an exponential relation at low V_c due to Fowler-Nordheim tunneling nature. The saturation region is supposed to appear at higher V_c , but only the exponential region is displayed in Fig. 4(c) as the device was severely damaged at high voltages. In the present structure, a back-gate configuration was used so that the back-gate overlapped with the emitter. The gate-to-emitter overlap in conjunction with the thin insulator is very attractive because the overlap enhances the gate controllability while the insulator prevents the parasitic gate leakage. The gate leakage current (I_g) was measured to be negligible as seen in Fig. 4(d), thanks to the gate insulator. A thinner gate insulator can obviously improve the gate field effect, and an ultra-thin buried oxide wafer indeed has the potential of boosting the performance of the device.

In this work, the geometries of the emitter and collector are identical so that the point-to-point electron projection causes symmetrical I_c - V_c characteristics in the forward and reverse biased regimes, which is undesirable in circuit design. The shapes of the emitter and the collector need to be point-to-plane configuration in order to obtain diode-like I_c - V_c characteristics. The symmetric electrodes here resulted from the fact that the initial straight line was subjected to isotropic ashing. The point-to-plane configuration could be attained from a trapezoidal shape, indicating the need for a further layout optimization. Although the measurements here were carried out at the individual device level, packaging techniques with vacuum encapsulation would enable implementation in practical applications.¹⁶

In summary, a planar lateral air transistor was fabricated using standard silicon semiconductor processing. The emitter and collector were sub-lithographically separated by photoresist ashing, with the curvature of the tip controlled by the thermal reflow of the photoresist. The gap can be shrunk as small as 10 nm in the future using this process. Since the nanogap separating the emitter and collector is smaller than the electron mean free path in air, vacuum is not needed. The present structure exhibits superior gate controllability and negligible gate leakage current due to adoption of the gate insulator. The device has potential for high performance and low power applications; also, since vacuum as the carrier transport medium is immune to high temperature and radiation, the proposed nanotransistors are ideal for extreme environment applications in military and space. Process and layout refinements such as coating a low workfunction material on the emitter, reducing the overlap area and optimizing the oxide thickness can potentially improve the cut-off frequency well into the THz regime. The THz frequency

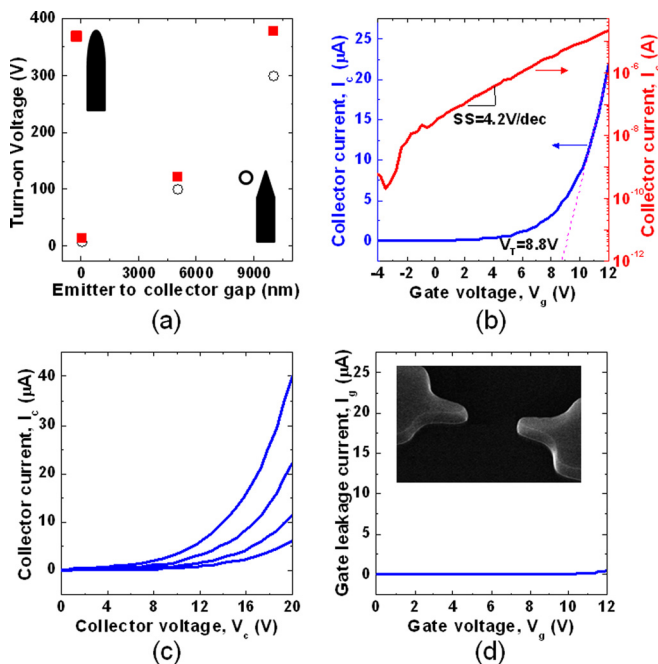


FIG. 4. (a) Simulation results for the turn-on voltage for two different emitter shapes; square symbols for hemiellipsoid tips and circle symbols for sharp tips. The difference in turn-on voltage for the two structures becomes reduced as the emitter-to-collector distance decreases. (b) I_c - V_g for $V_c = 10 \text{ V}$, (c) I_c - V_c characteristics for $V_g = 5, 6, 7,$ and 8 V , and (d) I_g - V_g characteristics for $V_c = 10 \text{ V}$.

operation of the vacuum channel transistor would be useful for applications in hazardous chemical sensing, noninvasive medical diagnostics, and high-speed telecommunications.

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