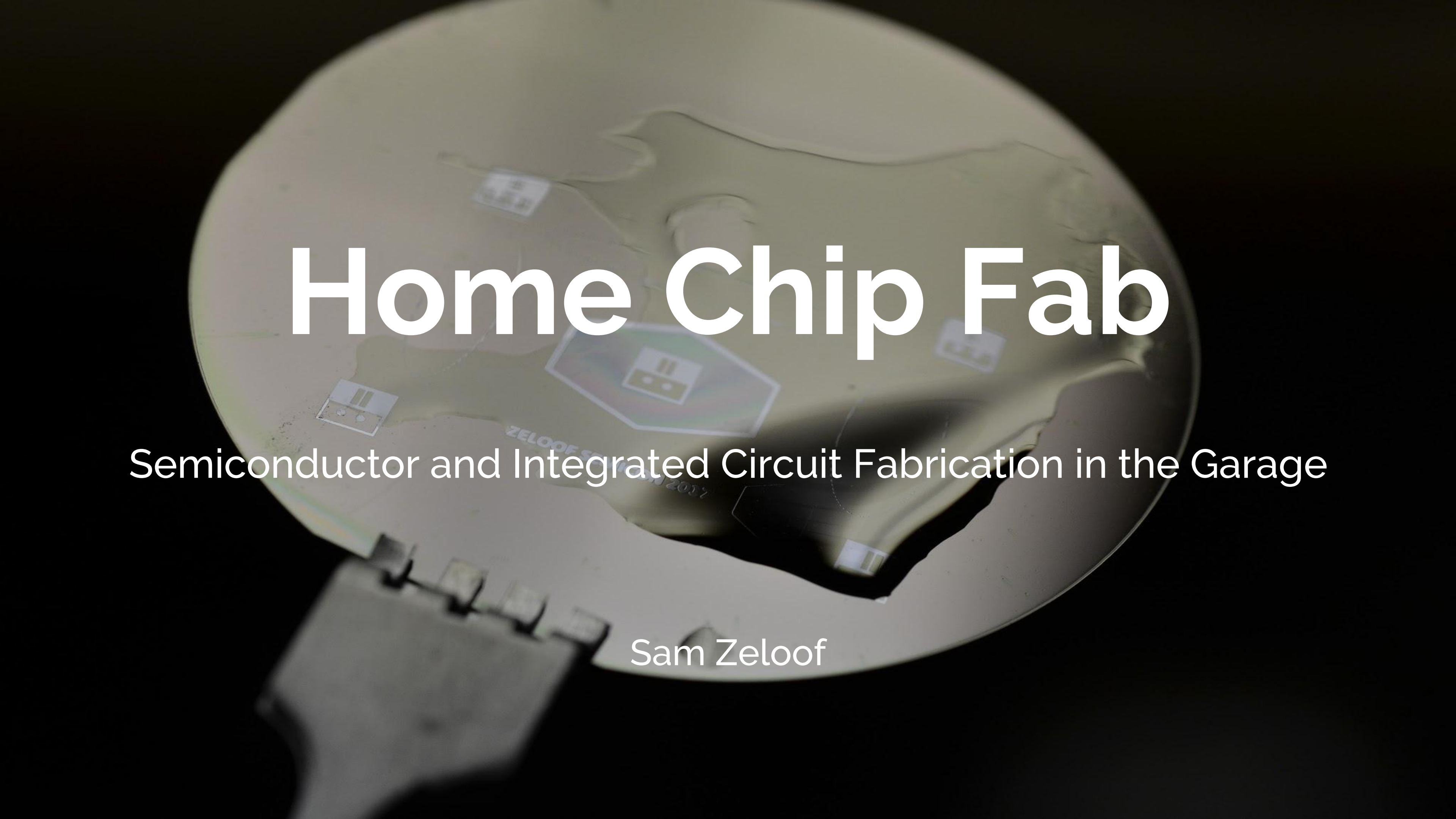


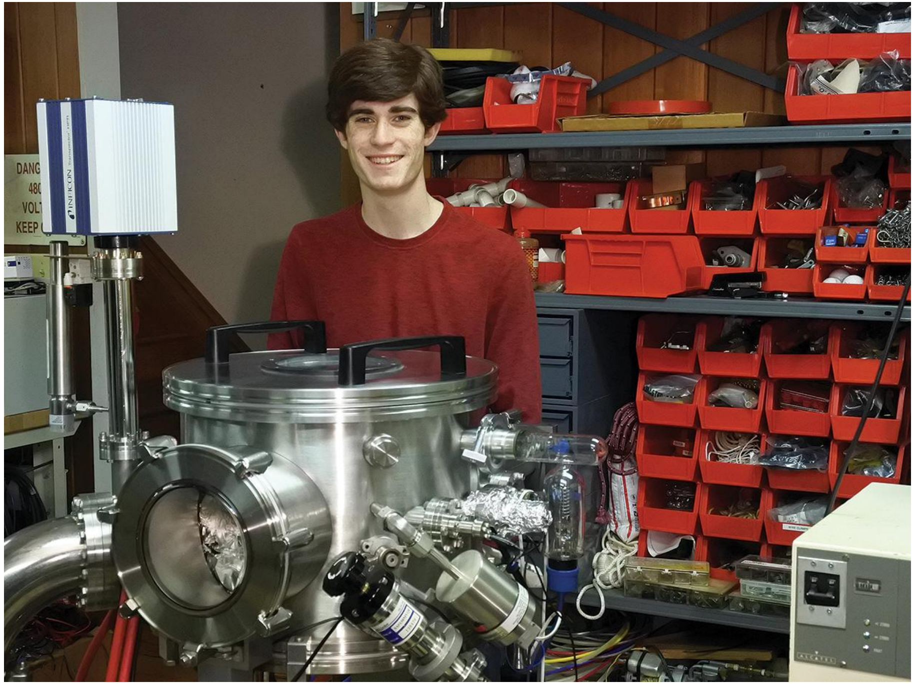
Home Chip Fab

Semiconductor and Integrated Circuit Fabrication in the Garage

Sam Zeloof

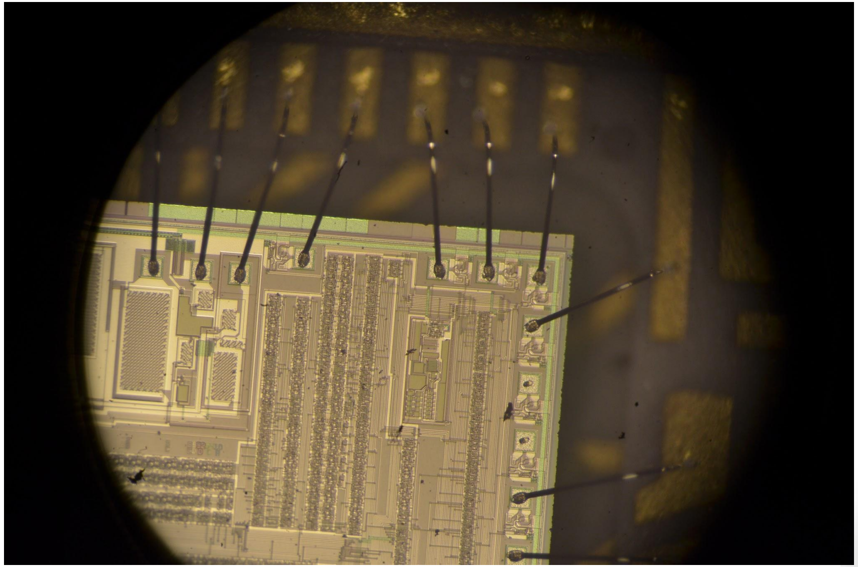
Outline

- Brief project overview
- Semiconductor physics basics
- Semiconductor fabrication

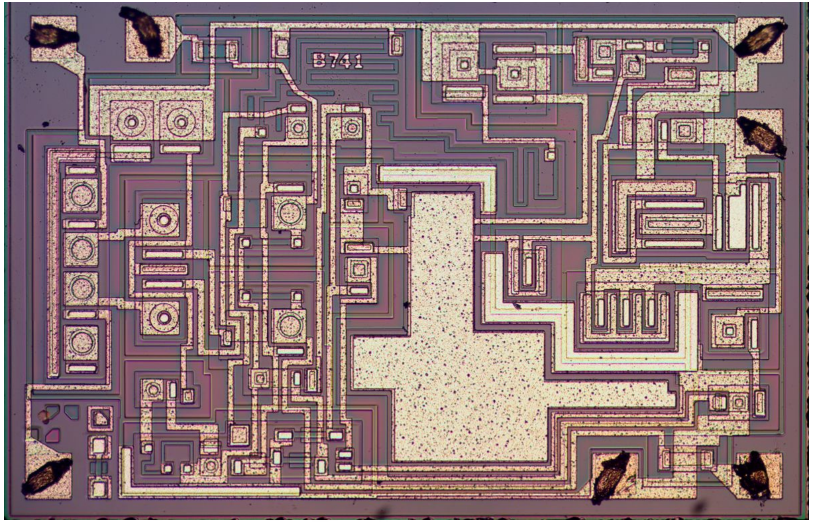


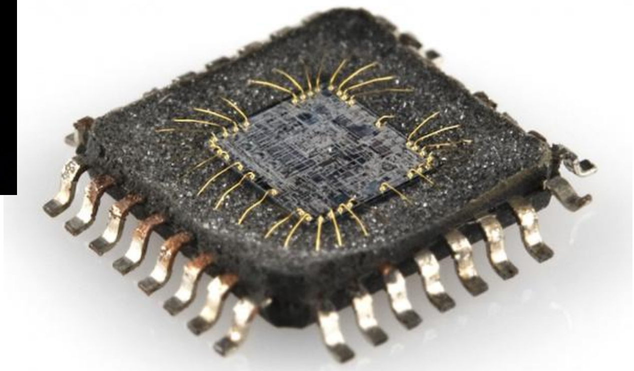
Project Overview

The goal…



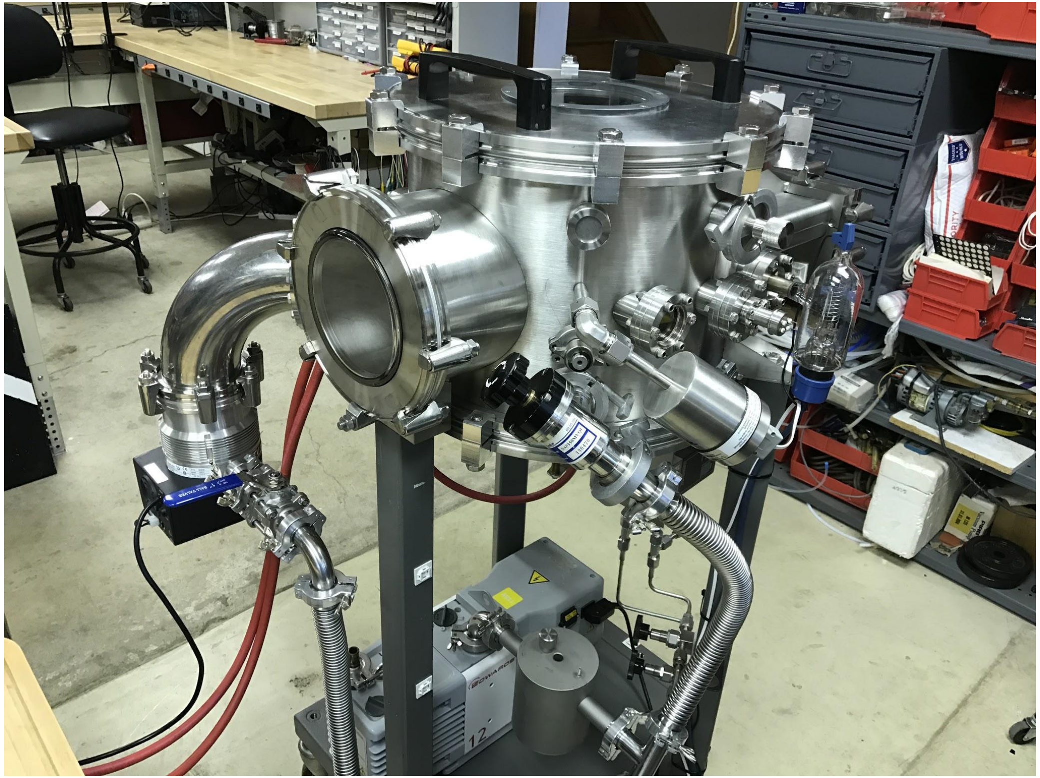
Jeri Ellsworth - DIY Transistors

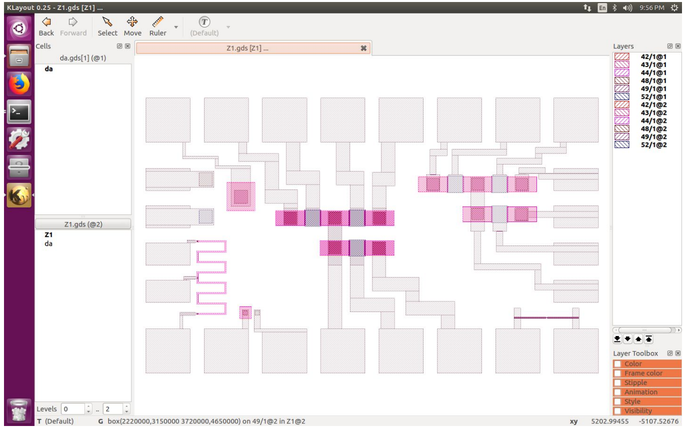




Computer → PCB → IC→ Logic gates/memory→ Transistors → Electrons

Over the past year and a half...



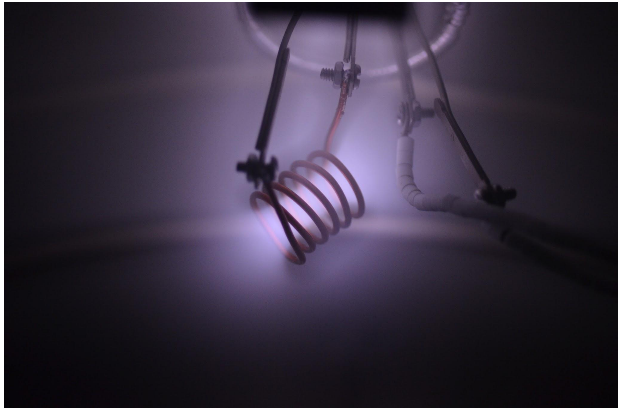


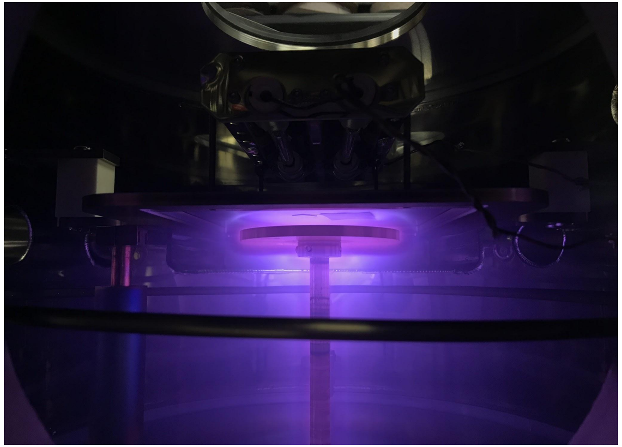
KLayout 0.25 - Z1.gds [Z1] ...

Levels 0 .. 2

T (Default) G box(2220000,3150000 3720000,4650000) on 49/1@2 in Z1@2 xy 5202.99455 -5107.52676

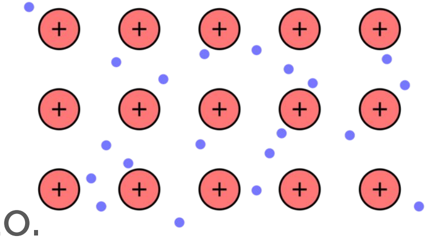
Over the past year and a half...





Semiconductor Physics 101

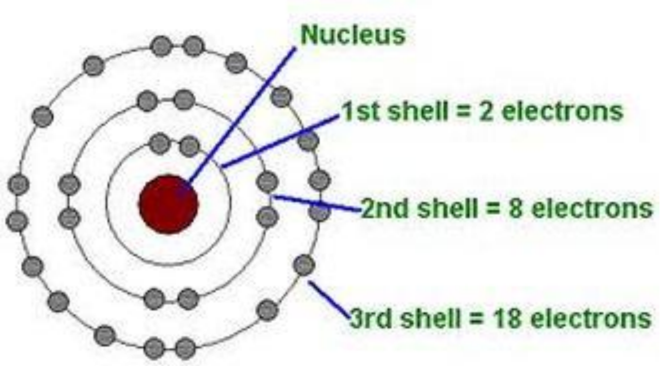
Semiconductor Physics 101

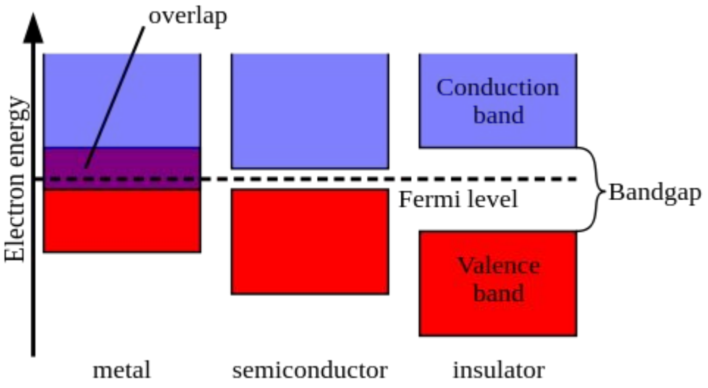


Some things conduct electricity, some don't, and some *kinda* do.

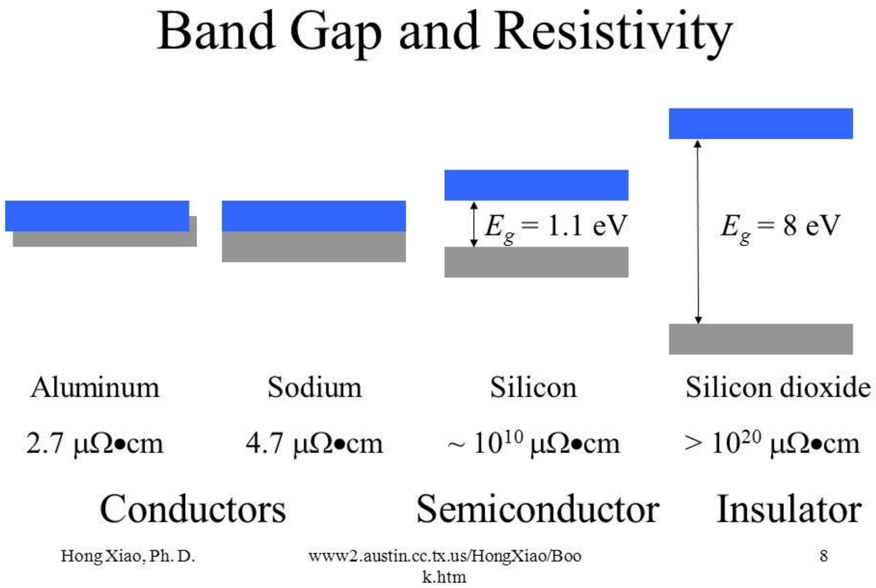
- Electrons exist in different energy levels
- Higher energy levels are more suited for conduction

Bandgap: the difference in energy between the valence band and the conduction band of a solid material





Semiconductor Physics 101

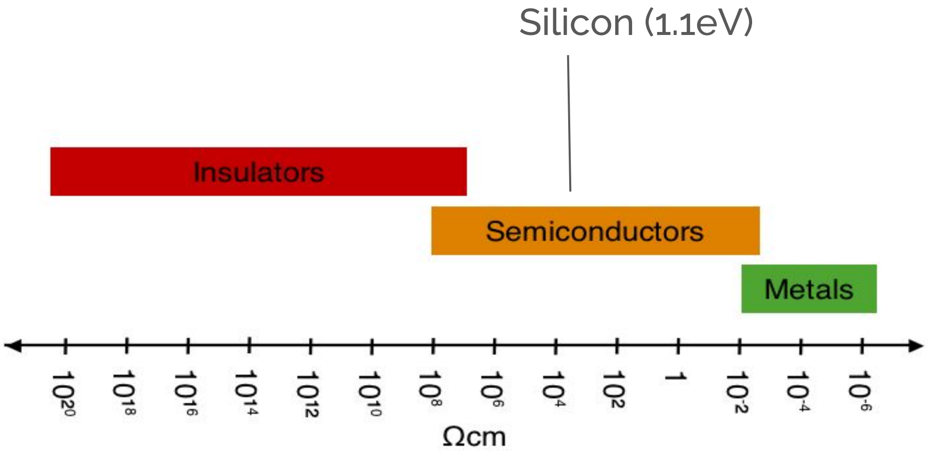


Band Gap and Resistivity

Aluminum	Sodium	Silicon	Silicon dioxide
2.7 μΩ•cm	4.7 μΩ•cm	~ 10^{10} μΩ•cm	> 10^{20} μΩ•cm
Conductors		Semiconductor	Insulator

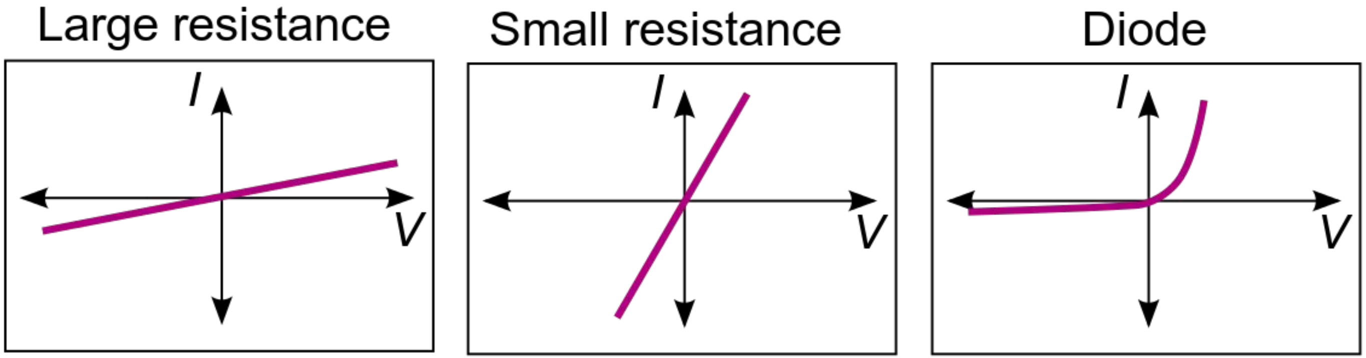
Hong Xiao, Ph. D. www2.austin.cc.tx.us/HongXiao/Book.htm 8

(Also why glass is transparent)



The bandgap inherent in semiconductors is the key to making useful devices (i.e. solar cell. Transistor, etc.)

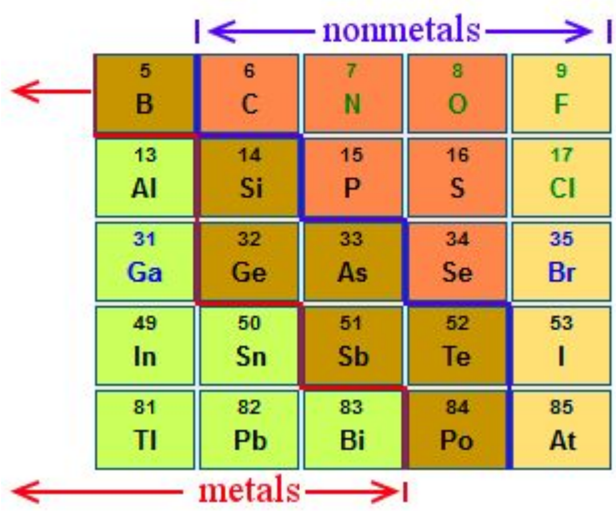
IV Curves



The electrical properties of semiconductors can be engineered to have “useful nonlinearities”

Doping and the PN Junction

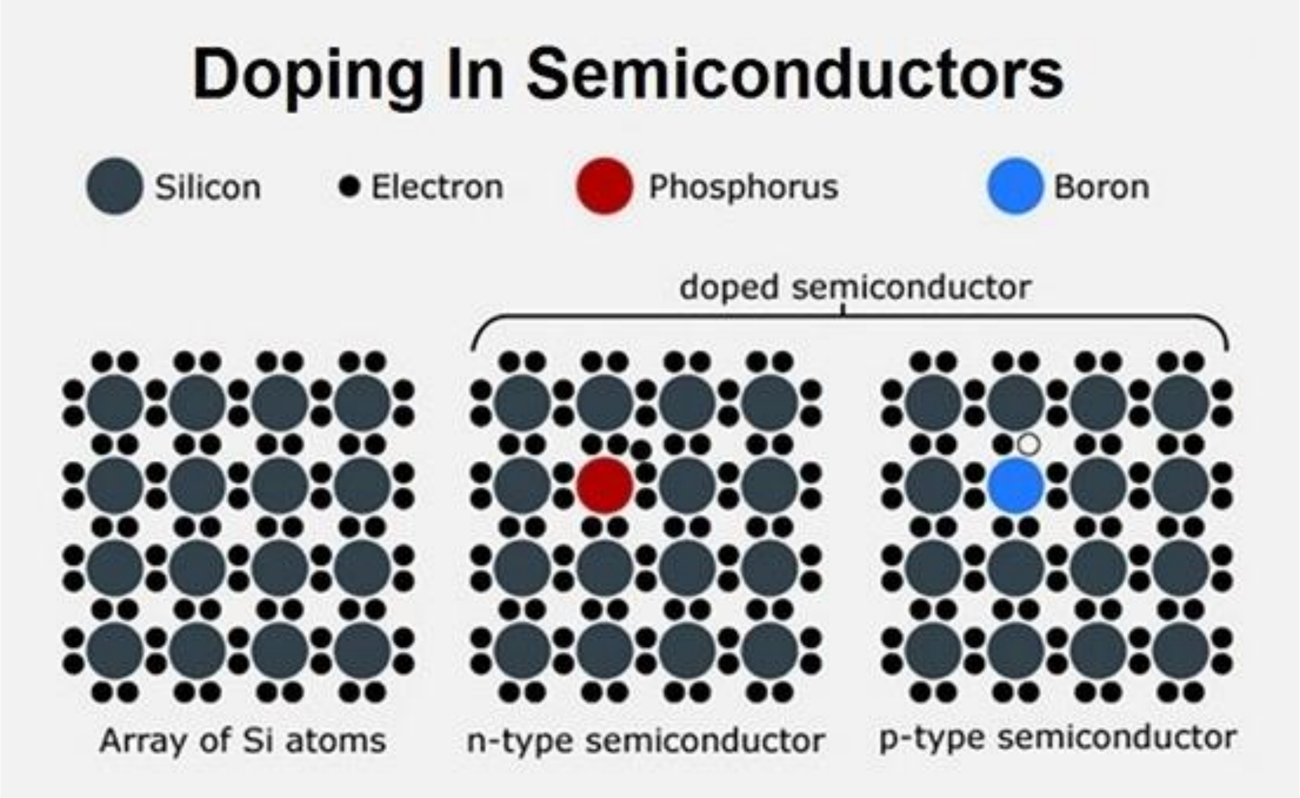
- Doping - adding small amounts of impurity to semiconductor crystal (Silicon) to modify electrical characteristics
- Hole - The absence of an electron (electron acceptor)



5 B	6 C	7 N	8 O	9 F
13 Al	14 Si	15 P	16 S	17 Cl
31 Ga	32 Ge	33 As	34 Se	35 Br
49 In	50 Sn	51 Sb	52 Te	53 I
81 Tl	82 Pb	83 Bi	84 Po	85 At

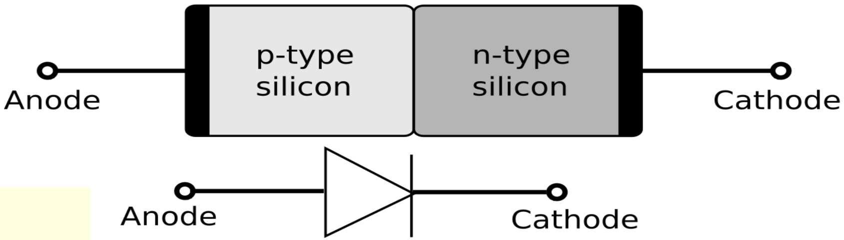
N type dopant - Negative, extra electrons (Phosphorus)

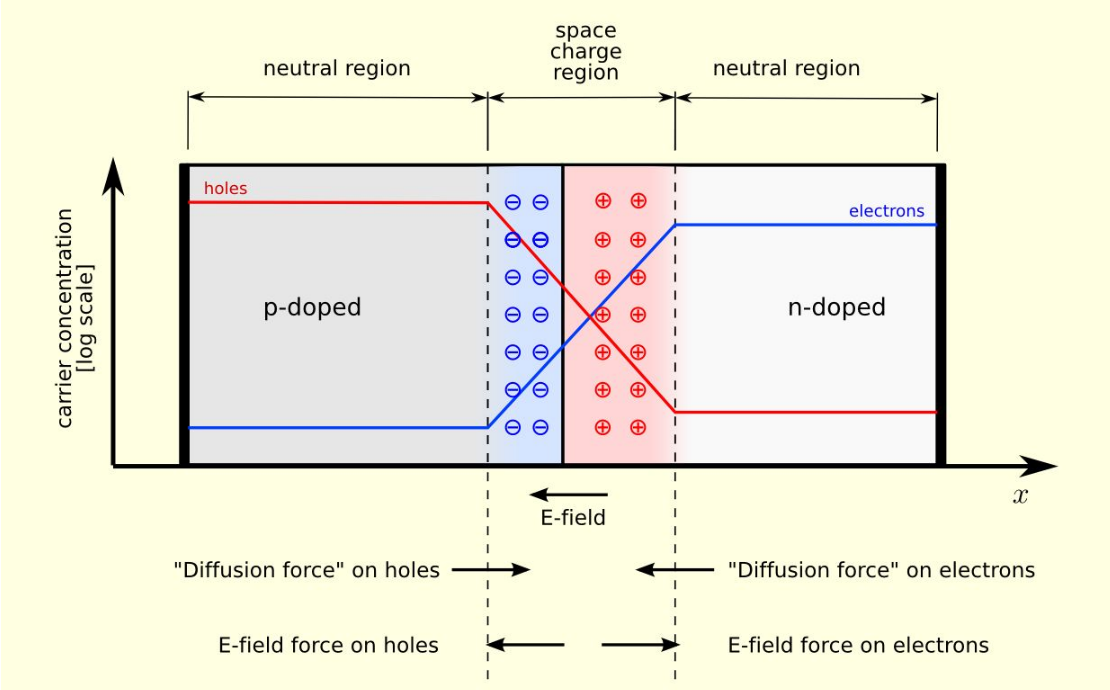
P type dopant - Positive, extra holes (Boron)



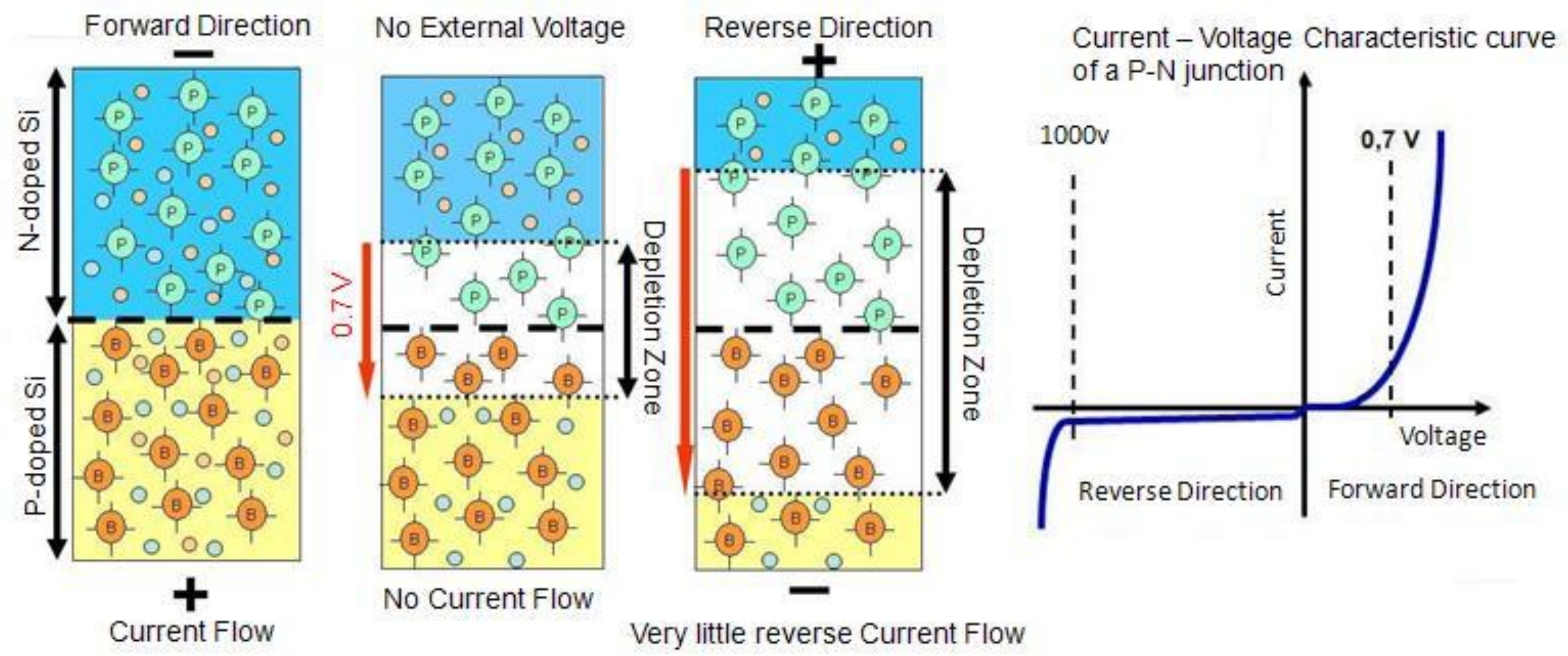
Doping increases conductivity, causes wave functions that describe electrons in valence and conduction bands to overlap and lowers the band gap. Overall adds charge carries, either electrons or holes.

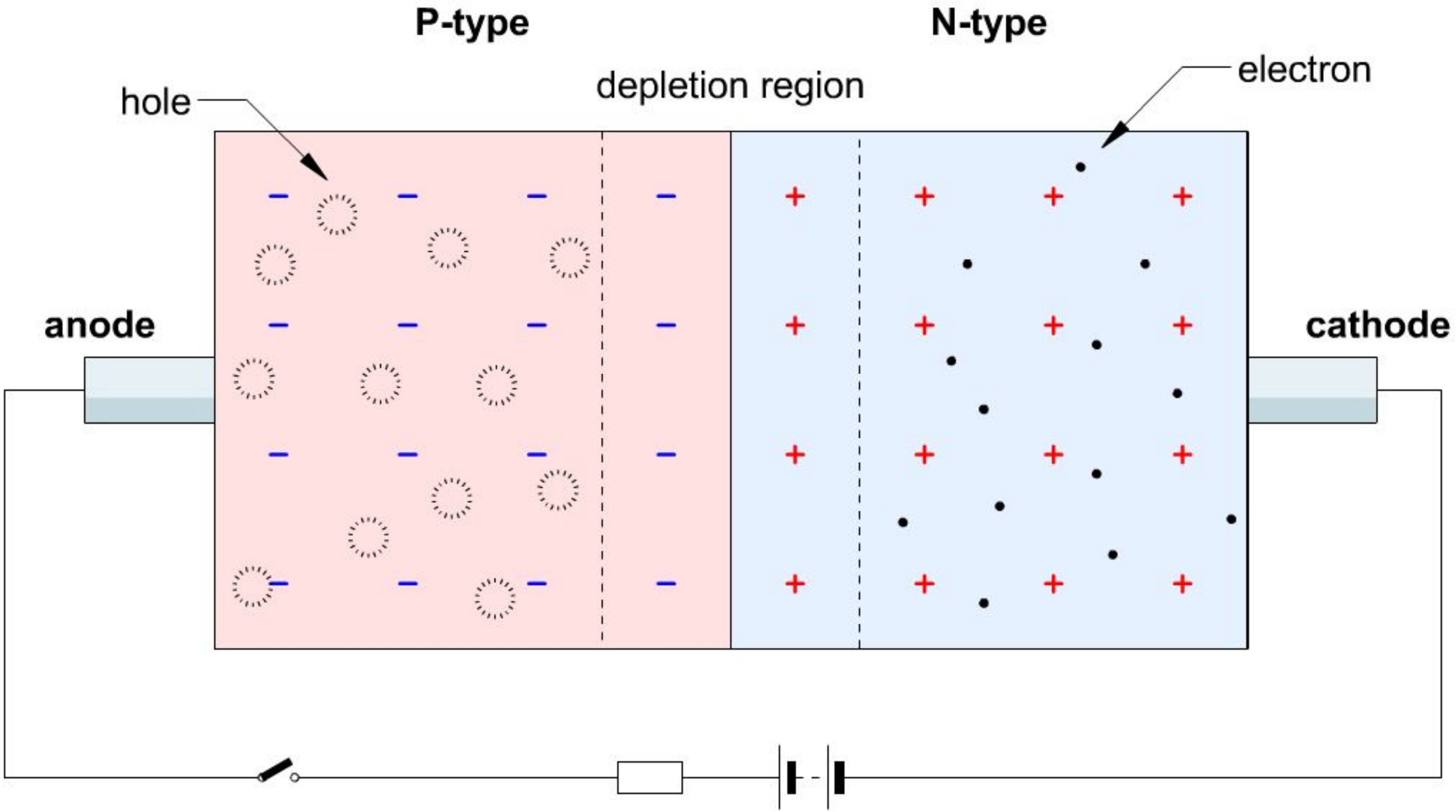
The PN Junction





The PN Junction

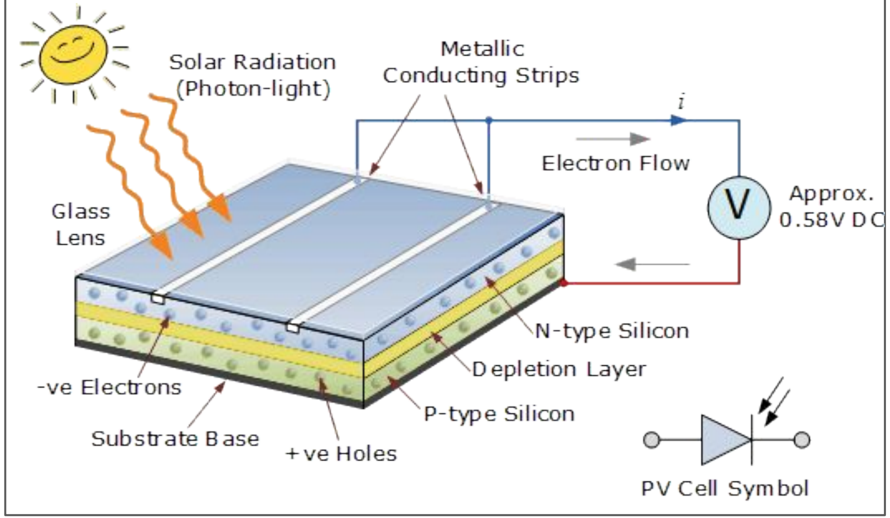



P-type
N-type
depletion region
hole
electron
anode
cathode

The PN Junction (cont.)

Not only can the PN junction rectify current, but it can also convert radiation (light, X-rays, etc) to electrical current or electrical current to light.

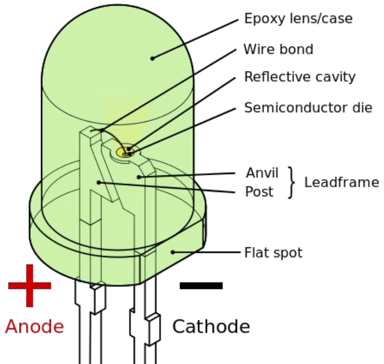
Solar (Photovoltaic) cell:
Photogeneration of charge carriers

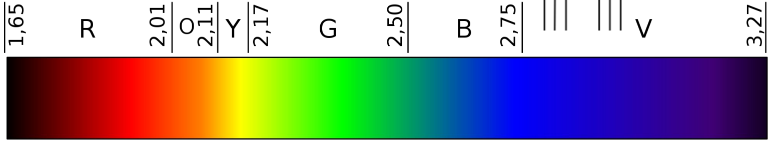


LED (Light Emitting Diode):
Charge carrier recombination induced electroluminescence

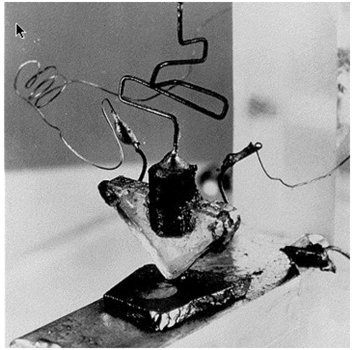
Bandgaps are engineered to color

GaP - 2.3eV

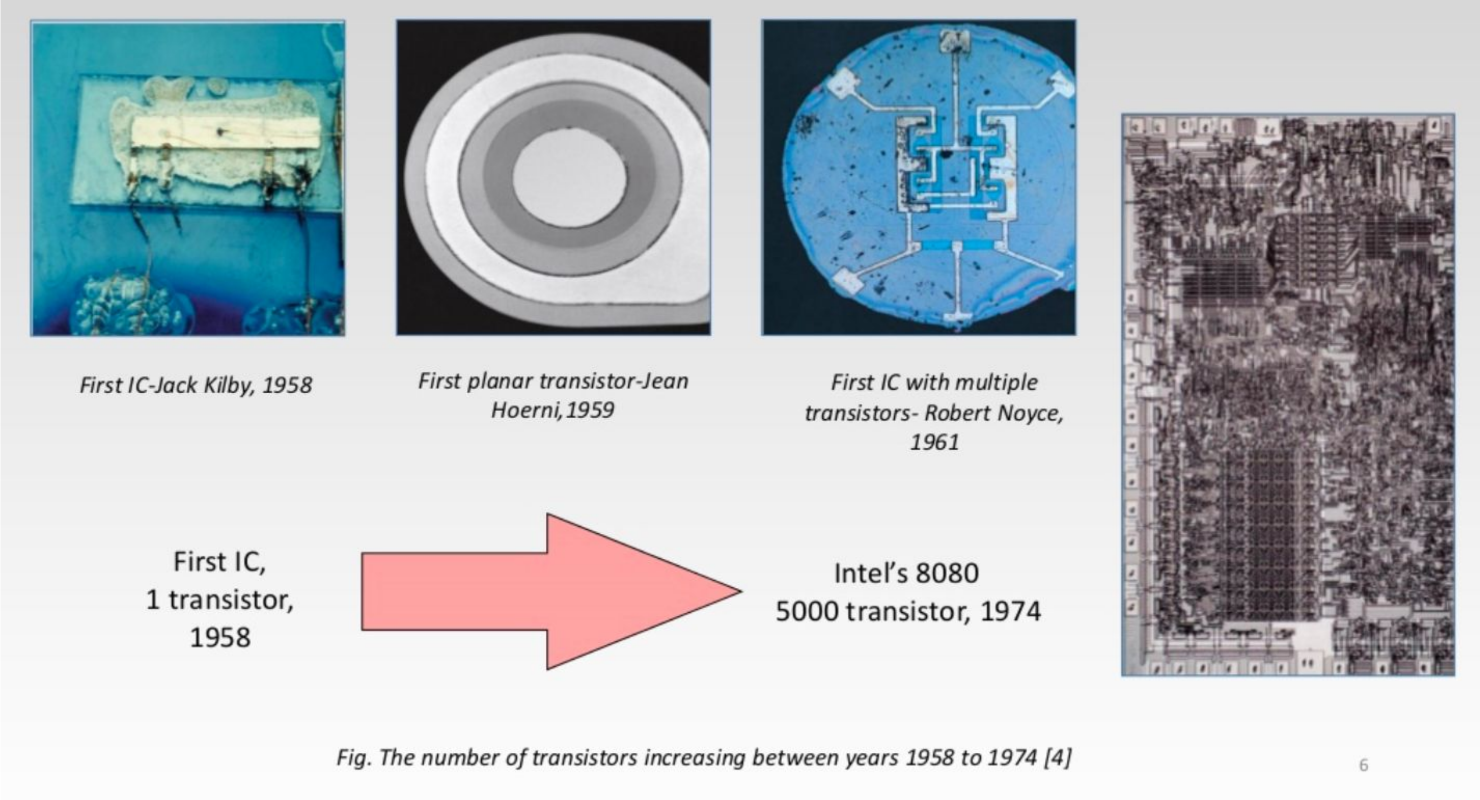




The Transistor



First Transistor, 1947



First IC-Jack Kilby, 1958

First planar transistor-Jean Hoerni,1959

First IC with multiple transistors- Robert Noyce, 1961

First IC,
1 transistor,
1958

Intel's 8080
5000 transistor, 1974

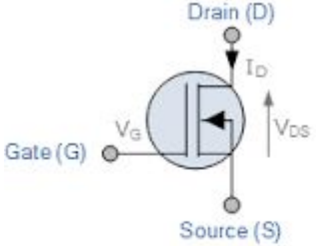
Fig. The number of transistors increasing between years 1958 to 1974 [4]

6

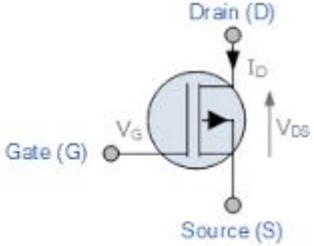
The MOSFET

Metal Oxide Semiconductor Field Effect Transistor

G = Gate
S = Source
D = Drain
TAB = Drain



N-channel



P-channel

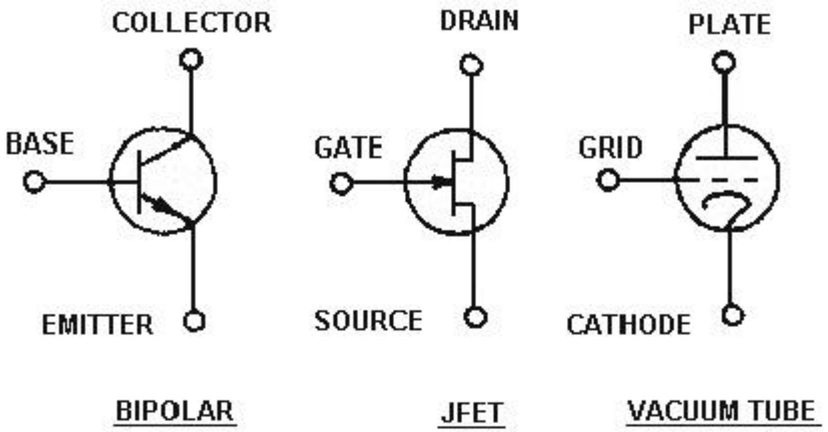
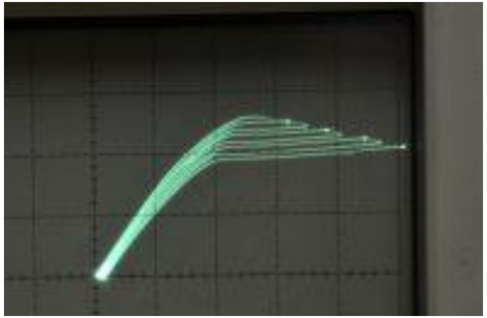
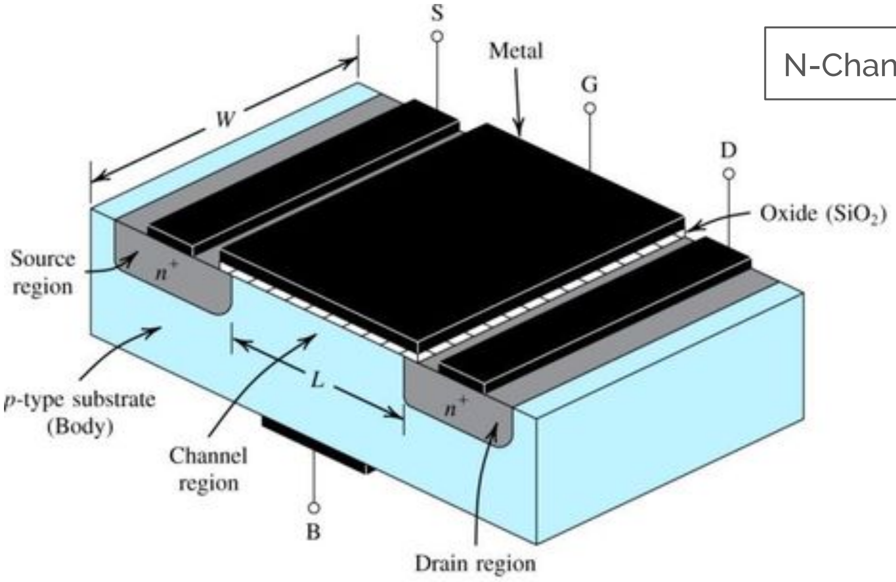


Figure 3-44.—Comparison of JFET, transistor, and vacuum tube symbols.

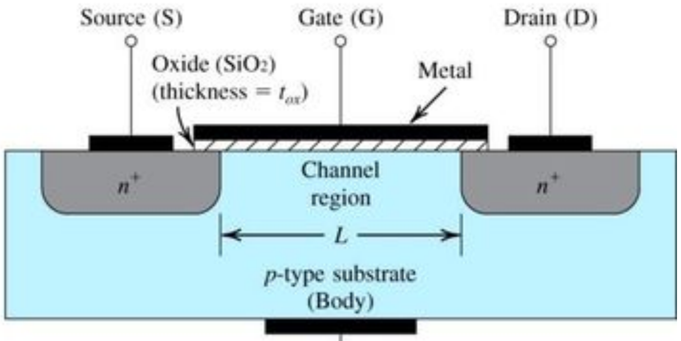
MOSFET Operation



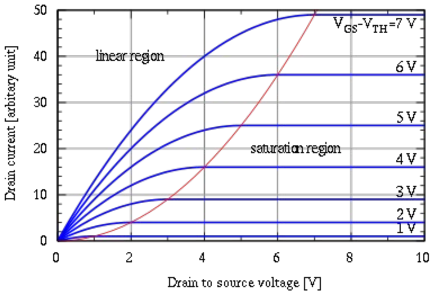
N-Channel Enhancement Mode FET



(a)



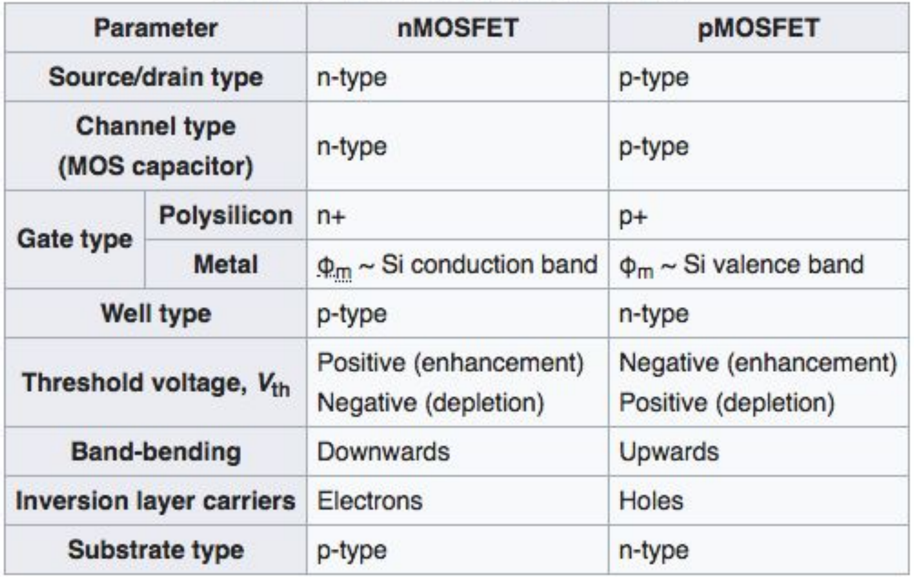
(b)



A positive voltage on the gate repels holes from the channel region and “inverts” it to N type so current can flow across the device

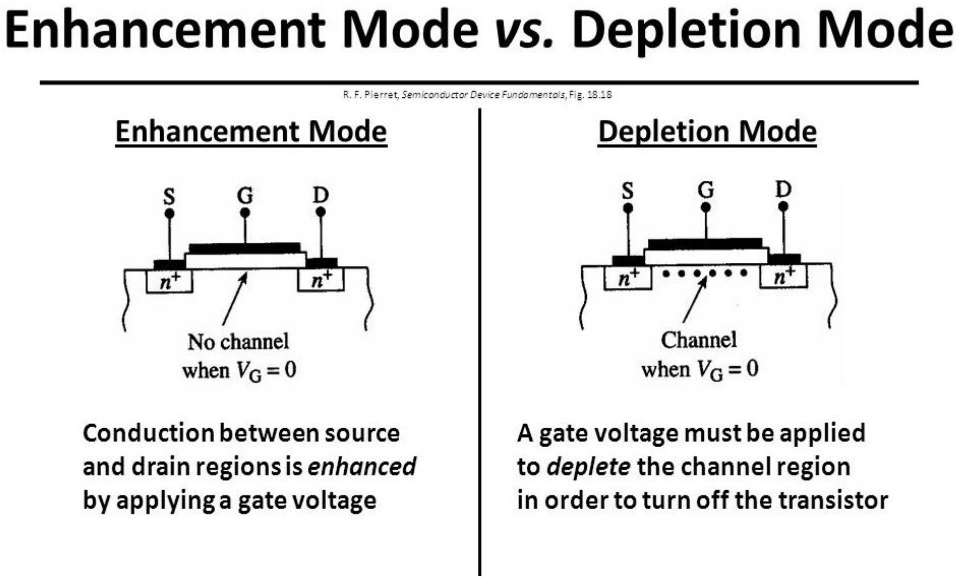
MOSFET Operation

Comparison of n- and p-type MOSFETs[7]



Parameter		nMOSFET	pMOSFET
Source/drain type		n-type	p-type
Channel type (MOS capacitor)		n-type	p-type
Gate type	**Polysilicon**	n+	p+
	Metal	ϕ_m ~ Si conduction band	ϕ_m ~ Si valence band
Well type		p-type	n-type
Threshold voltage, V_{th}		Positive (enhancement) Negative (depletion)	Negative (enhancement) Positive (depletion)
Band-bending		Downwards	Upwards
Inversion layer carriers		Electrons	Holes
Substrate type		p-type	n-type

Wikipedia



Enhancement Mode *vs.* Depletion Mode

R. F. Pierret, *Semiconductor Device Fundamentals*, Fig. 18.18

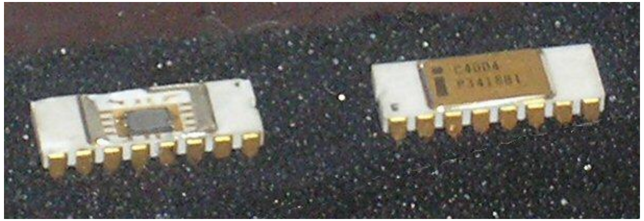
Enhancement Mode

Conduction between source and drain regions is *enhanced* by applying a gate voltage

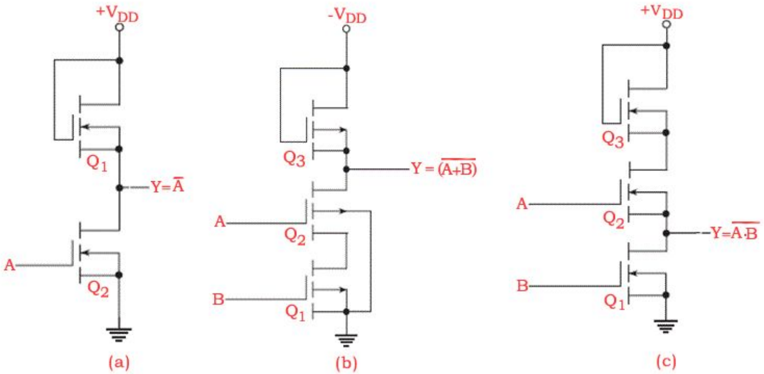
Depletion Mode

A gate voltage must be applied to *deplete* the channel region in order to turn off the transistor

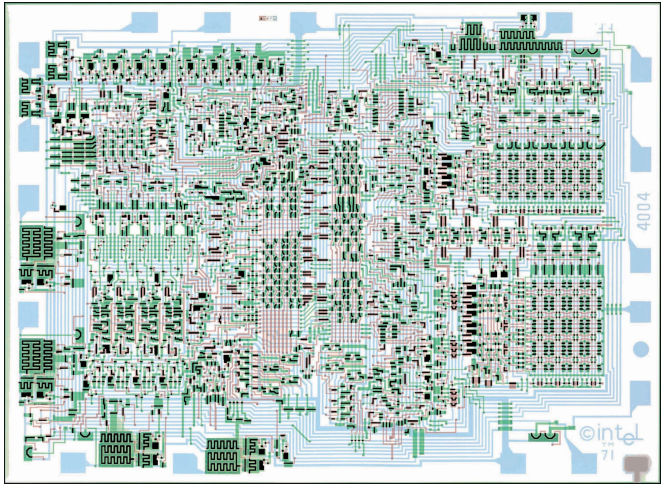
From Transistors to ICs



- Modern processors contain billions of transistors
- Intel 4004 (1969-1970) - 1,800 transistors
- Groups of transistors form logic gates
- Feature/process size = gate length = 10μm to 14nm and beyond



(a) NMOS logic circuit inverter, (b) NMOS logic two-input NOR
and
(c) NMOS logic two-input

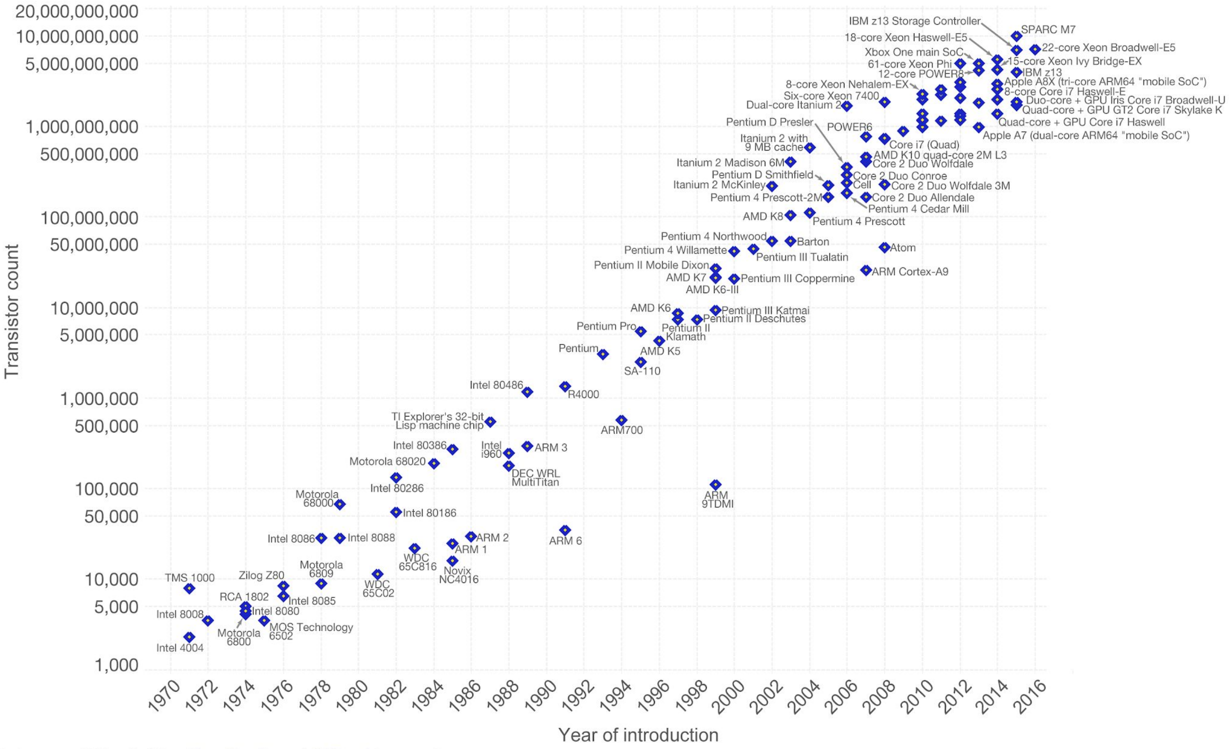


Moore's Law

"The number of transistors in a dense integrated circuit doubles approximately every two years"

Moore's Law – The number of transistors on integrated circuit chips (1971-2016)

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are strongly linked to Moore's law.

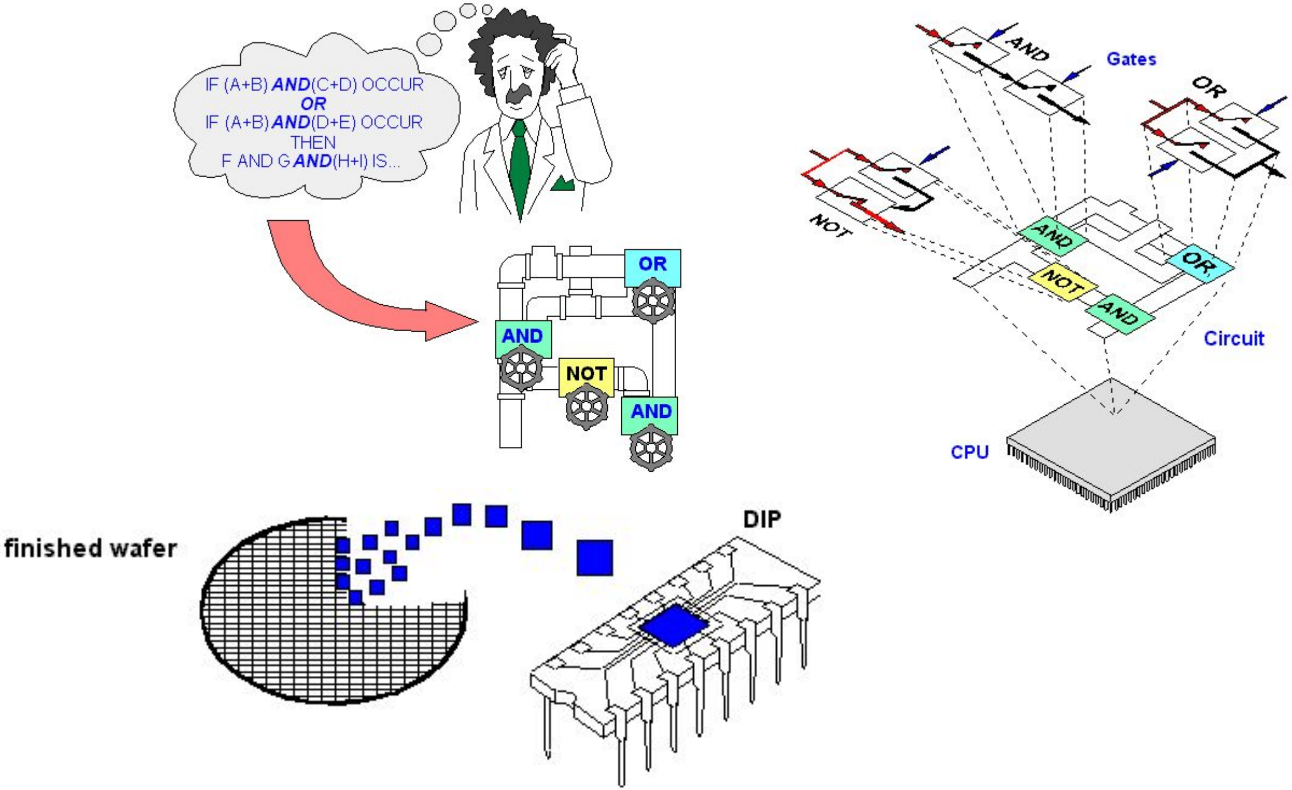


Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

Semiconductor Fabrication

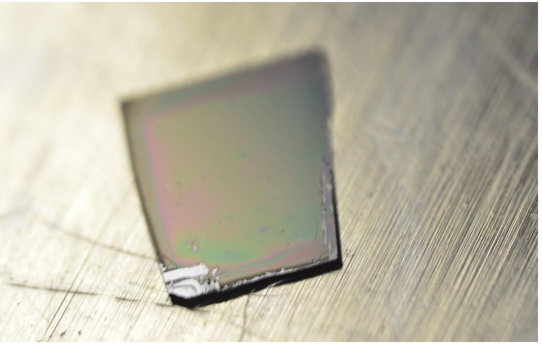
Semiconductor Fabrication

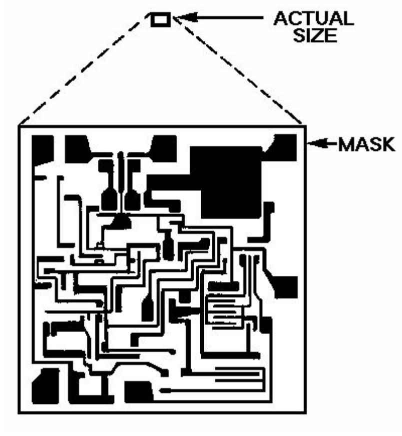
- Patterning
- Doping
- Layering



Patterning - Photolithography

- Etymology - Ancient Greek (writing with light)
- Used to fabricate ICs and PCBs - Features from mm to nm
- Photoresist - A UV sensitive layer is applied to the wafer as a liquid and baked to form a solid layer





- Resist layer is exposed through a mask and developed to leave the pattern on wafer surface, much like making prints in a darkroom

Photolithography

Chris A. Mack, Fundamental Principles of Optical Lithography, (c) 2007

Resist polarity:

Positive - exposed areas are removed during develop

Negative - exposed areas remain during develop

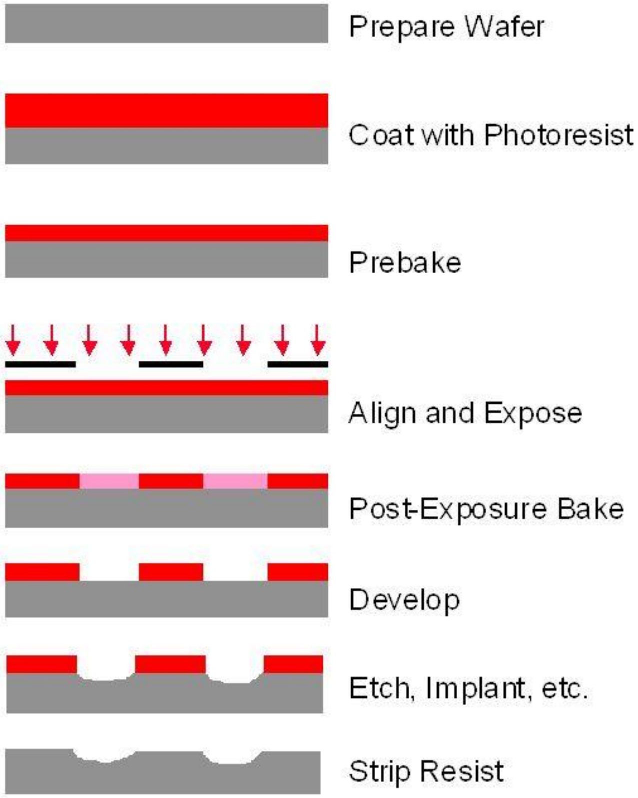
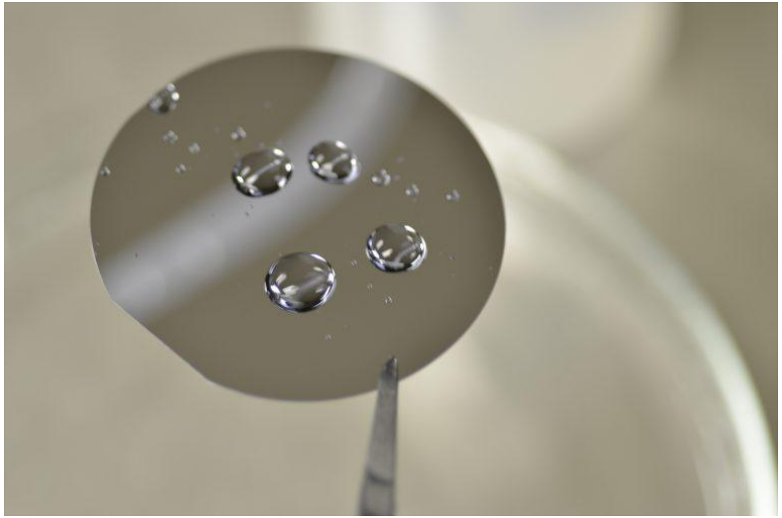


Figure 1.11 Example of a typical sequence of lithographic processing steps, illustrated for a positive resist.

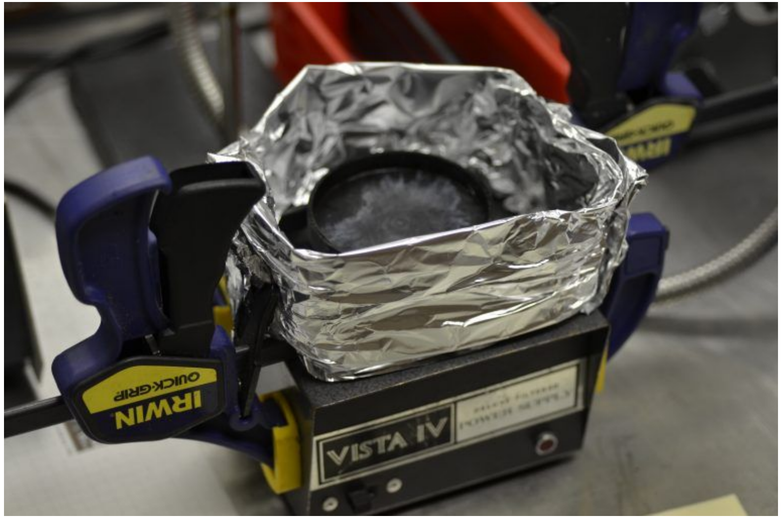
Photolithography - Example Process

1. Dehydration bake - 10 min @ 160˚C
2. Optional spin HMDS
3. Spin AZ 4210 (5510) resist 30 sec @ 3500 rpm ~3.5um (0.9um) film
4. Soft bake resist 1 (1) min @ 105˚C hotplate
5. Expose 200mJ (115mJ) @ 365nm
6. (If using 5510, post bake 105˚C hotplate 1 min)
7. Develop 1:3 400k KOH:H20 (RD6 2.8% TMAH) puddle 40 (60) sec
8. Water rinse (no solvent)
9. Hard bake 5 min @ 115˚C hotplate
10. Etch - HF 20 min or until surface hydrophobic @ 35˚C
11. Water rinse
12. Resist strip - Acetone or O2 plasma
13. Acetone then IPA then water rinse

Photolithography (cont.)

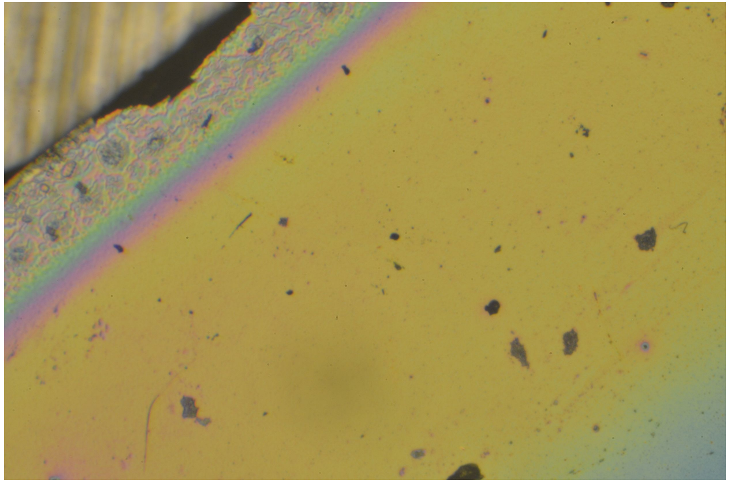


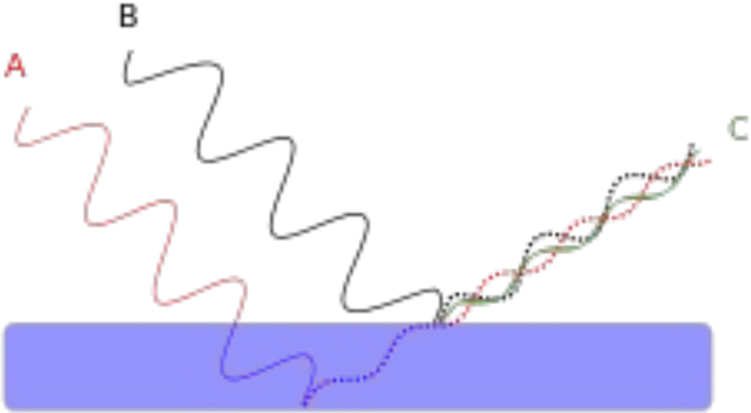
Hydrophilic Silicon Wafer



Spin Coater (PC fan)

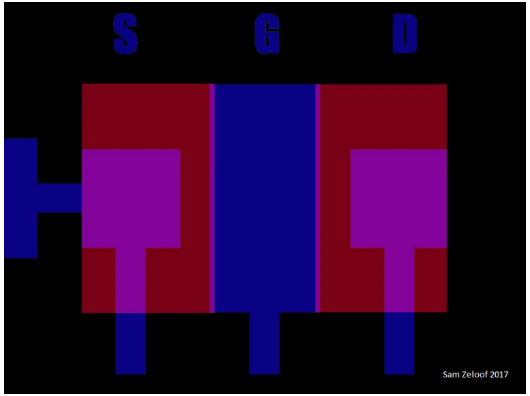
Photolithography (cont.)

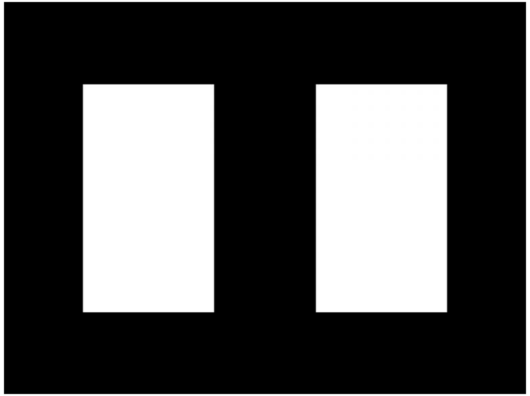


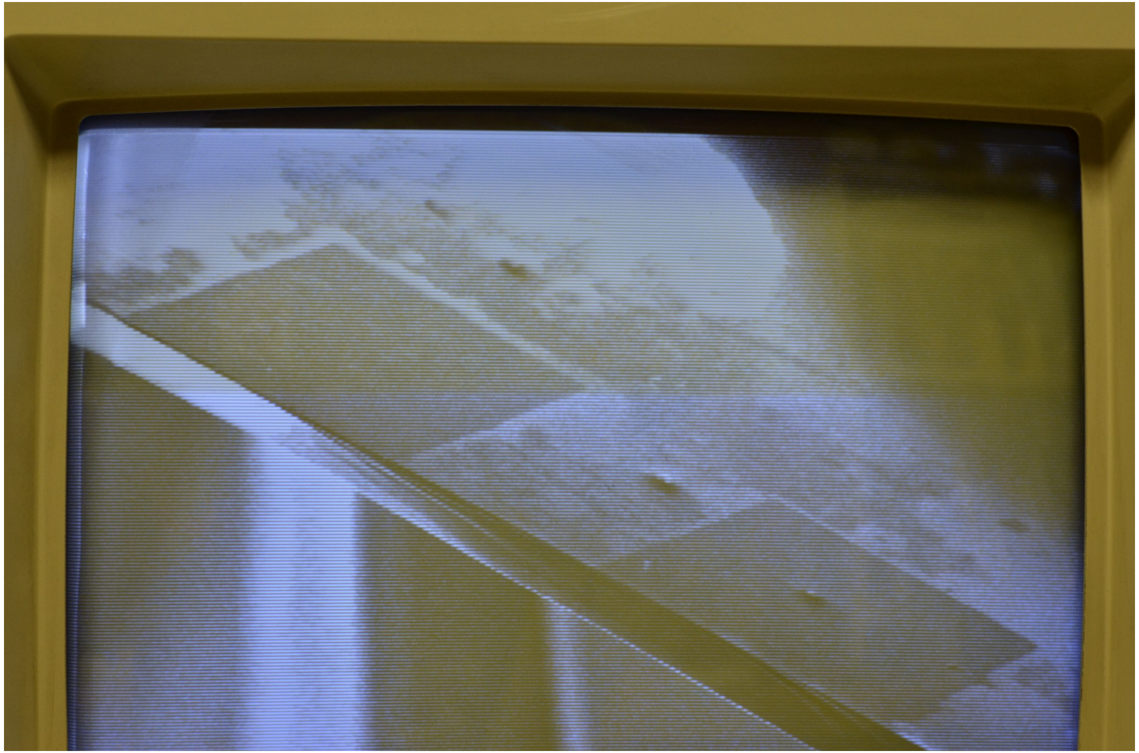


Thin Film Interference

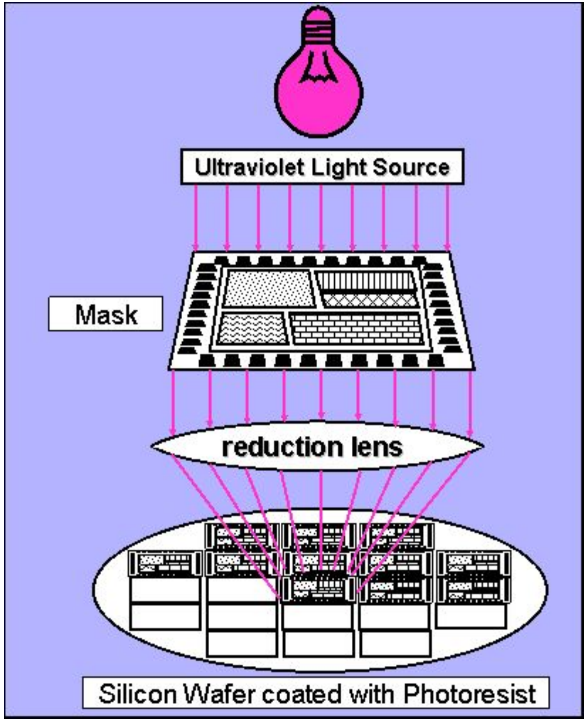
Photolithography (cont.)







Photolithography (cont.)



Traditional Mask Lithography

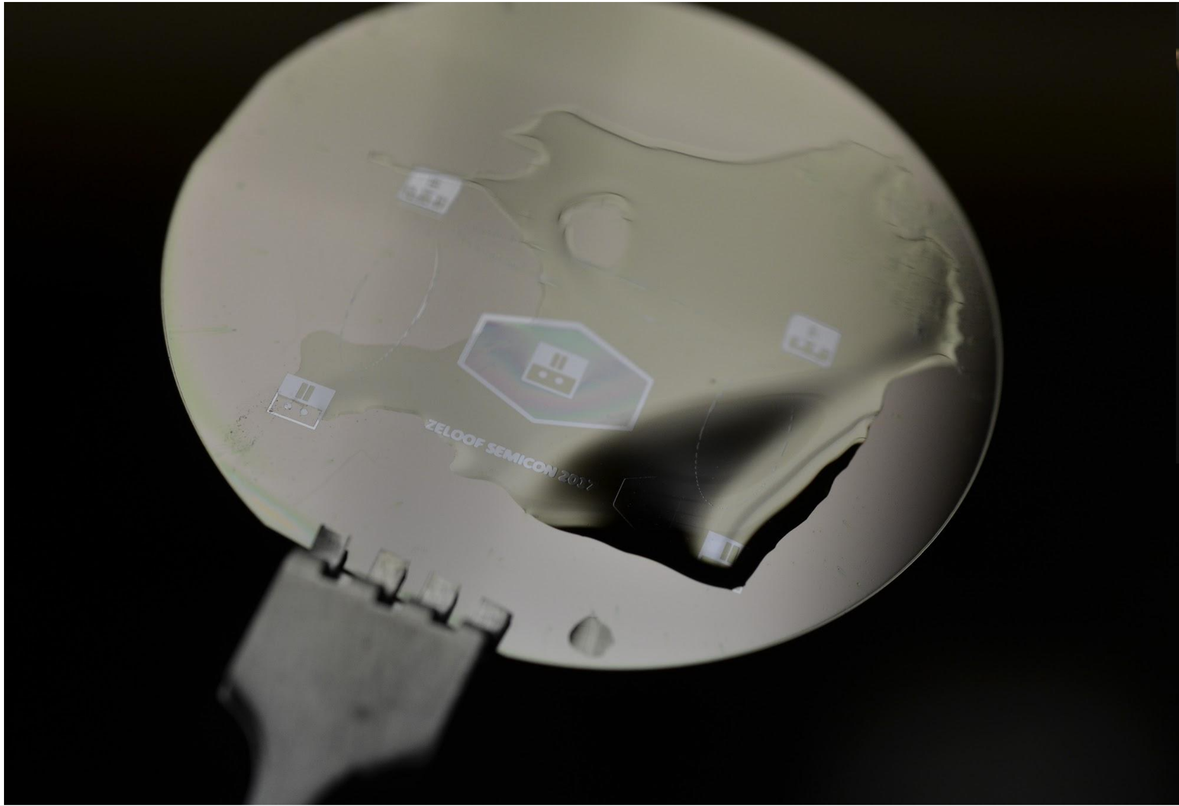
Projection Maskless Lithography

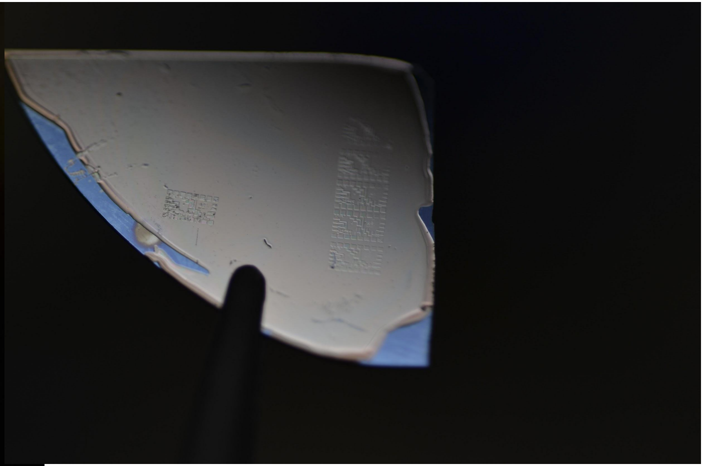
Maskless Photolithography

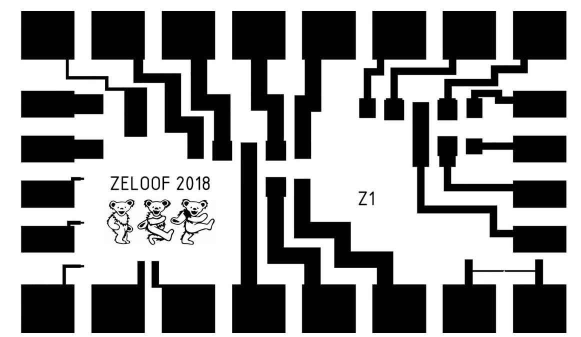
V1 - 10μm

V2 - deep submicron

Maskless Photolithography (cont.)



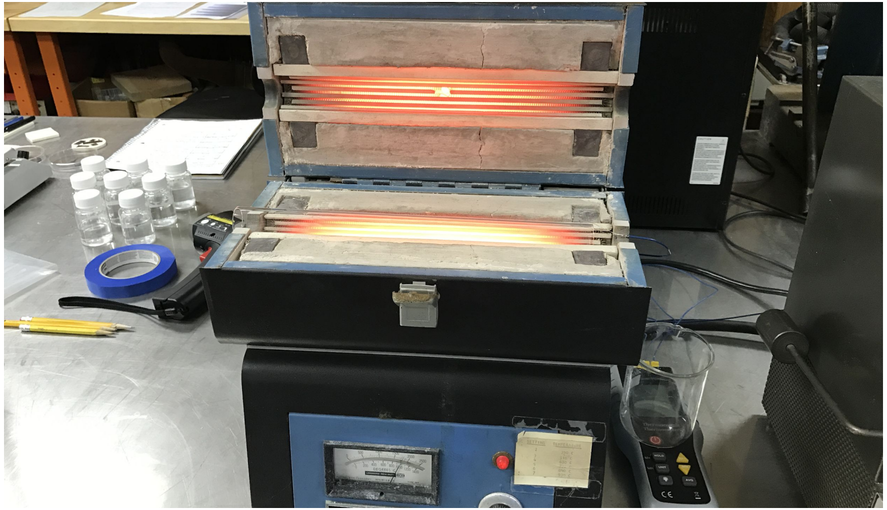




Doping

- Diffusion - high temperatures > 900˚C drive dopant atoms into Si lattice
  - Spin on dopant
    - Phosphoric acid (N)
    - Boric acid (P)
  - Solid source - BN, elemental Phosphorus
  - Gas source - Phosphine, Diborane
- Ion implantation - dopant gas is ionized and accelerated into Si wafer at high velocity
  - 25keV - 1MeV
  - Hazardous gases and high voltage required
  - Precise dopant concentration and depth control
  - Gate threshold voltage tuning

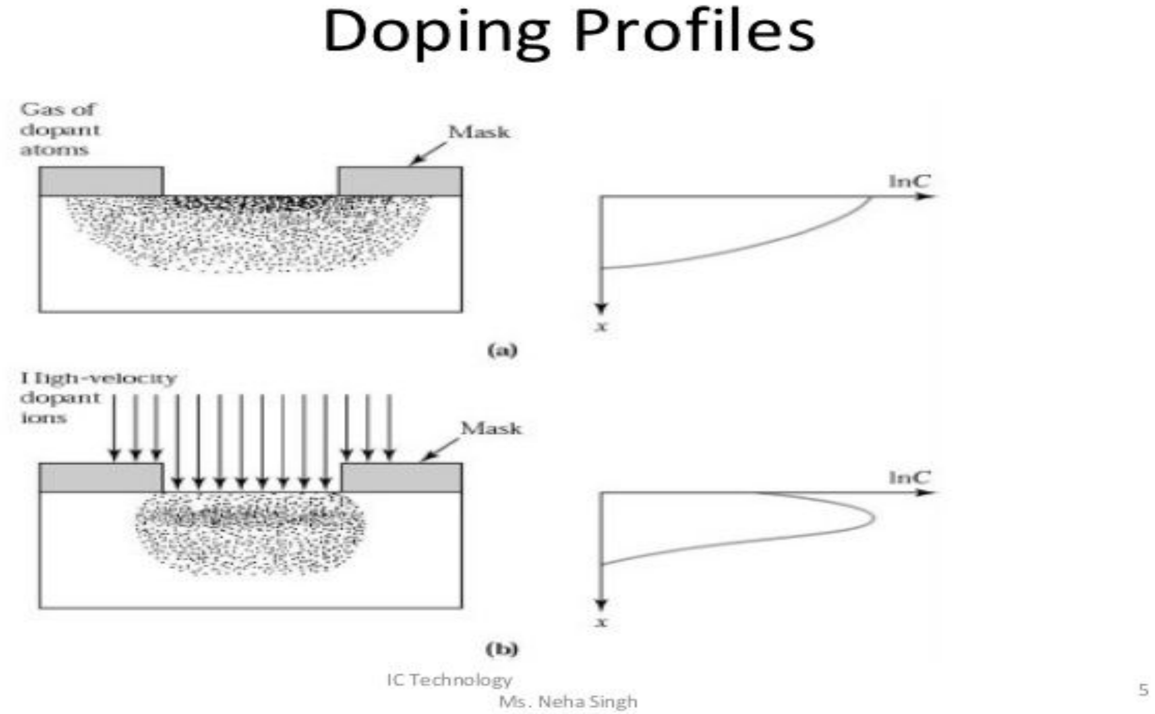
Doping Methods Comparison



Diffusion furnace

Ion implanter

Doping Methods Comparison (cont.)

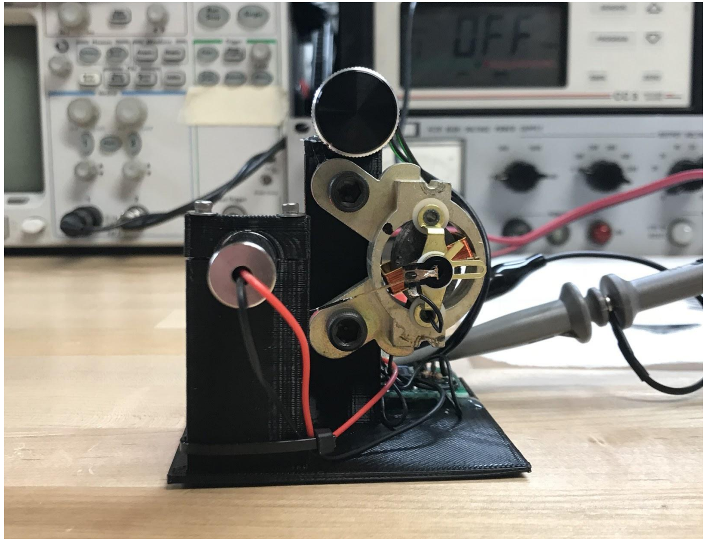


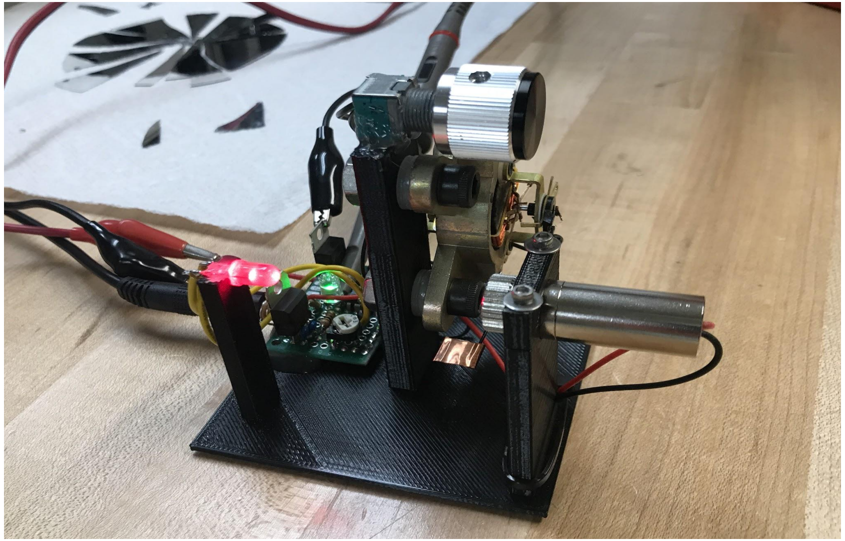
Doping Profiles

IC Technology
Ms. Neha Singh
5

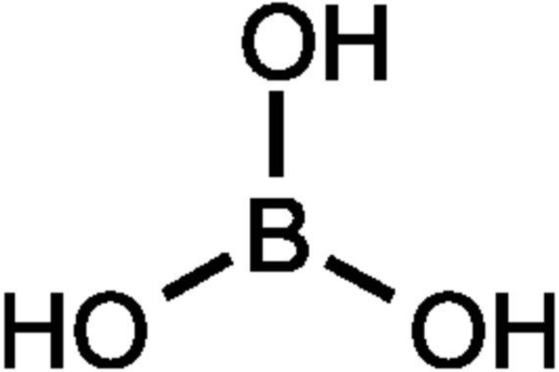
Boric Acid Solution Synthesis

- Small percentage Boric by weight (µg) in solvent is required
- Precision scales are expensive





Boric Acid Solution Synthesis (cont.)



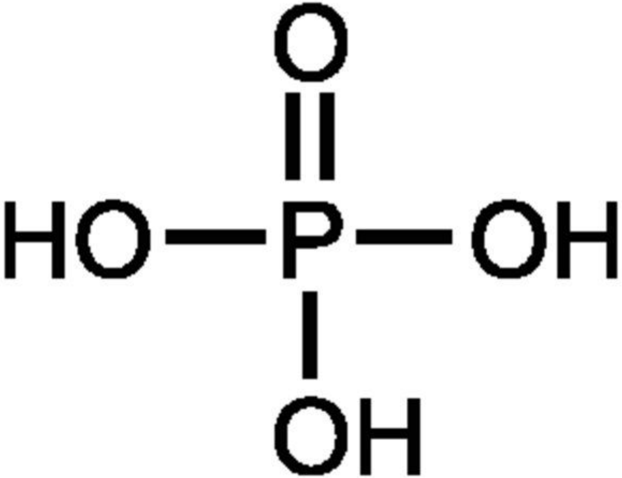
Phosphoric Acid Solution Synthesis

based on a 2,000 calorie diet.

CARBONATED WATER, HIGH FRUCTOSE CORN SYRUP AND/OR SUCROSE, CARAMEL COLOR, PHOSPHORIC ACID, NATURAL FLAVORS, CAFFEINE.

CAFFEINE CONTENT: 34 mg/12 fl oz.

2010-5517 11.27 FL OZ



Layering - Thermal Oxidation

- Silicon Dioxide (SiO_2, sand/quartz k=3.9) is dielectric that conveniently grows on Silicon
  - Native oxide ~25Å
  - Field oxide >5000Å
  - Gate oxide <<250Å
- Removed with HF (Hydrofluoric)
- Grown in tube furnace >1000˚C
  - Dry oxidation - Ambient or O_2 gas
    - Better film, less holes, slower (O_2 diffusion)
  - Wet oxidation - water vapor
    - Worse film, much faster (H_2O -> OH diffusion)

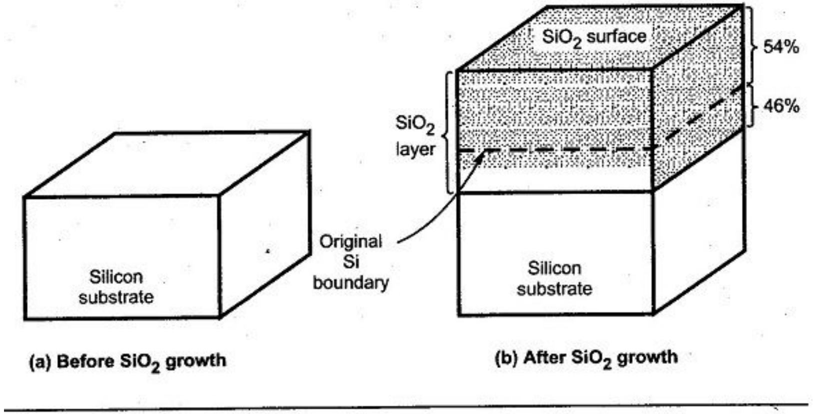
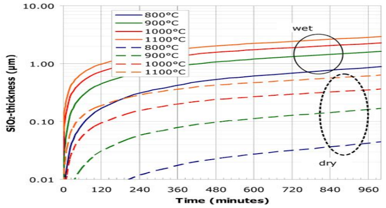
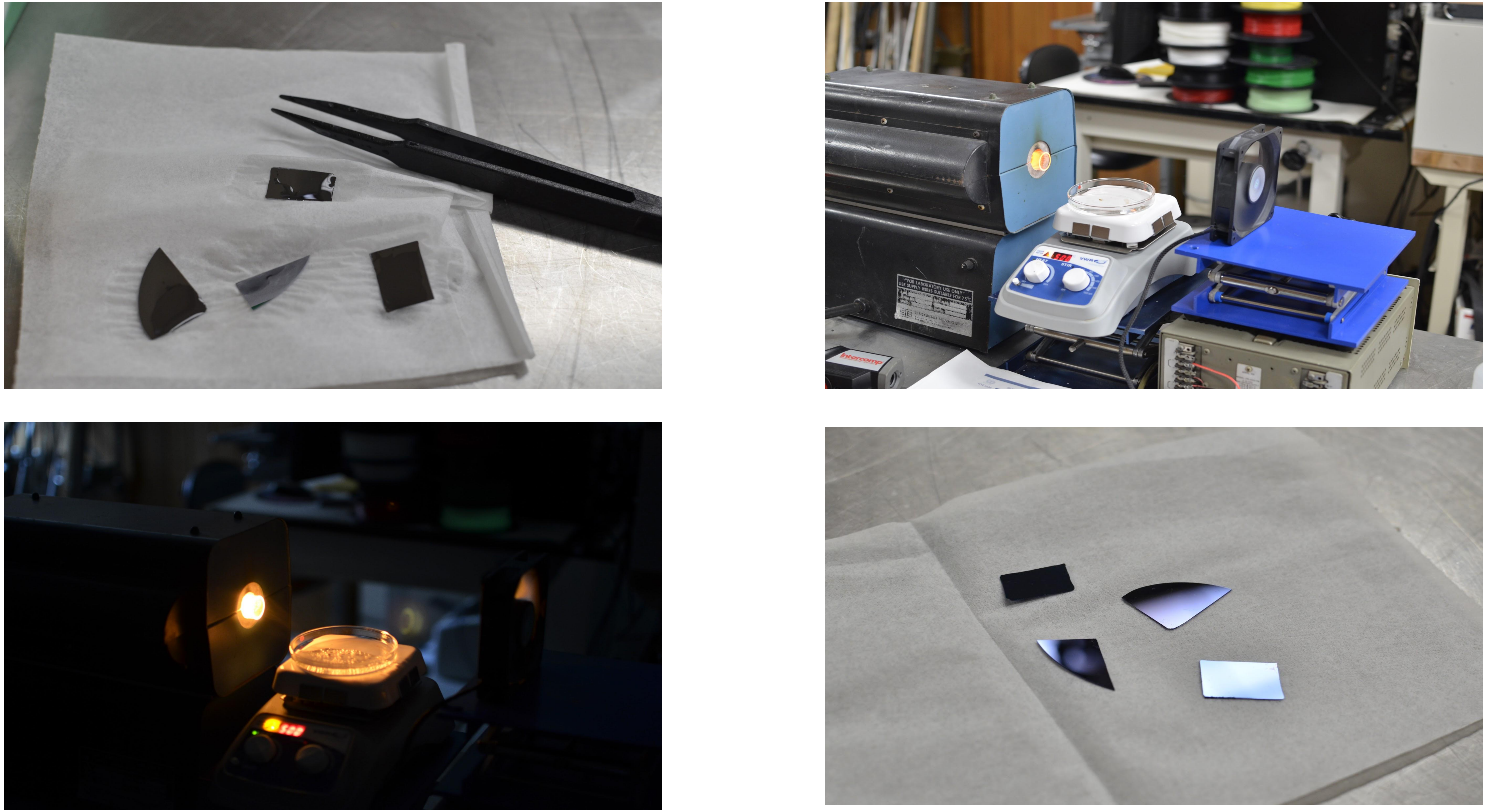


Fig. 1.4 Thermal Oxidation



Thermal Oxidation

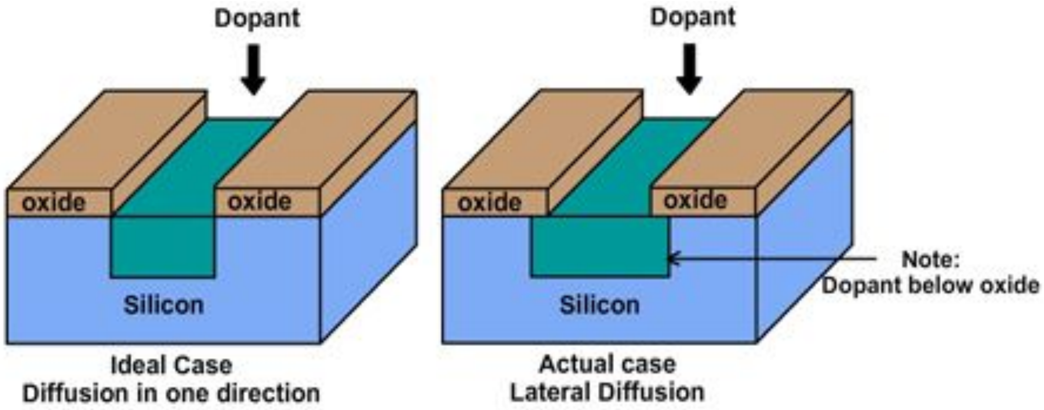


Oxide Etch - Hydrofluoric Acid

$H - F$

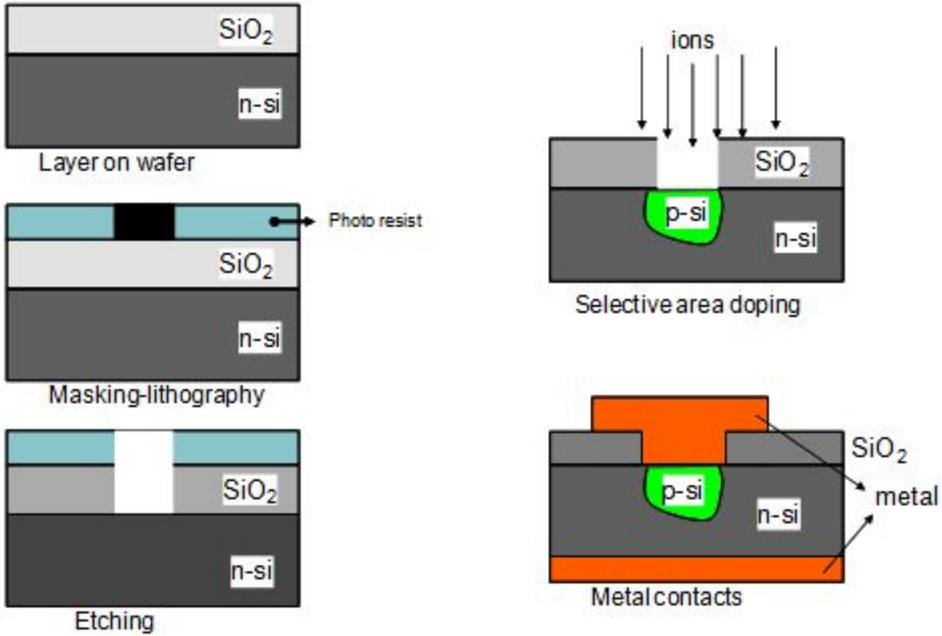
Chemistry Bench

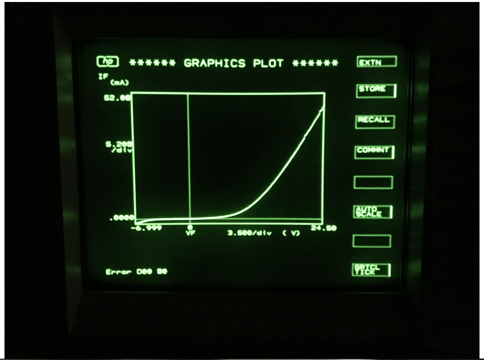
Oxide as Dopant Mask

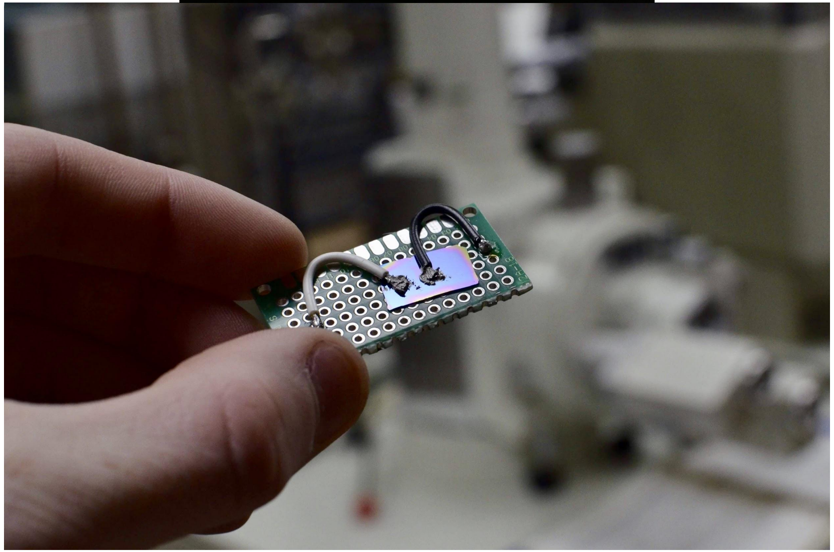


Thick oxide layers defined by photolithography are used to selectively dope regions of the device

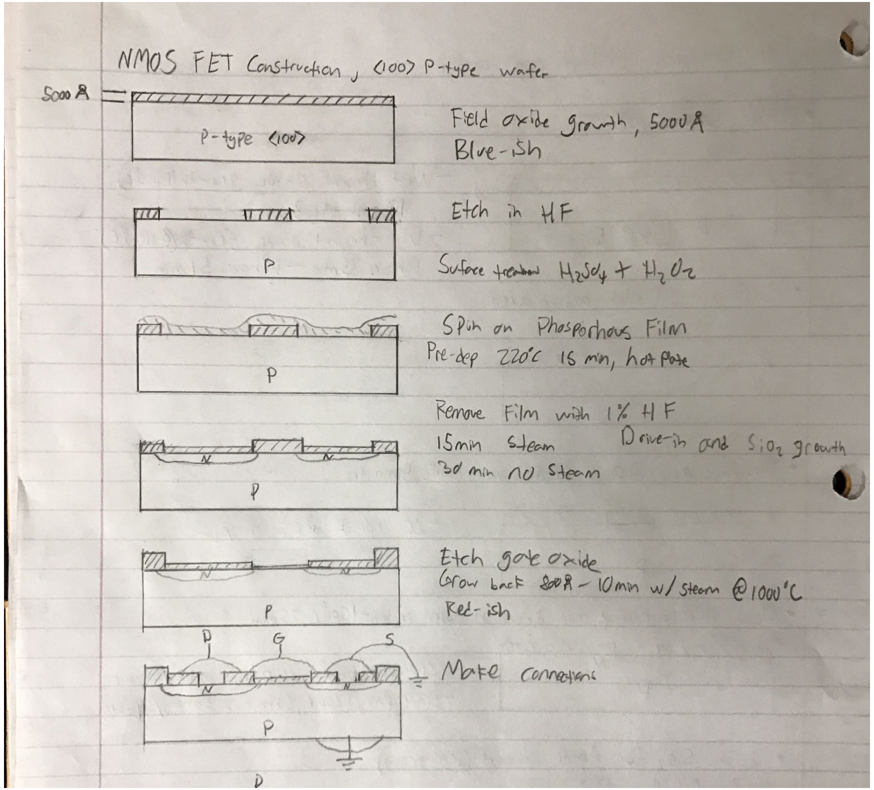
PN Junction Fabrication







FET Fabrication



NMOS FET Construction, <100> P-type wafer

Field oxide growth, 5000 Å
Blue-ish

Etch in HF

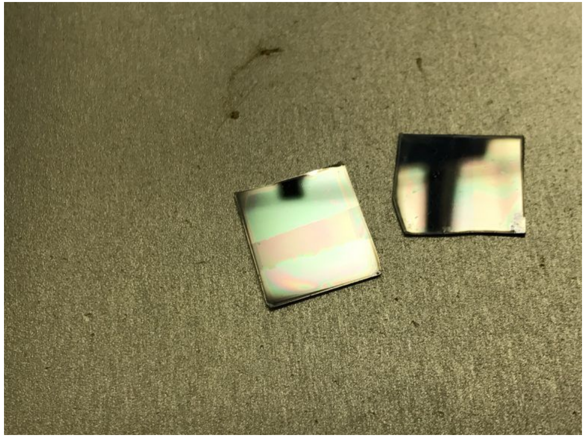
Suface treatment $H_2SO_4 + H_2O_2$

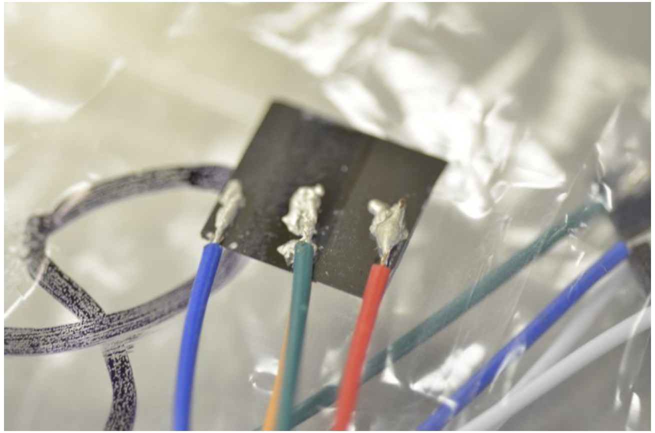
Spin on Phosporhous Film
Pre-dep 220°C 15 min, hot Plate

Remove Film with 1% HF
15min Steam
30 min no Steam
Drive-in and SiO_2 growth

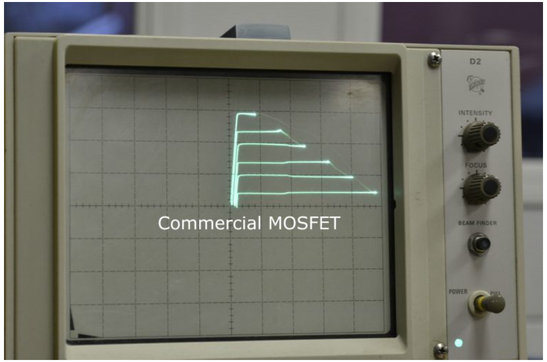
Etch gate oxide
Grow back 800Å – 10min w/ Steam @1000°C
Red-ish

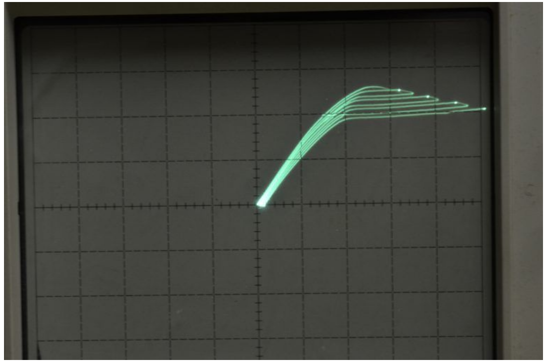
Make connections



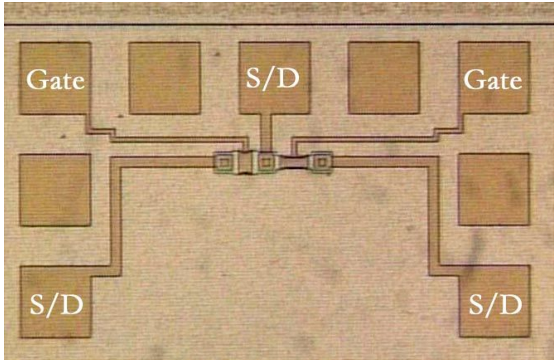


FET Fabrication (cont.)

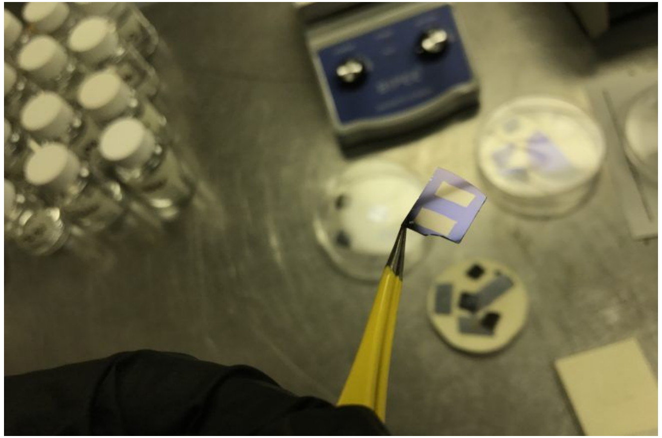




Characteristics due to dopant segregation and mobile ionic contaminants



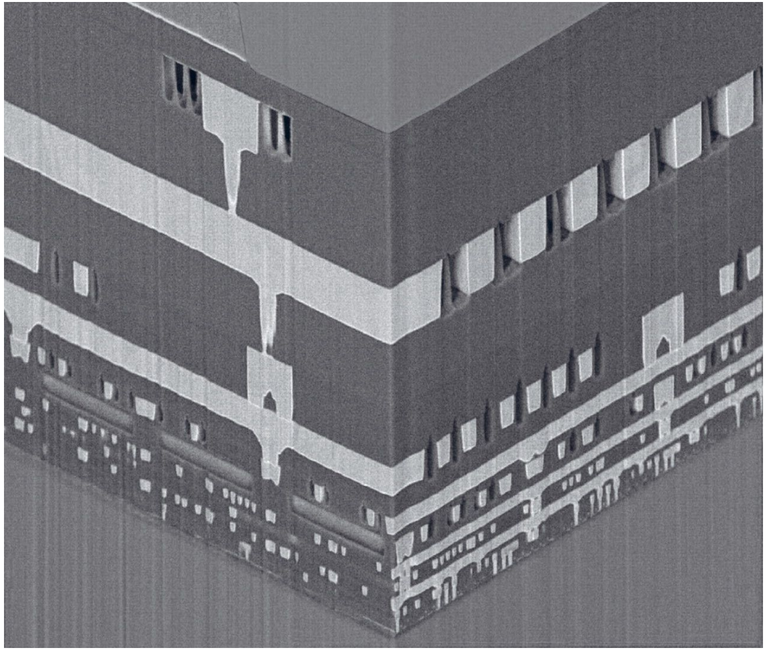
Fabricated with lithography

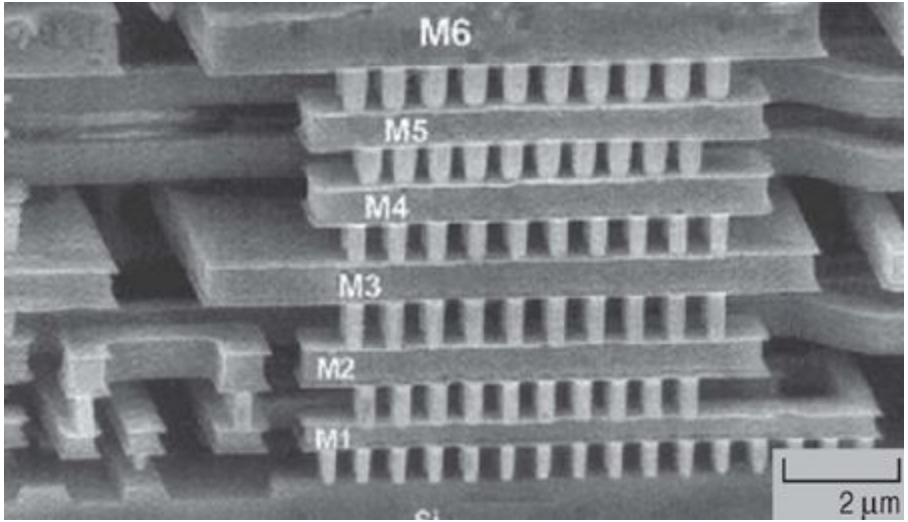


Fabricated with vinyl mask

Layering - Metalization

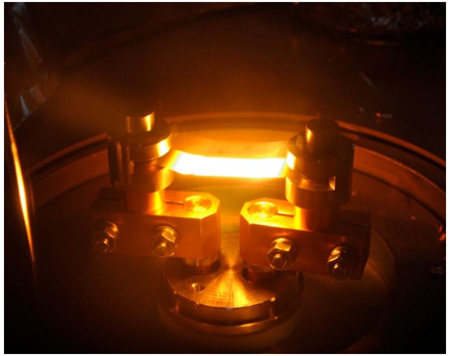
Modern ICs can have 8+ metal layers!



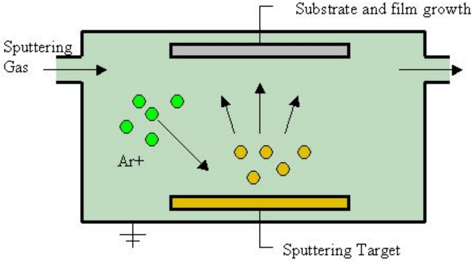


Metalization

- Thermal evaporation - source material is heated in boat until it evaporates and coats everything in the chamber
    - Fast
    - High vacuum required (1x10^{-6} Torr)
    - 1000A

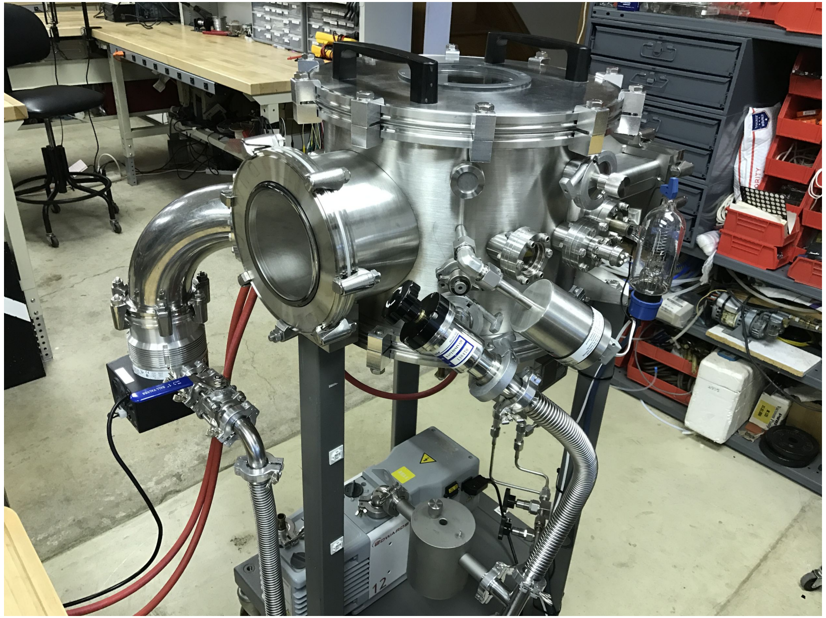


- Sputtering - high energy (plasma) ions are accelerated toward a target material and atoms are “knocked” off target and coat substrate
    - Medium vacuum required (50mTorr)
    - ~1000v



Metalization - Vacuum System

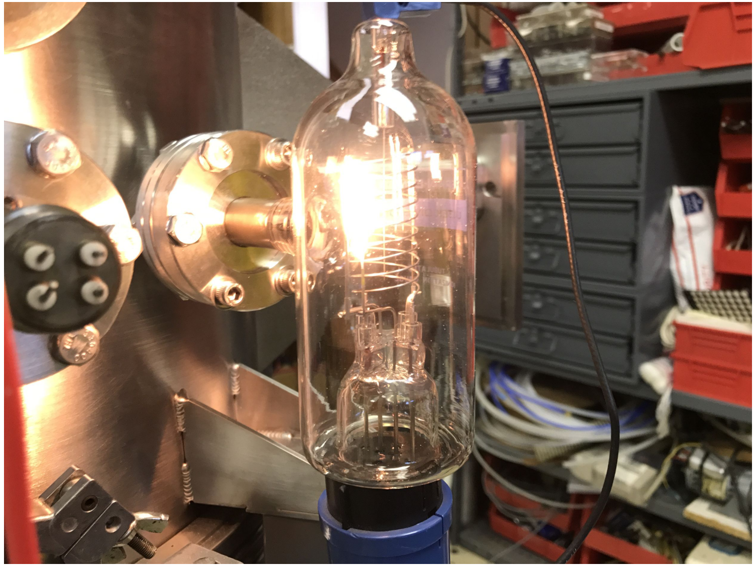
Need to be able to produce high vacuum conditions ~ $1x10^{-6}$ Torr and below so there are less gas collisions



Metalization - Vacuum System

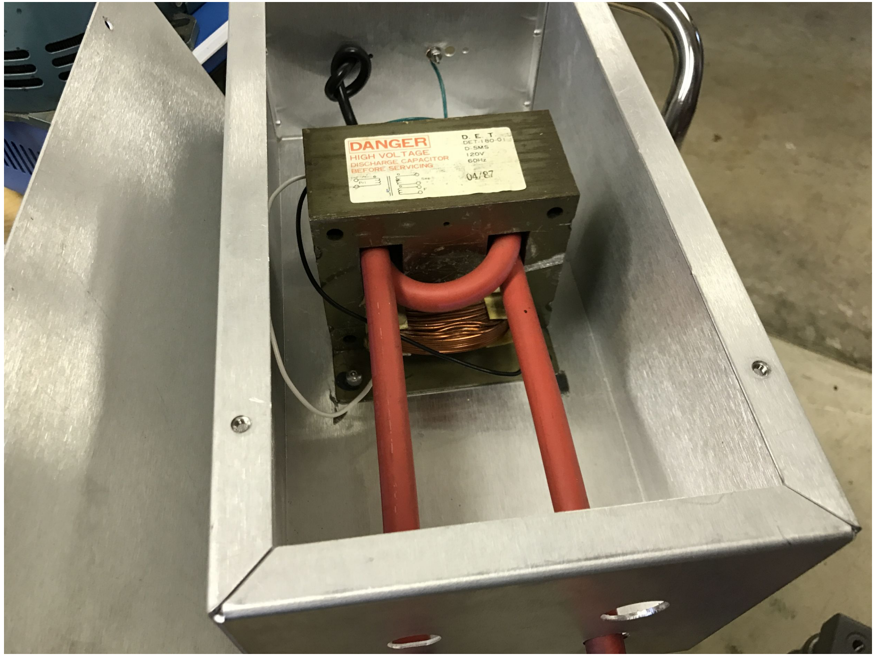
Turbomolecular pump

~48hr. pumping

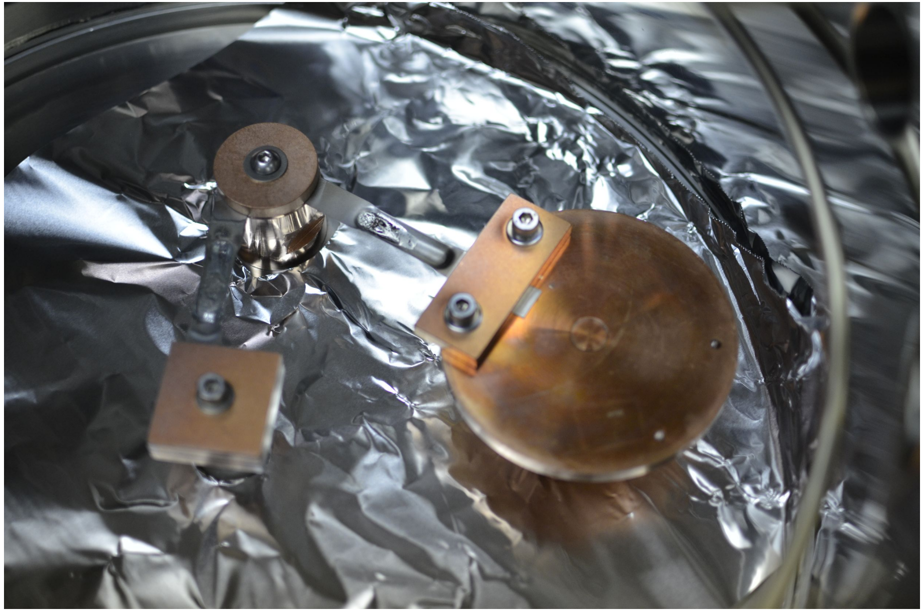


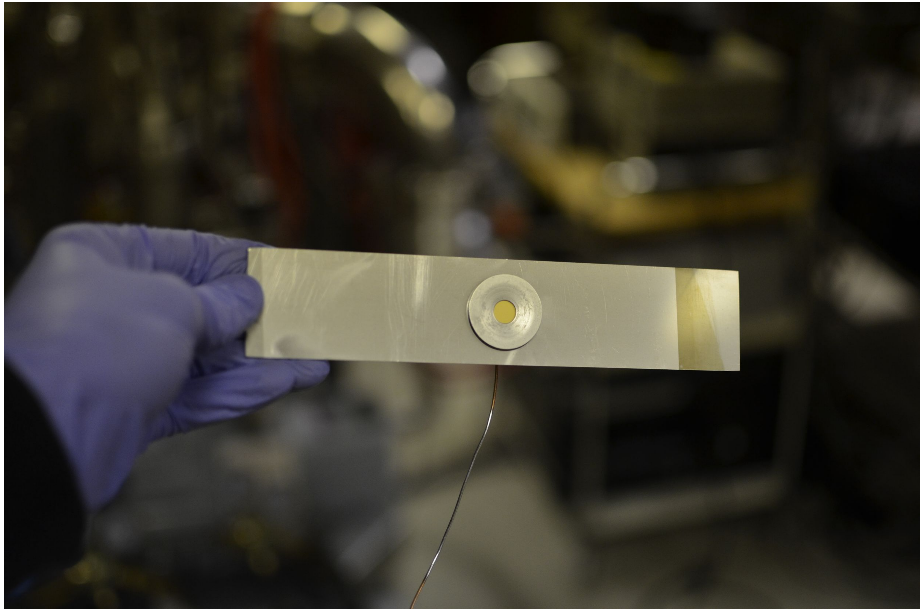
Hot cathode ionization gauge

Metalization - Thermal Evaporation

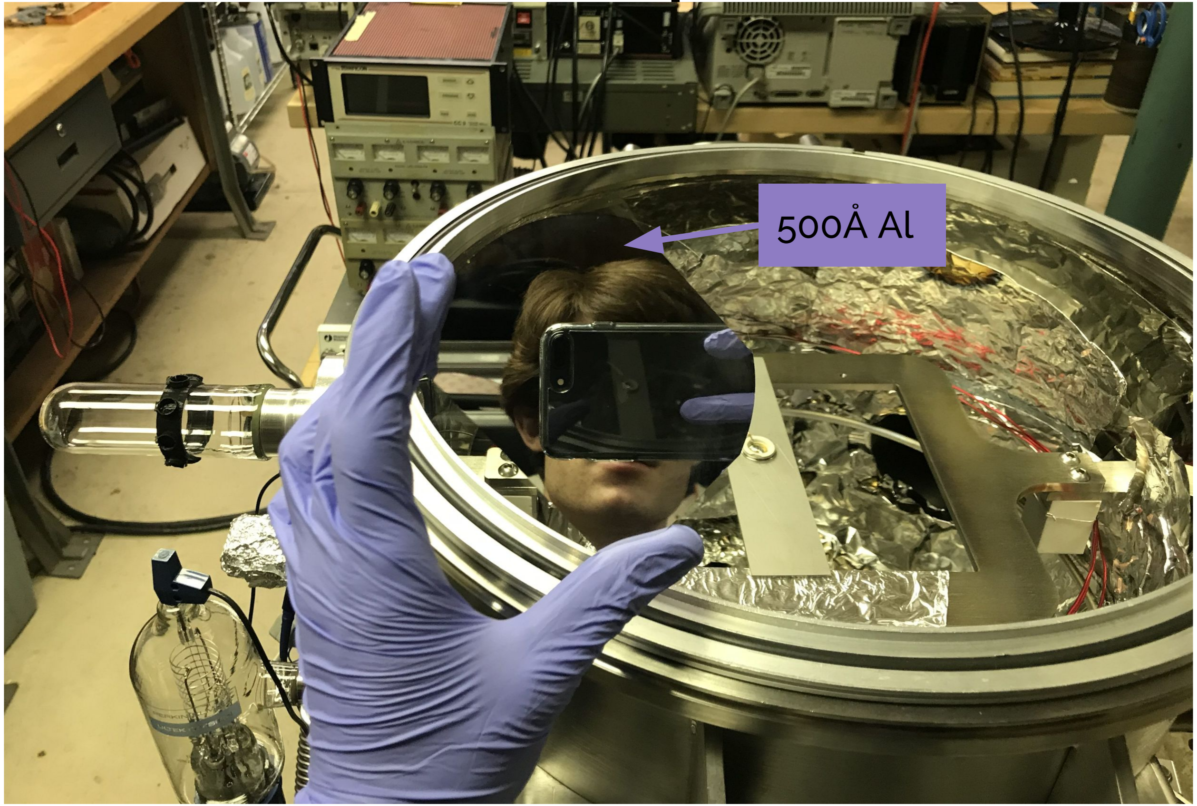


Metalization - Thermal Evaporation

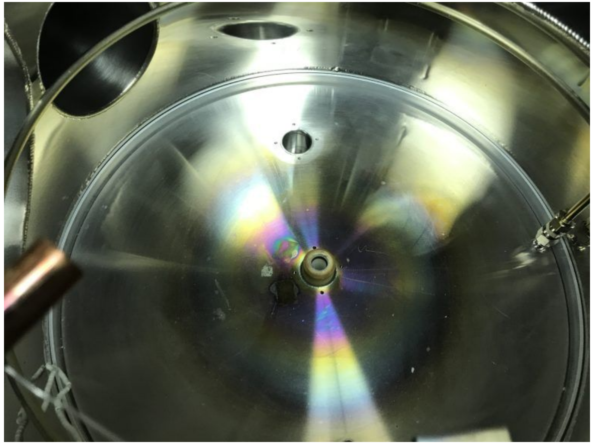




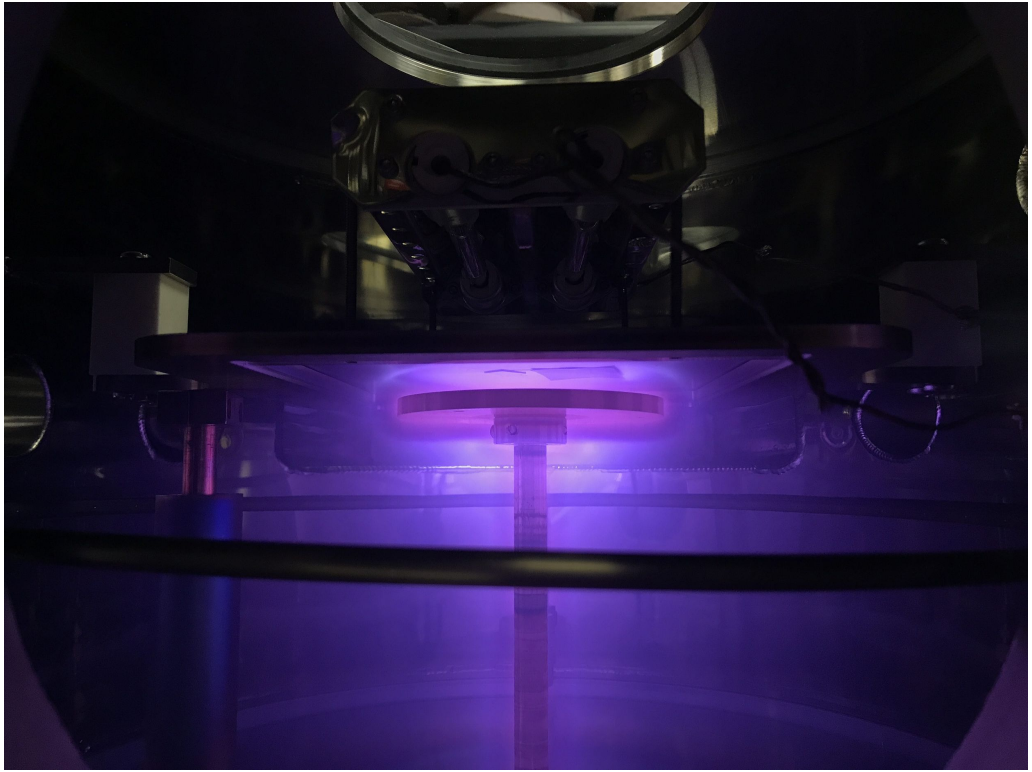
Metalization - Thermal Evaporation (cont.)

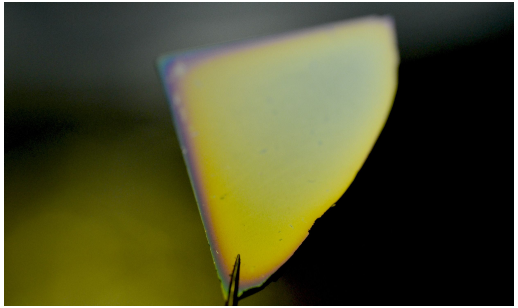


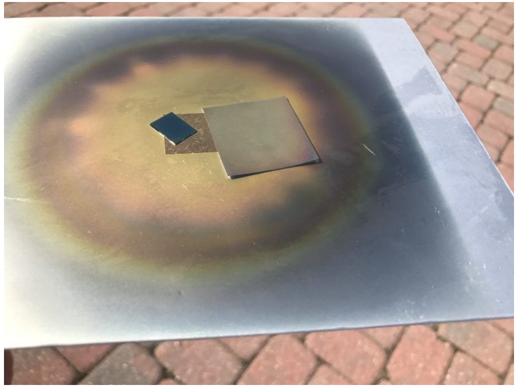
Metalization - Sputtering



Sputtering (cont.)

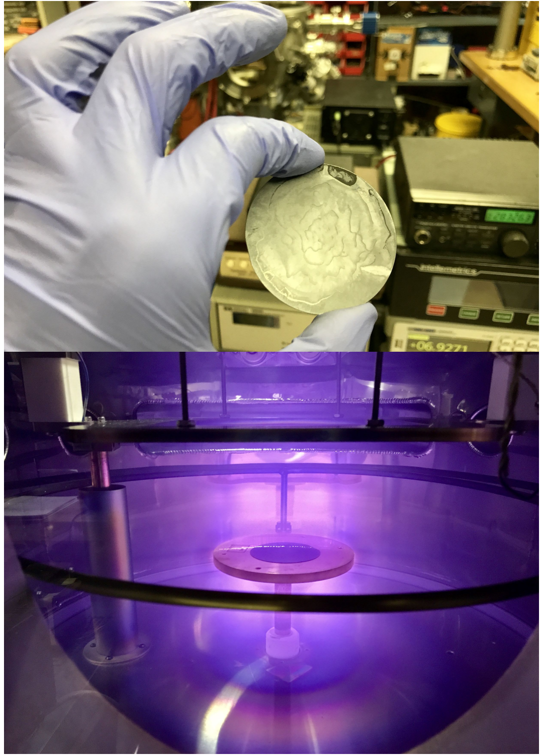




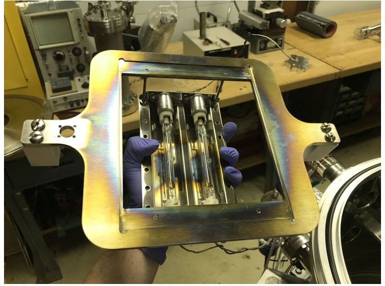


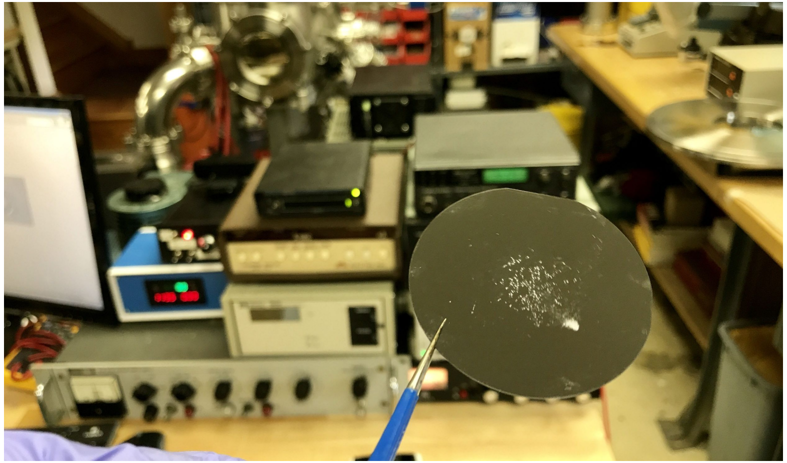
Plasma Cleaning

Same as sputtering, but lower power and typically O2 rather than Ar

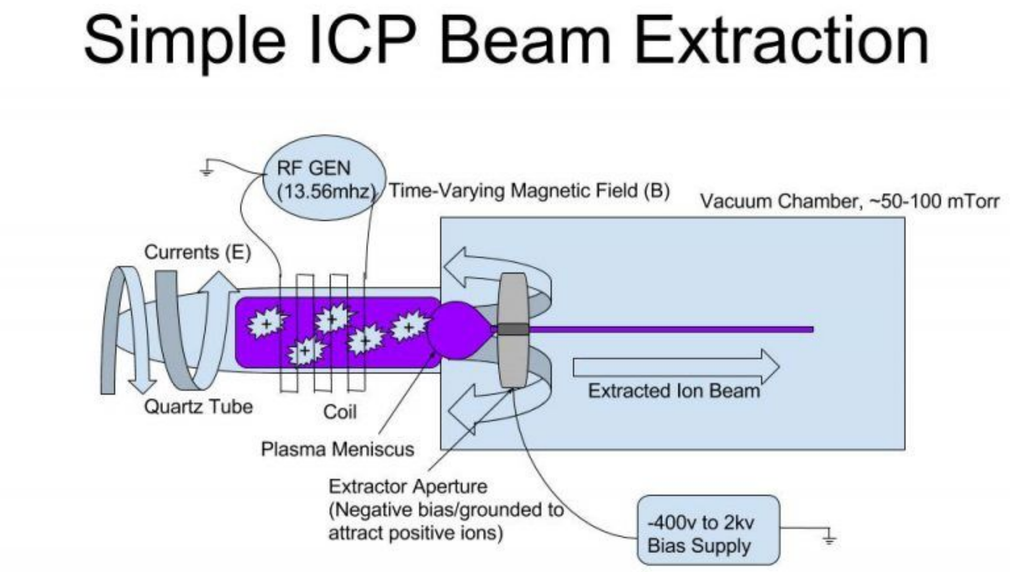


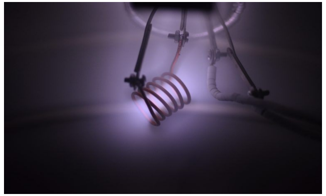
Photoresist
Ashing

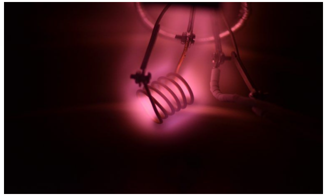


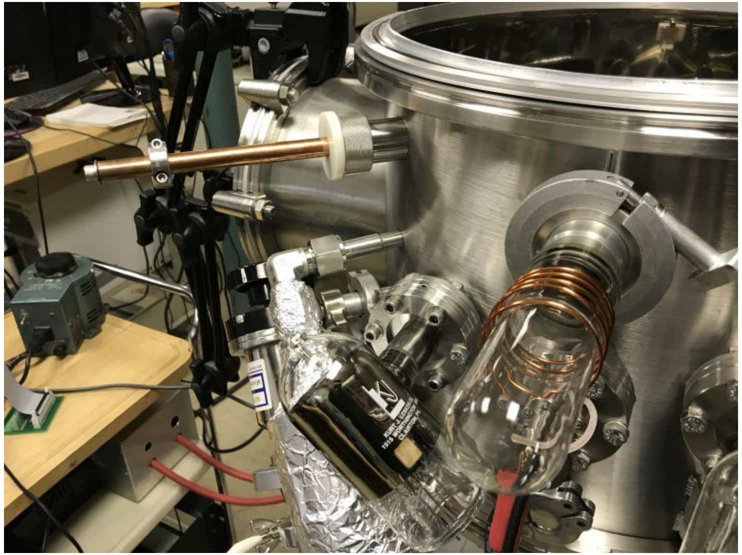


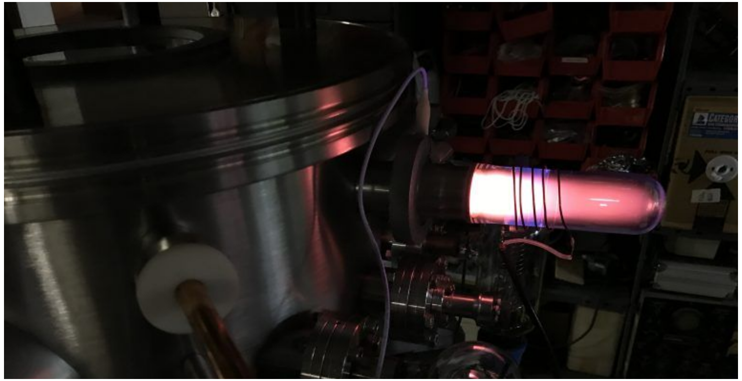
Plasma Cleaning (cont.)









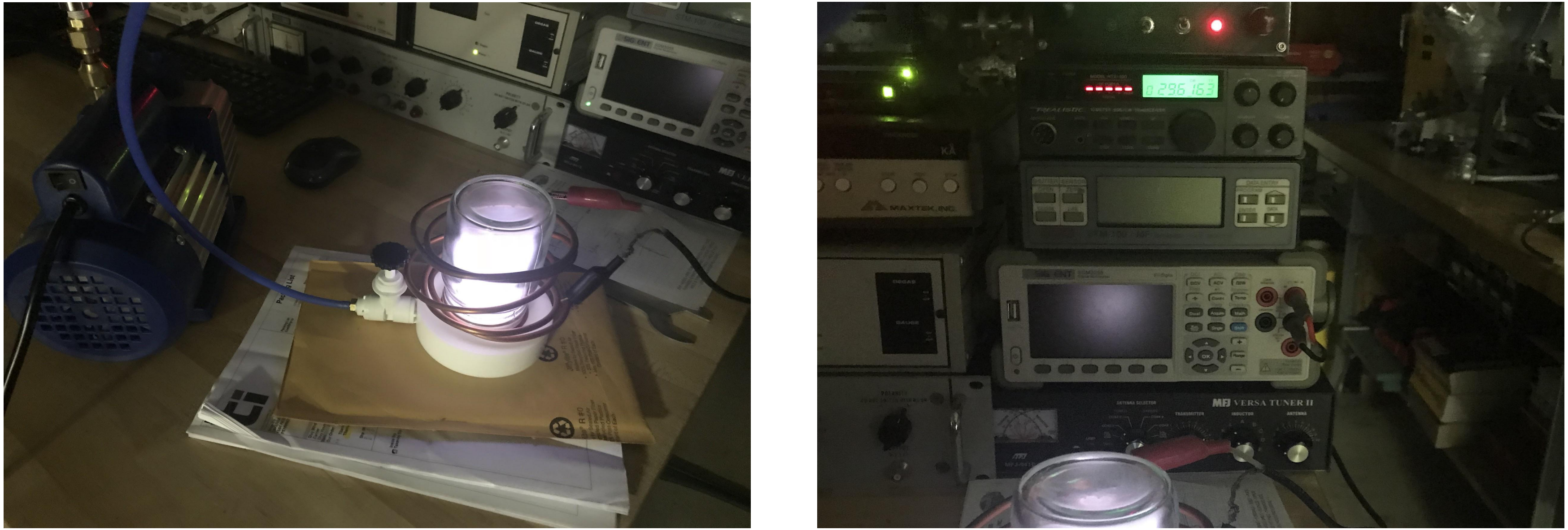


Plasma Cleaning (cont.)

Anode layer ion source

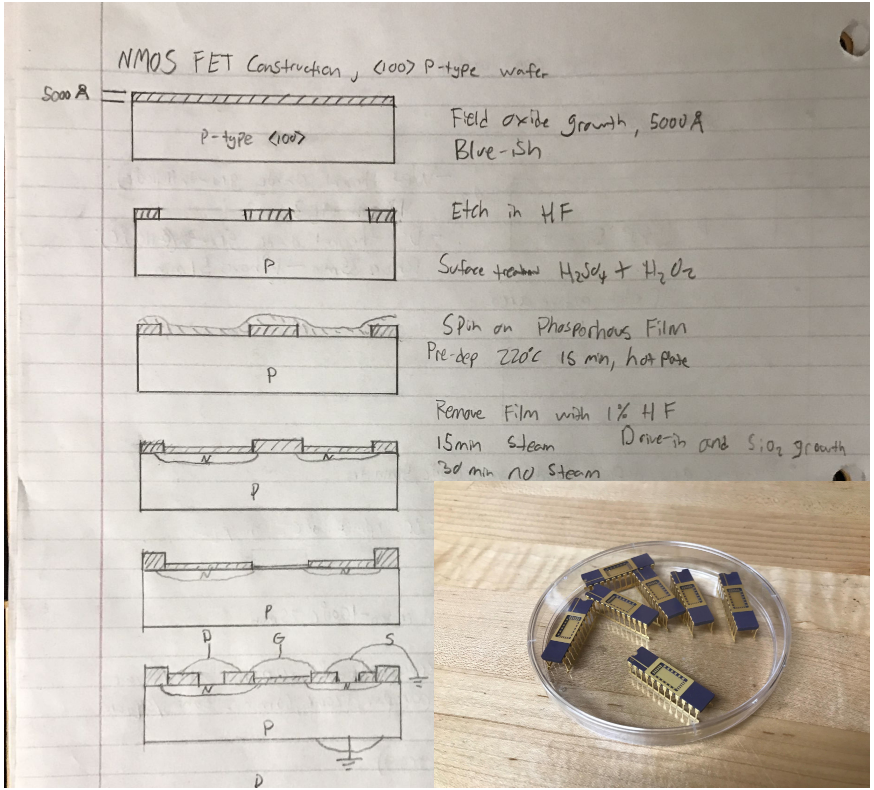
Plasma Cleaning (cont.)

Sticking with the spirit of using rust & stain remover and roach killer...



Mason jar vacuum chamber

Four Mask PMOS (1970)



NMOS FET Construction, ⟨100⟩ P-type wafer

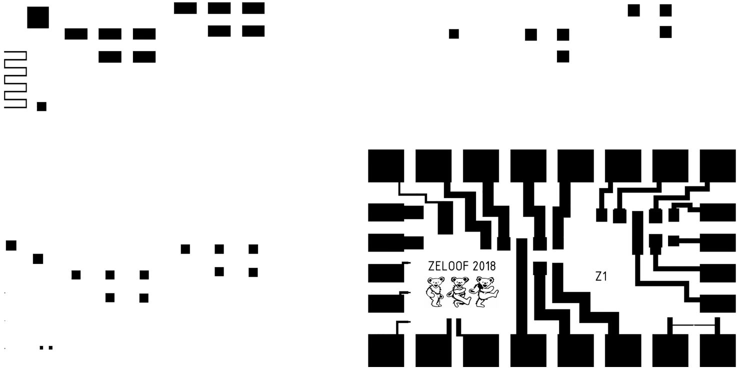
Field oxide growth, 5000 Å
Blue-ish

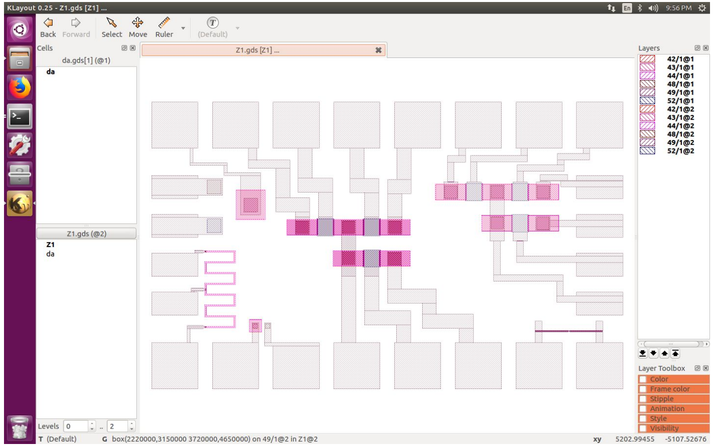
Etch in HF

Surface treatment $H_2SO_4 + H_2O_2$

Spin on Phosphorous Film
Pre-dep 220°C 15 min, hot Plate

Remove Film with 1% HF
15min Steam
30 min no Steam
Drive-in and SiO_2 growth





Levels 0 .. 2

T (Default) G box(2220000,3150000 3720000,4650000) on 49/1@2 in Z1@2 xy 5202.99455 -5107.52676

Four Mask PMOS (1970) (cont.)

Prep and Grow Field Oxide

- HF native oxide strip 5 min
- Piranha 3:1 H_2SO_4:H_2O_2 5 min
- RCA SC-1 5:1:1 H_2O:NH_3:H_2O_2 @ 80°C for 10 min
- RCA SC-2 6:1:1 H_2O:HCL:H_2O_2 @ 80°C for 10 min
- Water rinse
- HF dip
- Field oxide growth - 45 min @ 1150°C w/ water vapor, 5000Å blue

Pattern and Etch Active

- Dehydration bake - 10 min @ 160°C
- Optional spin HMDS
- Spin AZ 4210 (5510) resist 30 sec @ 3500 rpm ~3.5um (0.9um) film
- Soft bake resist 1 (1) min @ 105°C hotplate
- Expose active area 200mJ (115mJ) @ 365nm
- (If using 5510, post bake 105°C hotplate 1 min)
- Develop 1:3 400k KOH:H20 (RD6 2.8% TMAH) puddle 40 (60) sec
- Water rinse (no solvent)
- Hard bake 5 min @ 115°C hotplate
- Etch active area - HF 20 min or until surface hydrophobic @ 35°C
- Water rinse
- Resist strip - Acetone or O_2 plasma
- Acetone then IPA then water rinse

Doping

- Hydrophilic surface treatment NH_4OH/H_2O_2 or H_2SO_4/H_2O_2
- Spin dopant 30 sec @ 3500 rpm
- Pre deposition bake 10 min @ 200°C hotplate
- Diffusion 45 min @ 1200°C w/ N_2 gas flow in tube furnace
- Strip dopant film - Piranha then HF
- IPA then water rinse

Pattern and Etch Gate

- Dehydration bake - 10 min @ 160°C
- Optional spin HMDS
- Spin AZ 4210 (5510) resist 30 sec @ 3500 rpm ~3.5um (0.9um) film
- Soft bake resist 1 (1) min @ 105°C hotplate
- Expose gate window 200mJ (115mJ) @ 365nm
- (If using 5510, post bake 105°C hotplate 1 min)
- Develop 1:3 400k KOH:H20 (RD6 2.8% TMAH) puddle 40 (60) sec
- Water rinse (no solvent)
- Hard bake 5 min @ 115°C hotplate
- Etch gate - HF 20 min or until surface hydrophobic @ 35°C
- Water rinse
- Resist strip - Acetone or O_2 plasma
- Acetone then IPA then water rinse

Grow Thin Gate Oxide

- RCA SC-1 5:1:1 H_2O:NH_3:H_2O_2 @ 80°C for 10 min
- RCA SC-2 6:1:1 H_2O:HCL:H_2O_2 @ 80°C for 10 min
- Water rinse
- Grow gate oxide - 750Å - 2.5 min wet / 45 min dry @ 1150°C
- Acetone then IPA then water rinse

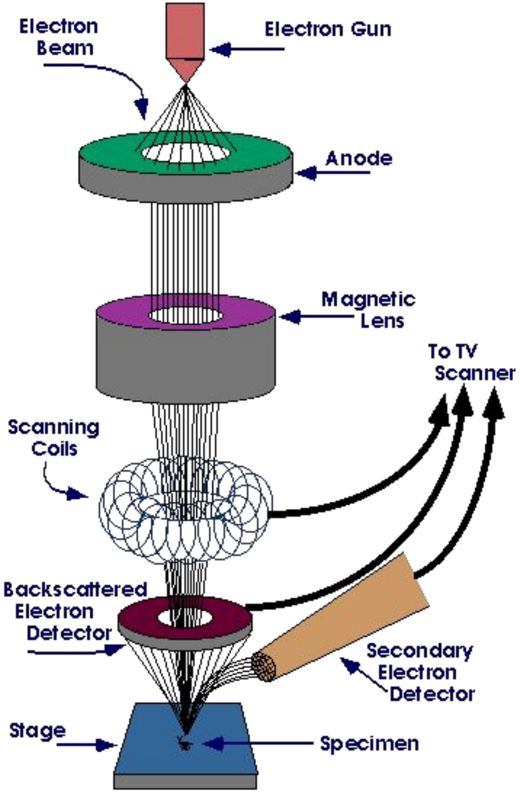
Pattern and Etch Contact

- Dehydration bake - 10 min @ 160°C
- Optional spin HMDS
- Spin AZ 4210 (5510) resist 30 sec @ 3500 rpm ~3.5um (0.9um) film
- Soft bake resist 1 (1) min @ 105°C hotplate
- Expose contact 200mJ (115mJ) @ 365nm
- (If using 5510, post bake 105°C hotplate 1 min)
- Develop 1:3 400k KOH:H20 (RD6 2.8% TMAH) puddle 40 (60) sec
- Water rinse (no solvent)
- Hard bake 5 min @ 115°C hotplate
- Etch contact - HF 20 min or until surface hydrophobic @ 35°C
- Water rinse
- Resist strip - Acetone
- Acetone then IPA then water rinse

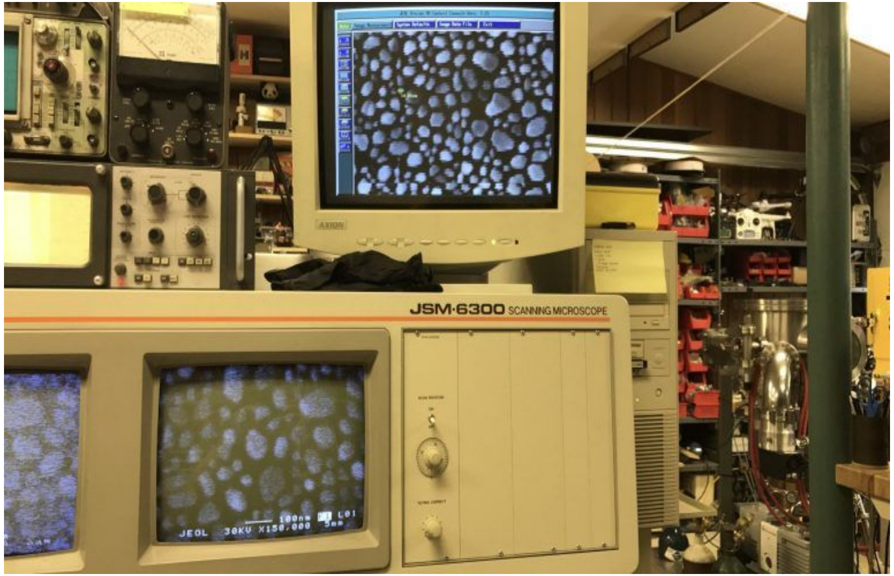
Deposit, Pattern, and Etch Metal

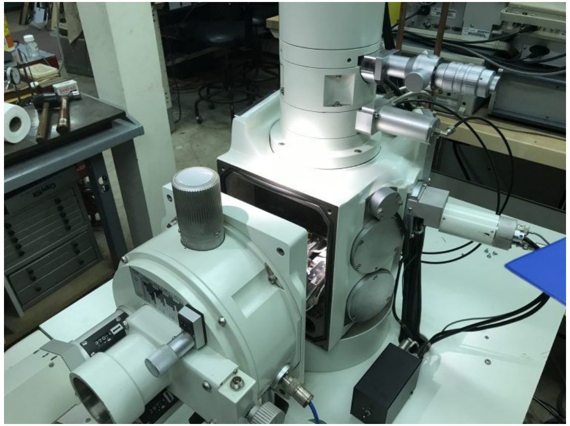
- Deposit metal - Al evaporation 3000Å
- Dehydration bake - 10 min @ 160°C
- Optional spin HMDS
- Spin AZ 4210 (5510) resist 30 sec @ 3500 rpm ~3.5um (0.9um) film
- Soft bake resist 1 (1) min @ 105°C hotplate
- Expose gate window 200mJ (115mJ) @ 365nm
- (If using 5510, post bake 105°C hotplate 1 min)
- Develop 1:3 400k KOH:H20 (RD6 2.8% TMAH) puddle 40 (60) sec
- Water rinse (no solvent)
- Hard bake 5 min @ 115°C hotplate
- Etch metal layer - H_3PO_4 5 min @ 40°C
- Water rinse
- Resist strip - Acetone
- Acetone then IPA then water rinse
- Anneal Al 10 min @ 475°C in H_2

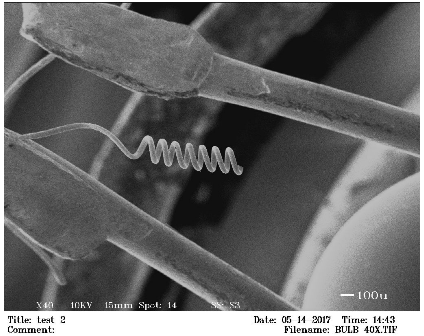
Scanning Electron Microscope



Scanning Electron Microscope (cont.)







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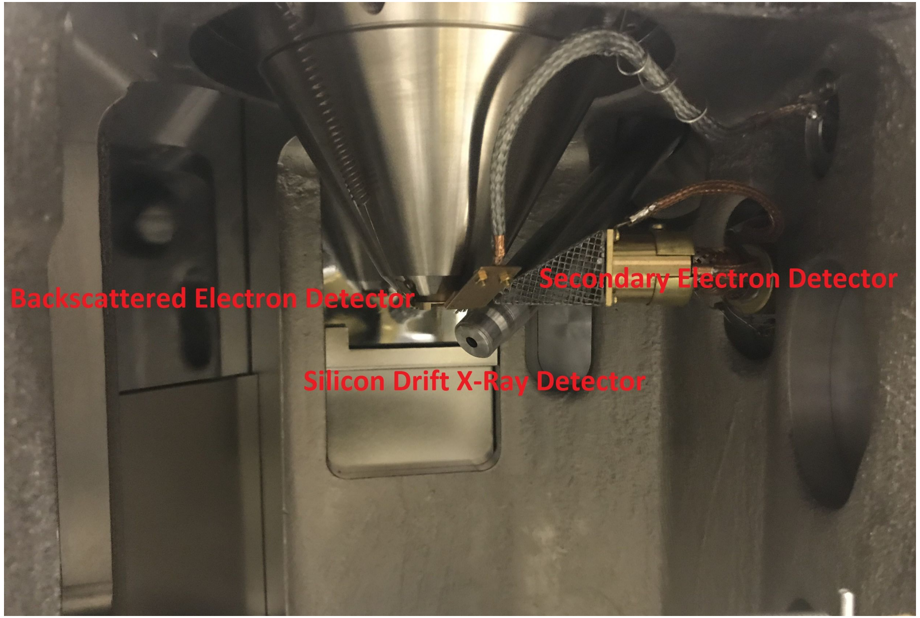

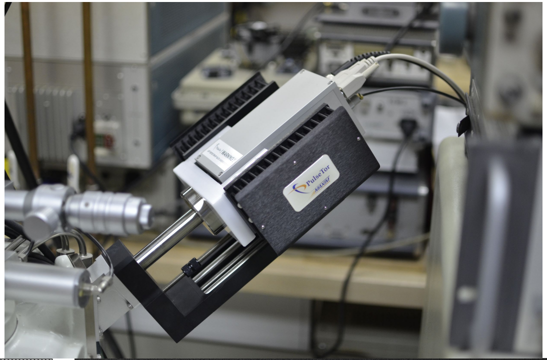

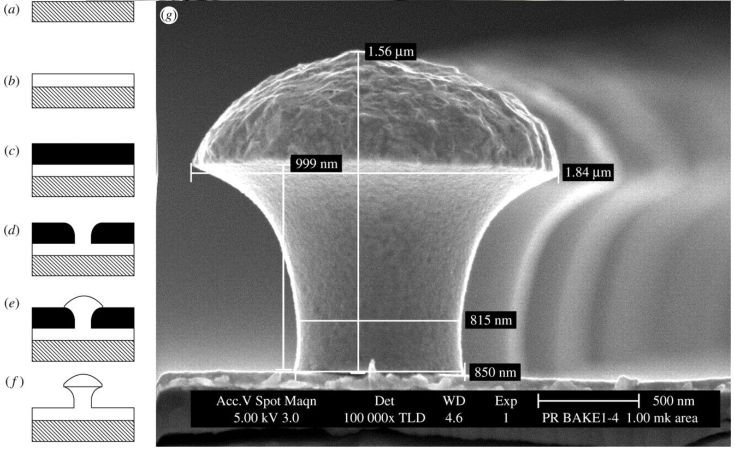

Scanning Electron Microscope (cont.)

Questions & Contact Info

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