Tunable High-Q N-Path Band-Pass Filters: Modeling and Verification

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***Abstract* — In this paper a differential single-port switched-RC N-path filter with band-pass characteristic is proposed. The switching frequency defines the center frequency, while the RC-time defines the bandwidth. This allows for high-Q highly tunable filters which can for instance be useful for cognitive radio. Using a linear periodically time-variant (LPTV) model, exact expressions for the filter transfer function are derived. The behavior of the circuit including non-idealities such as maximum rejection, spectral aliasing, noise and effects due to mismatch in the paths is modeled and verified via measurements. A simple RLC equivalent circuit is provided modeling bandwidth, quality factor and insertion loss of the filter. A 4-path architecture is realized in 65nm CMOS. An off-chip transformer acts as a balun, improves filter-Q and realizes impedance matching. The differential architecture reduces clock-leakage and suppresses selectivity around even harmonics of the clock. The filter has a constant -3dB bandwidth of 35MHz and can be tuned from 100MHz up to 1GHz. Over the whole band IIP3 is better than 14dBm, P_{1dB}=2dBm and NF<5.5dB,while the power dissipation increases from 2mW to 16mW (only clocking power).**

Index Terms — N-path filter, tunable filter, high linearity, Linear Periodically Time Variant circuit, commutated capacitors, CMOS bandpass filter, inductorless, cognitive radio, software-defined radio.

I. INTRODUCTION

In software defined radio (SDR) and cognitive radio transceivers, programmability is not only desired in the digital back-end, but also for analog front-end functions. A major challenge for such radios is the realization of an RF band-pass filter, with tunable center frequency over a wide frequency span. For cognitive radio applications in the TV-bands, relatively few and rather narrow spectral holes may exist between strong incumbent TV transmitter signals [1]. To reject the strong signals in order to avoid blocking of the receiver, such a filter should have very high linearity, high compression point but also very high Q (e.g. Q=50 for 10MHz bandwidth around 500MHz).

Although off-chip passive filters provide these properties, integrated CMOS alternatives are highly desired for reasons of size and cost. On-chip LC filters can be implemented but with limited tuning range and low Q, especially below 1 GHz where the achievable Q of on-chip inductors is poor and coils take large area. Q-enhanced techniques [2]-[4] can improve filter quality factor but degrade linearity and noise. Thus alternative tunable filters without inductors are highly wanted.

Inductor-less tunable filters based on periodically time variant networks have been addressed in literature under different names such as N-path filters, sampled data filters, commutated capacitors, etc. [4]-[10]. Discrete-time switched capacitor N-path filters are probably best known [8], but here we focus on their continuous time predecessors. Fig. 1 shows a block diagram of an N-path filter composed of N identical linear time-invariant (LTI) networks with impulse response h(t) and 2N frequency mixers (modulators), driven by time/phase shifted versions of the clock p(t) and q(t). The time shift between two successive paths is T/N, where T is the period of the modulating signal. If the LTI networks exhibit a lowpass characteristic around DC, the mixing results in a band-pass around the mixing frequency. Simply put, the input signal is downconverted to the baseband, filtered by the LTI network and then up-converted again to the original band of V_{in}. The center frequency is determined by the mixing frequency, insensitive to filter component values. A high mixing frequency combined with a narrow low-pass filter bandwidth allows for a very high filter-Q.

While time-continuous N-path filters have been proposed for kHz operating frequencies in the 60's [6], they seem to have been largely forgotten until recently. CMOS technology now allows N-path filters to work at TV-band RF frequencies [9], [10] and even above 1GHz [11]. In [9] an

8-path single-ended structure is used, and in [10] we proposed a differential 4-path filter combined with a broadband off-chip transformer. In [11] differential 4-path filters are applied in a quad-band SAW-less receiver. This paper aims to model and verify N-path filter performance. Using linear periodically time-variant (LPTV) analysis, exact expressions for the frequency response of differential N-path filters are derived. In [6] state-space analysis was used to derive the steady state and transient response for a single-ended N-path filter, which is however not directly applicable to our differential architecture. We will derive one set of equations that characterizes filtering but also possible imperfections like harmonic folding, noise and the effects of the clock phase imbalance and mismatch. Moreover, an equivalent RLC tank circuit will be derived to approximate N-path filter behavior around the center frequency. Finally, we will verify the model via extended experimental results compared to [10].

In section II we will derive the differential N-path filter architecture starting from Fig. 1 and then analyze its transfer function in section III. Section IV presents basic characteristics of the differential N-path filter. Its chip implementation is discussed in section V and section VI covers the measurement and verification versus the model.

II. N-Path Filter

We will now derive the differential N-path filter from Fig. 1, where we aim for a high-linearity implementation using MOS-switches as passive mixers and RC low-pass filters (see Fig. 2a). Furthermore we will try to develop some intuitive understanding of the filter behavior.

A. Single Ended Switched RC N-Path Filter

Fig. 2c shows a multi-phase clocking scheme for the switches with non-overlapping on-times. Thus no charge exchange between capacitors can occur. For this reason and since a resistor is a memory-less element, it can be shared by all paths and shifted in front of them (Fig. 2b). Moreover, if the clocks for the first and second set of switches are identical, the first set can also implement the function of the second set. V_{out} becomes then available between the shared resistor and switches. Fig. 2b shows the resulting single-port single-ended N-path filter (V_{out} is both input and output). If we use the capacitor voltages as outputs, the circuit behaves as a highly linear multiphase passive mixer [12], [13].

To intuitively understand the filter behavior of Fig. 2b it is useful to see it as a two-step process: 1) the input signal experiences downconversion and low-pass filtering passing through the switches to the capacitors side; 2) the same switches up-convert the filtered capacitor voltage

to the output node. Another way to understand the filtering is to realize that at any moment one and only one capacitor is connected to the output node. If we assume that time constant $RC>>T_S/N$, the output voltage will be the average of the input voltage V_{in} over the time that the capacitor "looks at V_{in}". If the frequency of V_{in} is equal to the switching frequency, each capacitor will observe the same part of the input waveform during every period. As each capacitor sees another part, the result is a staircase approximation of V_{in}, see Fig. 2d (4-path example). In fact, the capacitors experience steady DC voltage and conduct in first order approximation no current. If the input frequency deviates from the clock frequency the signal portion seen by a capacitor will "travel over the period" and the capacitors experience an AC voltage (with $f = \Delta f$) thus they conduct current while switches are on and the average voltages on the capacitors is closer to zero. Consequently signals at input frequencies below or above the switching frequency will be suppressed with an amount depending on the offset from the switching frequency.

B. Differential Switched RC N-Path Filter

If we repeat the analysis for input signals around harmonics of the clock frequency, we also find non-zero average values. This fits to the comb-like characteristic of N-path filters [4], i.e. its repetitive selectivity around harmonics of the switching frequency. The differential architecture of Fig. 3 aims to cancel even harmonic responses. Each path is differential-in and differential-out, but contains one grounded capacitor connected to two anti-phase driven switches. A 4-phase 25%-duty-cycle clock provides all required clocks (see Fig. 3). Now, for input signals around even harmonics of the clock frequency, no net charge is stored on the capacitors in steady state and no upconverted signal appears at the output.

III. ANALYSIS

To model the behavior of the N-path filter quantitatively, we will now apply LPTV state space analysis [14], [15] to derive the exact shape of the transfer function of differential N-path filter.

A. State Space Analysis of LPTV circuits

For an LPTV network which is periodic with the frequency $f_S = 1/T_S$ the output spectrum is related to the input spectrum as [16]:

$$V_{out}(f) = \sum_{-\infty}^{\infty} H_n(f) V_{in}(f - nf_S) \tag{1}$$

Where $V_{in}(f - nf_S)$ represents the shifted version of the input spectrum to account for frequency translation (mixing), while $H_n(f)$ describes the spectral shaping (filtering) properties of an LPTV network. To simplify analysis, we make two assumptions: (1) The off-impedance of the switches is infinite and the on-impedance is zero. (2) The switching is instantaneous.

The time interval $nT_S < t < nT_S + T_S$ is divided into M portions (M is the number of the states), and each portion identified by k can be represented as $nT_S + \sigma_k < t < nT_S + \sigma_{k+1}$, k=0,…, M and $\sigma_0 = 0$ (see Fig. 4). During each interval there is no change in the state of the switches and the network turns to an LTI system. The state equations for interval k can be written as:

$$\begin{aligned} \dot{x}_k(t) &= A_k x_k(t) + B_K u(t) \\ y(t) &= C_k x_k(t) + D_k u(t) \end{aligned} \tag{2}$$

Where $u(t)$ is the input vector, $x_k(t)$ the state vector and $y(t)$ is the output vector. If we define $u_k(t)$ and $y_k(t)$ to be equal to the input $u(t)$ and output $y(t)$ respectively during the k-th interval, and zero otherwise, the state equations in (2) can be reformulated as [14]:

$$\begin{aligned} \dot{x}_k(t) &= A_k x_k(t) + B_K u_k(t) \\ &\quad + \sum_{n=-\infty}^{\infty} x_k(nT_S + \sigma_k)\delta(t - nT_S - \sigma_k) - x_k(nT_S + \sigma_{k+1})\delta(t - nT_S - \sigma_{k+1}) \\ y_k(t) &= C_k x_k(t) + D_k u_k(t) \end{aligned} \tag{3}$$

In (3) the Dirac's delta function $\delta(t)$ has been used to add the effects of the initial conditions to the equations at the beginning of an interval, while subtracting it at the interval's end. Then the output $y(t)$ is the sum of all responses from M states in the system:

$$y(t) = \sum_{k=1}^{M} y_k(t) \tag{4}$$

Since we are interested in the spectrum of the output of the system we need to take the Fourier transform from (4). It can be shown [14] that if we apply a complex exponential $u_{in}(t) = Ae^{j2\pi ft}$ as input, the output state at discrete moments can be calculated by reforming the state equations to a set of difference equations at the switching moments, and the output will be of the form:

$$x_k(nT_S + \sigma_k) = G_k(f) A e^{j2\pi ft} \delta(t - nT_S - \sigma_k) \tag{5}$$

The input spectrum can be represented as a summation of sinusoidal signals. As a result the frequency response of the system at discrete transition moments takes the form:

$$x_k(nT_S+\sigma_k)=G_k(f)u_i(t)\delta(t-nT_S-\sigma_k) \tag{6}$$

By applying (5) to (3) and taking the Fourier transform, the spectrum of the state vector becomes:

$$X_k(f)=\sum_{n=-\infty}^{\infty}H_{n,k}(f)u_i(f-nf_S)$$

$$H_{n,k}(f)=\left(j2\pi fI-A_k\right)^{-1}\left(\begin{array}{l}B_k\dfrac{1-\exp(-j2\pi nf_S\tau_k)}{j2\pi n}\exp(-j2\pi nf_S\sigma_{k-1})\\+f_SG_{k-1}(f-nf_S)\exp(-j2\pi nf_S\sigma_{k-1})-f_SG_k(f-nf_S)\exp(-j2\pi nf_S\sigma_k)\end{array}\right) \tag{7}$$

Where τ_k is the length of k-th time interval (see Fig. 4) and I is an identity matrix.

B. Analysis of the Differential Single Port N-path Filter

We will apply the analysis procedure described in the previous part to derive the output spectrum of the differential N-path filter. Although Fig. 3 illustrates a 4-path architecture, analysis is done for a general differential N-path system. At any moment two capacitors are connected to the differential output through two switches, which are activated with the same phase of the input clock. The resulting time domain signal is the superposition of the signals from different capacitors at different moments without any overlap. Since there is no interaction between capacitor voltages, the analysis of the simple network illustrated in Fig. 5 suffices, where just one path is illustrated with its timing diagram for the switches. The state equations for this circuit are:

$$\begin{array}{ll}\dfrac{dv_c(t)}{dt}=\dfrac{2}{RC}v_c(t)+\dfrac{2}{RC}v_{in}(t) & nT_S<t<nT_S+\sigma_1\\ v_c(t)=v_c(nT_S+\sigma_1) & nT_S+\sigma_1<t<nT_S+\sigma_2\\ \dfrac{dv_c(t)}{dt}=\dfrac{2}{RC}v_c(t)-\dfrac{2}{RC}v_{in}(t) & nT_S+\sigma_2<t<nT_S+\sigma_3\\ v_c(t)=v_c(nT_S+\sigma_3) & nT_S+\sigma_3<t<(n+1)T_S\end{array} \tag{8}$$

Where $v_c(t)$ is the voltage on the capacitor in Fig. 5. If one of the two switches is on, the output voltage will track the voltage on the capacitor. When switches are off, the voltage on the capacitor will be held, not affecting the output. Hence, the output spectrum contribution will be calculated in the track mode. As a result, A_k and B_k in (7) should be defined from either the first

or third equation in (8), depending on which switch is on. As a result, according to (8) for *k=1* and *k=3*: $A_1 = A_3 = B_1 = -B_3 = 2/(RC) = 2\pi f_{rc}$, where $f_{rc}=(\pi RC)^{-1}$ is defined as the 3dB bandwidth of a single low-pass filter with resistor R/2 and capacitor C (see Fig. 5).

Applying $v_{in}(t) = Ae^{j2\pi ft}$ as the input in the state equations in (8) and also assuming that $\tau_1 = \tau_3$ and $\tau_2 = \tau_4$, we can find $G_k(f)$ in (6) for *k=0,1* as:

$$G_0(f) = -\frac{\exp\left(j2\pi\tau_1(f-nf_S)\right)-\exp\left(-2\pi\tau_1 f_{rc}\right)}{\exp\left(j\pi(f-nf_S)/f_S\right)+\exp\left(-2\pi\tau_1 f_{rc}\right)}\cdot\frac{1}{1+j\left(f-nf_S\right)/f_{rc}}$$
$$G_1(f) = -G_0(f)\exp(j2\pi f\sigma_2) \tag{9}$$

Assuming the output voltage is following the voltage on capacitor C_1 during interval k=1, based on (8) the Fourier transform of the output can be found as:

$$V_{out,1}(f) = \sum_{n=-\infty}^{\infty} H_{n,1}(f)V_{in}(f-nf_S)$$
$$H_{n,1}(f) = \frac{1}{1+jf/f_{rc}}\left(\frac{1-\exp(-j2\pi n\tau_1 f_S)}{j2\pi n}+\frac{1+\exp(j2\pi\tau_2(f-nf_S)-j2\pi n\tau_1 f_S)}{2\pi f_{rc}/f_S}G_0(f)\right) \tag{10}$$

The output spectrum is the superposition of contributions for all N paths, and taking into account the phase shifts between the contributions the complete output spectrum can be found as:

$$V_{out}(f) = \sum_{n=-\infty}^{\infty} H_n(f)V_{in}(f-nf_S)$$

$$H_n(f) = \sum_{m=-1}^{N}\exp(j2\pi nm/N)H_{n,m}(f)$$

$$H_{n,m}(f) = \frac{1}{1+jf/f_{rc}}\left(\frac{1-\exp(-j2\pi n\tau_m f_S)}{j2\pi n}+\frac{1+\exp(j2\pi\tau_{m+1}(f-nf_s)-j2\pi n\tau_m f_S)}{2\pi f_{rc}/f_S}G_{0,m}(f)\right)$$

$$G_{0,m}(f) = -\frac{\exp(j2\pi\tau_m(f-nf_S))-\exp(-2\pi\tau_m f_{rc})}{\exp(j\pi(f-nf_S)/f_S)+\exp(-2\pi\tau_m f_{rc})}\cdot\frac{1}{1+j(f-nf_S)/f_{rc}} \tag{11}$$

Where $\tau_{m+1} = T_S/2-\tau_m$ for each path (see Fig. 5). According to (11) $H_n(f)$ is composed of N components generated by the N paths. We will now derive filter characteristics from (11).

IV. Characteristics of a Differential N-path Filter

A. Filtering and Harmonic Folding Back Effects

Analysis of (11) shows that $H_n(f)$ is undefined for n=0, but we can take the limit of $H_n(f)$ when "n" approaches continuously to zero, resulting in:

$$H_0(f)=\frac{N}{1+jf/f_{rc}}\left(\tau f_S+\frac{1+\exp(j\pi(T_S-2\tau)f)}{2\pi f_{rc}/f_S}\left(-\frac{\exp(j2\pi\tau f)-\exp(-2\pi\tau f_{rc})}{\exp(j\pi f/f_S)+\exp(-2\pi\tau f_{rc})}\cdot\frac{1}{1+jf/f_{rc}}\right)\right) \tag{12}$$

We assumed for an ideal N-path filter $\tau_1=\tau_2=...=\tau_N=\tau=T_S/N$. In (12) $H_0(f)$ represents the desired filtering characteristic without any frequency translation. $H_0(f)$ for a 4-path filter with the values of R=100Ω, C=50pF and f_S=500MHz is shown in Fig. 6. In Fig. 6 the comparison between theoretical transfer function from (12) and the simulated results applying Spectre RF PSS-PAC is shown, which fit completely on top of each other. Fig. 6 illustrates the desired filtering around the switching frequency with 1.8dB insertion loss; however, there are response peaks around odd harmonics of the switching frequency (repetitive poles in the denominator in (12)). Thanks to the differential architecture, even harmonics do not show peaking in the transfer function. From (11) we see that $H_n(f)\neq 0$ for $n=kN$ where k=0, ±1, ±2, …and is zero for other values of n. Thus folding back from input frequencies around $k(N\pm 1)f_S$ to the desired band around f_S occurs. Some non-zero terms which result in downconversion in a 4-path filter are shown in Fig. 7. For instance, k=1 renders non-zero $H_{\pm 4}(f)$, modeling folding from $3f_S$ and $5f_S$ to f_S (both with frequency shift $-4f_S$). However, for an 8-path architecture the first folding back will happen from $7f_S$. As a conclusion, increasing the number of paths will increase the distance between f_S and the first folded component around (N-1) f_S. Often, a passive low pass filter might be needed in front of the N-path filter and increasing N relaxes the low pass filter transition band requirements.

B. The Effect of the Switch Resistance

In order to include the effect of the switch resistance in our analysis, we consider the model shown in Fig. 8. Since in the architecture illustrated in Fig. 3, at any moment just two of the switches are on, the model in Fig. 8 includes two switch resistances in front of an ideal N-path filter with zero switch resistances. Employing (11) with $f_{rc}=(\pi C(R+R_{SW}))^{-1}$, the transfer

function from V_{in} to V_f can be easily found and using superposition of the V_{in} and V_f contribution we find:

$$V_{out}(f) = \frac{2R_{SW}}{R+2R_{SW}} V_{in}(f) + \frac{R}{R+2R_{SW}} \sum_{n=-\infty}^{\infty} H_n(f) V_{in}(f - nf_S) \tag{13}$$

If R_{SW} is set to zero in (13) it returns to the previous form of (11). Switch resistance can have strong impact on the maximum achievable rejection in N-path filters. To understand this, consider the frequency transfer function including the switch resistance effect for n=0:

$$H_{0,SW}(f) = \frac{2R_{SW}}{R+2R_{SW}} + \frac{R}{R+2R_{SW}} H_0(f) \tag{14}$$

According to (14), close to the switching frequency the effect of the switch resistance is not significant (H_0 term is close to 1 and dominates). But for frequencies further away from the switching frequency, where $H_0(f)$ is close to zero, the first term often dominates and the output can be approximated as: $V_{out}(f) = (2R_{SW}/(R+2R_{SW}))V_{in}(f)$. Thus, maximum filter rejection is limited by the switch resistance, as exemplified by Fig. 9 for the same 4-path filter used for Fig. 6 but with R_{SW}=5Ω. As a conclusion, in order to increase the maximum rejection of the filter, the switch resistance should be very small with respect to the source resistance R_S.

C. Input Impedance of an N-path Filter

In this section we will derive simple expressions for the input impedance of the N-path filter in Fig. 8 at the switching frequency, its odd harmonics and for frequencies far away from the peak points in Fig. 9. It will be shown that these impedances are all resistive. Around filter response peaks the filter becomes high-ohmic. To quantify the insertion loss and input impedance, we approximate (12) for $f_S >> f_{rc}$, $f \approx nf_S$ for odd *n*, resulting in:

$$H_0(nf_S) \approx \frac{2N(1-\cos(2\pi nD))}{4D(n\pi)^2} + (1-ND) \qquad 0 < D \le 1/N \tag{15}$$

Where n=1, N±1, 2N±1,…and $D = \tau / T_S$ is the duty cycle of each clock phase. As an example, if we substitute N=4 and D=1/4 and n=1, then $H_0(f_S) \approx 8/\pi^2$, i.e. 1.8dB insertion loss in the pass band, which fits to Fig. 6. According to (15) increasing N will reduce the insertion loss. As an example, for an 8-path system the insertion loss becomes 0.4dB. On the other hand, this will result in less attenuation at odd harmonics of the switching frequency which is undesired. Note that switch resistance can easily be taken into account by substituting (15) in (14) to find

an approximate equation for $H_{0,SW}(nf_S)$. To find the equivalent input impedance of the N-path system $Z_{in}(nf_S)$ we define: $H_{0,SW}(nf_S) = Z_{in}(nf_S)/(Z_{in}(nf_S)+R)$. As a result: $Z_{in}(nf_S) = H_{0,SW}(nf_S)R/(1-H_{0,SW}(nf_S))$. For a 4-path system (N=4, D=1/4) we find:

$$Z_{in}(nf_S) = R_{in}(nf_S) = \frac{8R + (n\pi)^2 R_{SW}}{(n\pi)^2 - 8} \tag{16}$$

Equation (16) predicts that at the switching frequency the input impedance of the N-path system is resistive, which is similar to a tank circuit at the resonance frequency. For n=1, (16) corresponds to the energy conservation based derivation in [12], but (16) can also be used for other values of n. For frequencies far away from the switching frequency and its odd harmonics, using (14) we again find purely resistive input impedance:

$$Z_{in}\,|_{\Delta f >> f_S} = R_{in}\,|_{\Delta f >> f_S} = \frac{R + 2R_{SW}}{ND} - R \tag{17}$$

Where for an ideal system (D=1/N) (17) reduces to $2R_{SW}$. Intuitively this can be understood because the capacitors act like a short circuit for $\Delta f >> f_S$.

We can conclude that for the switching frequency the N-path filter has high impedance (16) and for frequencies far away from the switching frequency it renders small impedance (17). We will now apply derivations in (15)-(17) to derive a simple RLC model for the N-path filter. Later in section V, (16) will be applied to define the required conditions for input power matching.

D. RLC Model, Bandwidth and Quality Factor

Around f_S , the filter transfer function $H_0(f)$ as shown in Fig. 6 resembles that of a high-Q tank circuit. Now we want to quantify this similarity and find an equivalent RLC model. As a result we can predict the quality factor and bandwidth for the N-path filter. Although (11) encompasses a repetitive pattern of poles and zeros, we are mostly interested in poles which occur close to the switching frequency. Equating the denominator of $H_n(f)$ in (11) to zero ($\exp(s/(2f_s)) + \exp(-2\pi D f_{rc}/f_S) = 0$) to find the poles, we find: $s = -4\pi D f_{rc} + j2\pi(2k+1)f_S$, k=0, ±1, ±2, …, indeed odd harmonics of f_S. In order to make a narrow band approximation we just consider the poles close to the switching frequency which are: $s = -4\pi D f_{rc} \pm j2\pi f_S$ and set these poles equal to the poles of the transfer function of Fig. 10, which is shown in (18):

$$H(s)=\frac{s/(RC_p)}{s^2+(R_p+R)s/(R_pRC_p)+1/(L_pC_p)} \tag{18}$$

As a result C_p and L_p in the RLC model can be found as:

$$C_p=\frac{R_p+R}{8R_pR\pi Df_{rc}} \tag{19a}$$

$$L_p=\frac{1}{4\pi^2C_p(f_S{}^2+4(Df_{rc})^2)}\approx\frac{1}{C_p(2\pi f_S)^2} \tag{19b}$$

The value of R_p in the RLC model is already derived in (16) for a 4-path system with n=1 for the switching frequency. Note that R_p and C_p are independent of f_S, in contrast to L_p. However, the term $4(Df_{rc})^2$ in the denominator of (19b) can be non-negligible compared with $f_S{}^2$. Thus the maximum peak in the transfer function can be slightly shifted to higher frequencies which also fits with the N-path filter responce. For $f_S >> f_{rc}$ this shift is negligible. To verify the validity of the RLC model, consider a 4-path filter with R=100Ω and C=50pF. Employing (16) and (19) we find C_p=30.8pF, L_p=3.27nH, R_p=430Ω. The comparison between the RLC model and exact transfer function in Fig. 11 shows a nearly perfect match around the switching frequency. Applying the RLC model we can find the bandwidth as: $BW=1/(2\pi(R\,||\,R_p)C_p)=4Df_{rc}$. Intuitively this can be understood considering that in Fig. 5 the resistor value charging the capacitor is R/2 and the capacitor sees this resistor value for a fraction 2D of the period, i.e. the effective resistor is R/(4D). Therefore the 3dB bandwidth becomes 4D times the low-pass filter bandwidth defined by f_{rc}. Finally for a 4-path system $BW=f_{rc}$ and $Q=f_S/BW=f_S/f_{rc}$.

E. Imbalance Multiphase Clocking and Mismatch in the Paths

Next consider what happens if there is mismatch between paths or if clocking signals deviate from the ideal situation. With mismatch, we can expect that even order terms are no longer perfectly cancelled and extra frequency components show up. As an example $H_{\pm2}(f)$ which was 0 for an ideal N-path system can be non-zero around the desired band. According to (11) this renders an image response (e.g. conversion from $f_{in}=f_S+\Delta f$ to $f_{out}=f_S-\Delta f$) and also folding back from signals around $f_{in}=2f_S$ to $f_{out}=f_S$. As we use large valued integrated capacitors (10s of pF) good matching is possible and therefore we focus on quantifying clock

phase errors. We model clock pulse width variations in the multiphase clocks and apply (11) considering unequal pulse widths. Fig.12 shows the calculated image suppression and folding back from $2f_S$. According to Fig. 12 one degree of phase error will result in 42dB of image rejection and 45dB suppression of second harmonic folding.

F. Noise

Most output noise power is due to the thermal noise of the source and switch resistances, where noise folding from around harmonics of f_S should be incorporated. As the switches do not carry DC current, the flicker noise of the switches can be neglected. At any moment two switches are in the on-state (see Fig. 3) and since noise contributions of the switches are not correlated, we can use the model in Fig. 13, similar to Fig. 8. As the input impedance around f_S (16) is significantly bigger than R, the noise voltage source $V_{n,R}$ has a much higher transfer to $V_{n,out}$ than $V_{n,SW}$ has, which should be beneficial for noise figure.

Relation (13) between the input and output spectrum of an LPTV system can also be applied to random signals. For Fig. 13a we can find $N_{out,R}(f)$, the thermal noise due to R:

$$N_{out,R}(f) = \left|\frac{2R_{SW} + RH_0(f)}{R + 2R_{SW}}\right|^2 N_R(f) + \sum_{n=-\infty, n\neq 0}^{\infty} \left|\frac{R}{R + 2R_{SW}} H_n(f)\right|^2 N_R(f - nf_S) \tag{20}$$

The first terms accounts for the noise power which appears at the output without any frequency translation and the second part accounts for noise folding, where $N_R(f - nf_S)$ is the frequency shifted version of the noise power generated by R. Note that $H_n(f)$ in (20) can be calculated by applying $f_{rc} = (\pi C(R + R_{SW}))^{-1}$ in (11).

To calculate the output noise power due to switch resistance we consider Fig. 13b. Similar to the previous case the frequency transfer from $V_{n,SW}$ to $V_{n,f}$ can be calculated from (11) with $f_{rc} = (\pi C(R + R_{SW}))^{-1}$. Then by applying the procedure described in section IV-B the transfer function from $V_{n,SW}$ to $V_{n,out}$ can be derived. Finally for the circuit in Fig. 13b we find:

$$N_{out,SW}(f) = \left(\frac{R}{R + 2R_{SW}}\right)^2 \left(\left|H_0(f) - 1\right|^2 N_{SW}(f) + \sum_{n=-\infty, n\neq 0}^{\infty} \left|H_n(f)\right|^2 N_{SW}(f - nf_S)\right) \tag{21}$$

Again the first part inside the second parenthesis in (21) corresponds to the noise power without frequency translation. Since $H_0(f)$ is close to one around the switching frequency for

an N-path filter (e.g. 0.81 for a 4-path architecture), the contribution of the first part is very small. The second part in (21) is the noise folding term and turns out to be almost negligible. For example, in a 4-path architecture with R_{SW}=5Ω and R=100Ω, the noise at the output due to switch resistance is approximately 2% of the total noise at the output. Finally, the noise factor can be calculated as: $F = N_{out}/(A_v^2 N_{in})$. For a 4-path differential filter with R_{SW}=5, R=100Ω the calculated noise figure from (20), (21) is 0.92dB, which is mainly caused by the noise folding of noise coming from the source resistance R.

V. Implementation of a 4-Path Differential Filter

A 4-path differential single port filter is realized in 65nm standard CMOS technology (see Fig. 14). The block diagram of the filter is illustrated in Fig. 15. Capacitors of 66pF are realized with NMOS transistors, at 720mV gate bias, to achieve large capacitance density with good linearity. NMOS switches of W/L=100/0.06 are driven by a 25% duty cycle 4-phase clocks. The clock phases are capacitively coupled to the gates of the switches which are biased at 950mV DC voltage to provide full 1.2V swing on the gate-source nodes of the switches. This swing insures the maximum achievable linearity for switches with fixed sizes. Increasing switch size will improve linearity and decrease the switch resistance, but larger switch size also means larger parasitic capacitors, affecting the frequency range and clock leakage and also requiring more clock power to drive the switches.

An off-chip wide-band (50-1000MHz, Mini-Circuits JTX-4-10T) RF transformer serves as a balun for single to differential conversion. Moreover, it increases the impedance level seen by the switched-capacitor circuit, increasing filter-Q without degrading its noise. The architecture in Fig. 15 also has an extra resistor R_M to provide input power matching to 50Ω. To find the required conditions for power matching we will use (16). Neglecting switch resistance, $R_{in}(f_S)$ "looking into the IC" can be written as: $R_{in} = 8R_{out}/(\pi^2 - 8)$, where R_{out} is the driving impedance seen by the IC (see Fig. 15). Then the required value for R_M to provide matching can be found as: $R_M = 4\pi^2 R_s/(16 - \pi^2)$. For Rs=50Ω the value for R_M becomes 322Ω. In practice, the insertion loss of the transformer is non-negligible and in our case it was actually sufficient to implement R_M. In the general case an equivalent total resistance R_M according to the derived value is needed for good S_{11}.

The simplified block diagram of the quadrature clock generator with low phase error [17] is shown in Fig. 16. A master clock (CLK) at 4 times the switching frequency is applied from off-chip. A flip-flop based divider divides the input clock by four, while an AND-gate between node A and B generates a 25% clock (see Fig. 16). Finally a shift register implemented with transmission gate flip-flops produces 4-phase clocks to drive the switches. These clocks are then capacitively coupled to the gate of the switches after proper buffering.

VI. Measurement Results and Comparison

An external differential high input impedance buffer amplifier is added to the circuit in Fig. 15 to be able to measure with 50Ω equipment without loading the output of the filter. We utilized Agilent ATF-54143 HEMT transistors to make an amplifier with high linearity and low noise in order to have minimum influence on the measurement results. Measurement results show that the tunable filter in Fig. 15 works from 100MHz up to at least 1GHz. Fig. 17 shows measurement results and compares them to a simulation employing an ideal transformer and R_M=322Ω for $f_S = 400MHz$, while also including a bond-wire inductance estimate. The buffer amplifier gain is de-embedded in all experiments, but the transformer effects are included. Considering the fact that R_{out} in Fig. 15 is 123Ω, R_{SW}≈5Ω and NMOS capacitors have the value of approximately 66pF (simulated value) then according to discussion in section IV-D bandwidth is calculated as 36MHz. The measured value for the bandwidth is 35MHz which renders a Q ranging from 3 to 29 (0.1 to 1GHz).

Close to f_S the input is matched to 50Ω for a narrow band, simplifying the design of a preceding band-pass or low-pass filter to mitigate the harmonic folding problem. The maximum filter rejection is limited by non-zero switch resistance and impedance R_{out}. Applying (17) and considering a 4-path architecture (N=4) and D=0.25 for frequencies far away from the switching frequency, input impedance R_{in} can be approximated as two times the switch resistance R_{SW}. The maximum rejection, α, can then be estimated as:

$$\alpha \approx 20\log(\frac{\pi^2}{8}\frac{2R_{SW}}{R_{out}+2R_{SW}}) \qquad (22)$$

Thus increasing R_{out} by applying the transformer not only results in less bandwidth and hence an increased Q, but also larger maximum achievable filter rejection. More attenuation can also be achieved using wider switches at the cost of clock driver power. In the implemented architecture,

R_{SW}≈5Ω, R_{out}=123Ω, resulting in α=-20.6dB. Measurement results render -16dB (Fig. 17). The difference is likely due to the effect of the non-zero rise and fall times of the clock, reducing the effective duty cycle to below 25%. According to (17) this results in larger input impedance and hence a smaller maximum rejection. Fig. 17 also illustrates the frequency selectivity around odd harmonics of the switching frequency. A rejection of 10dB is found around $3f_S$. Other harmonic responses are lower than the maximum attenuation (16dB) posed by the switch resistance and parasitics of the board, and are not observable in the measurement results.

Fig. 18 compares the calculated and measured values for folding back from all of the harmonics of f_S up to 15th. In this measurement the switching frequency is taken to be 100MHz and we have removed the transformer and applied a microwave hybrid with wider frequency band in order to remove the bandwidth limitation from the transformer. For odd harmonics the deviation between measurement and calculated results is due to band limitation imposed by the parasitics of the input of the chip. Even order harmonics are rejected due to the differential nature of the circuit, but mismatch and clock errors limit the rejection. Fig. 18 shows that spectral aliasing from even harmonics is better than -60dB. Measurement results of the in-band image rejection are presented in Fig. 19 and prove to be better than 50dB.

The differential architecture also reduces the power leakage from the switching clock to the RF input. In Fig. 15, the rising and falling edges of the clock mainly produce a common mode signal, which is suppressed by the common mode rejection of the transformer. At the RF input, the clock power <-62dBm was measured over the whole band. The flexible tuning capability of the filter is illustrated in Fig. 20 for f_S swept from 100MHz up to 1GHz. In-band S_{11} proves to be better than -10dB and the voltage transfer characteristic exhibits a maximum of 2dB passband attenuation over the entire tuning range. Due to parasitics of the transformer and PCB some peaking occurs at 100 and 200MHz center frequencies. The main frequency limitations of the current design are related to the clocking circuit and transformer. Wider frequency ranges are possible by improving the clocking circuit and removing the transformer for on-chip applications. The implemented 4-phase clock generator consumes between 2mW and 16mW ($f_s = 0.1 - 1GHz$, $f_{CLK} = 0.4 - 4GHz$). The rest of the circuit is free of dissipation from the supply.

Around the switching frequency the N-path filter has high input impedance ($4.3R_S$ in a 4-path filter). Thus not much current flows through the filter and one might intuitively expect good linearity, certainly for large switch-overdrive voltages (≈800mV). Fig. 21 shows IIP3 measurement results where the worst value within the 3dB bandwidth is reported. It is always better than 14dBm.

Noise figure measurements have been done using a low noise buffer amplifier. As de-embedding of the transformer and buffer amplifier noise contribution proved to be difficult, raw measured data are shown in Fig. 22. The NF including transformer and buffer amplifier is below 5.5dB. Two simulated curves (PSS+Pnoise in the Spectre RF) are also shown in Fig. 22 both for an ideal transformer and ideal buffer amplifier and: 1) R_M=322Ω (matched); 2) no R_M (unmatched). The latter case predicts about 1dB noise figure.

In table I the design is compared with two other on-chip filters, one using Q-enhancement [4] and the other an 8-path filter [9], clearly illustrating benefits in tuning-range, linearity and noise. In [9] the achieved Q is increased significantly by increasing source resistance and also increasing the total capacitance value without providing matching. Inserting a resistor deteriorates the NF significantly. Reactive impedance transformation as employed in this paper ensures a low NF.

VII. Conclusions

In this paper an integrated tunable band-pass filter based on N-path periodically time variant networks is analyzed, implemented and measured. The proposed differential 4-path architecture provides a high-Q inductor-less filter with a decade tuning range (0.1-1GHz). The availability of high quality switches in CMOS technology offers high linearity (≥14dBm) while according to theory and measurement, the architecture can have low noise as well (theoretically close to 1dB for the unmatched case, 3dB for the matched case). Although the filter rejection with this implementation is currently limited to 16dB, the extreme tunability and high linearity are attractive assets for software-defined or cognitive radio applications.

Acknowledgements

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Figure and Table Captions

Fig. 1. Architecture of an N-path filter [4] (p and q are the mixing functions and T is the period of the mixing frequency).

Fig. 2. (a) Switched-RC N-path filter. (b) Single port, single ended N-path filter. (c) Multiphase clocking. (d) Typical (in-band) input and output signal.

Fig. 3 Single port differential 4-path filter.

Fig. 4 Time intervals for the state space analysis.

Fig. 5 Differential Single path circuit and the clock phases for the switches.

Fig. 6 Theoretical and simulated curve for $H_0(f)$ af $f_S = 500MHz$.

Fig. 7 $H_n(f)$ around the switching frequency for a 4-path filter. This determines the folding back from odd harmonics of the switching frequency ($f_S = 500MHz$).

Fig. 8. N-path filter with switch resistance.

Fig. 9 Switch resistance effect on the maximum rejection of a 4-path filter (R=100Ω and C=50pF)

Fig. 10 Equivalent RLC circuit model for the N-path filter.

Fig. 11 Comparison of the transfer of the RLC model with the full N-path filter model (11).

Fig. 12 Image and second harmonic rejection with phase error in the driving clock phases.

Fig. 13 The model considered for noise calculation (a) Source noise (b) Switch resistance noise.

Fig. 14 Micrograph of the 65nm CMOS chip.

Fig. 15. Filter architecture including a balun and buffer amplifier for measurements.

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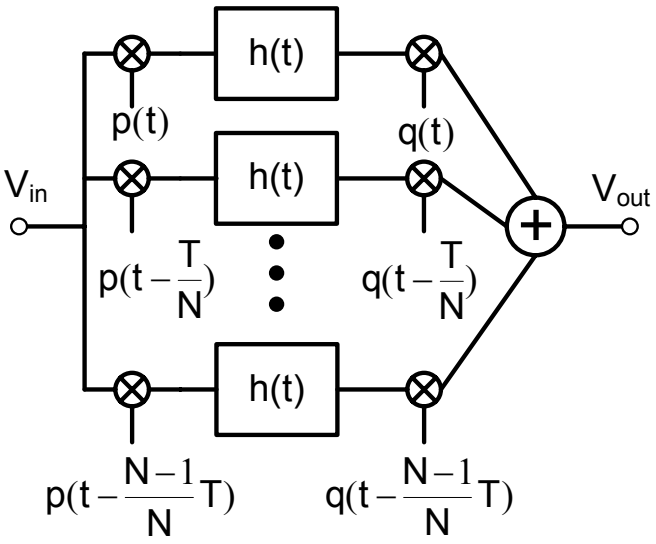
Fig. 21. Measured minimum IIP3 for $f_S = 0.1 - 1GHz$.

Fig. 22 Measured and simulated noise figure.

TABLE I. COMPARISON WITH OTHER DESIGNS



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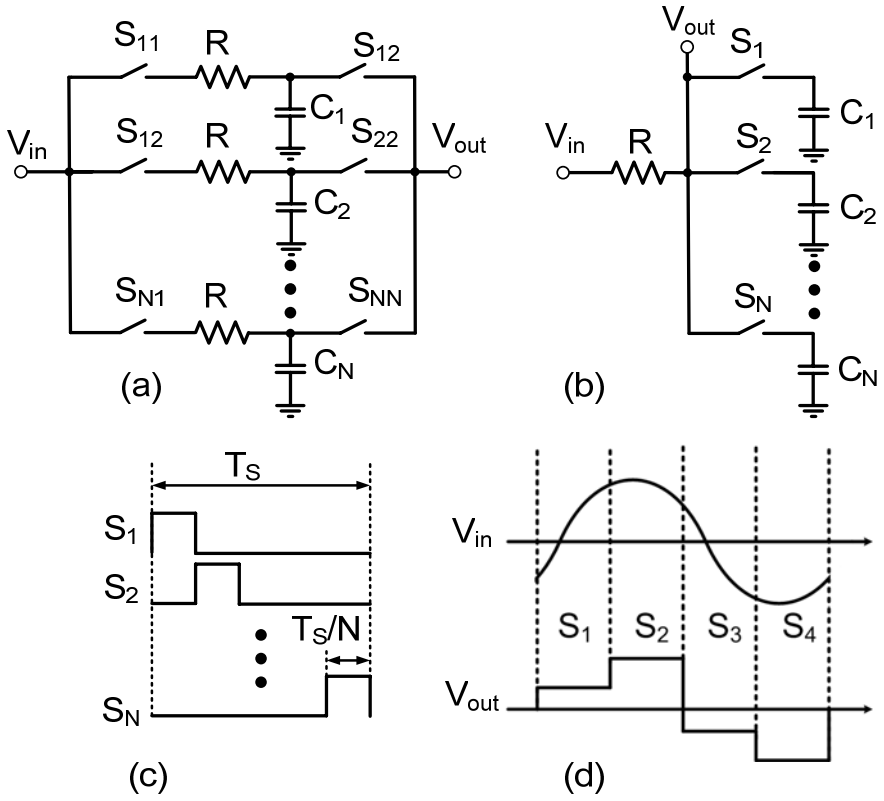

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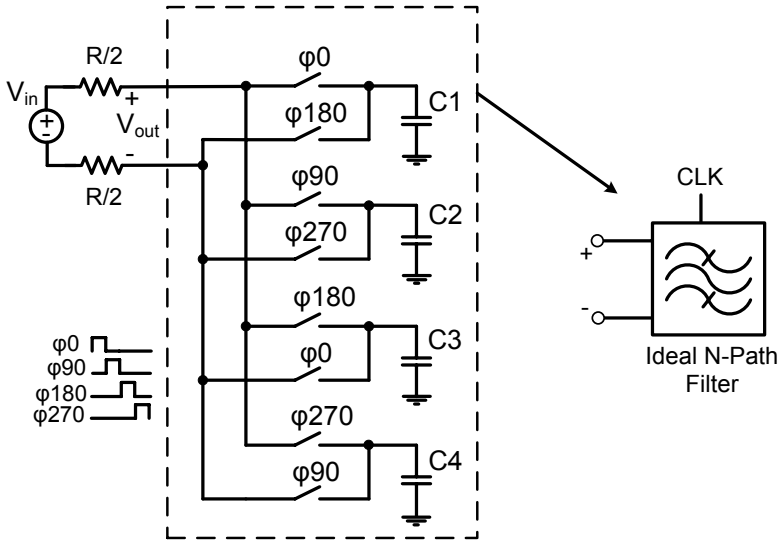
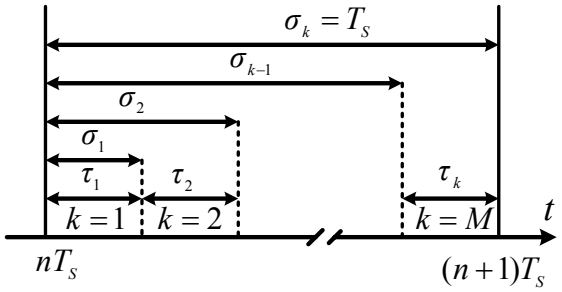


Fig. 3 Single port differential 4-path filter.



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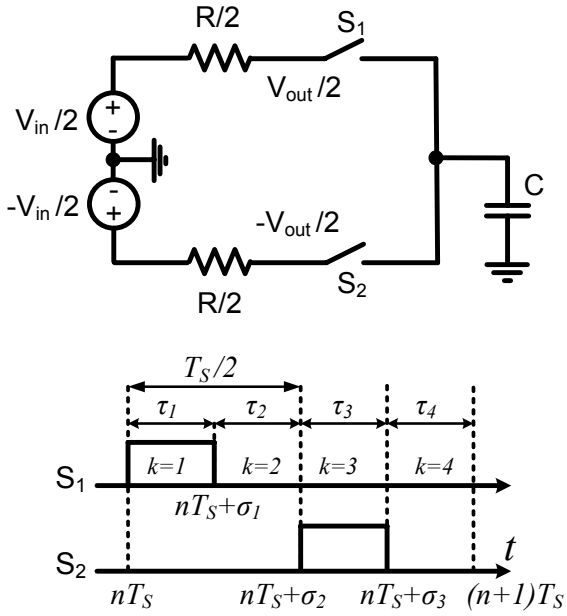

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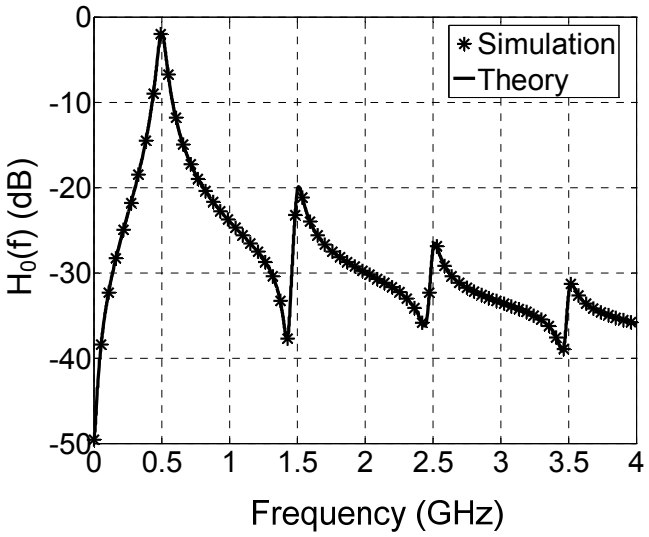
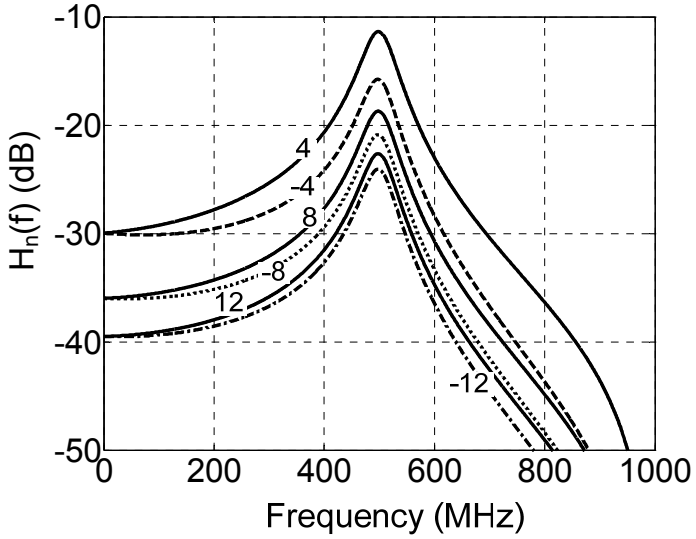


Fig. 6 Theoretical and simulated curve for $H_0(f)$ at $f_S = 500MHz$.



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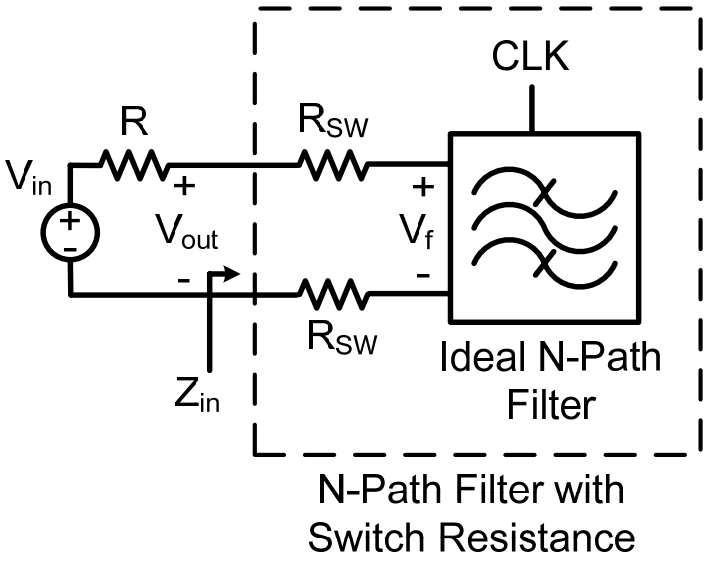

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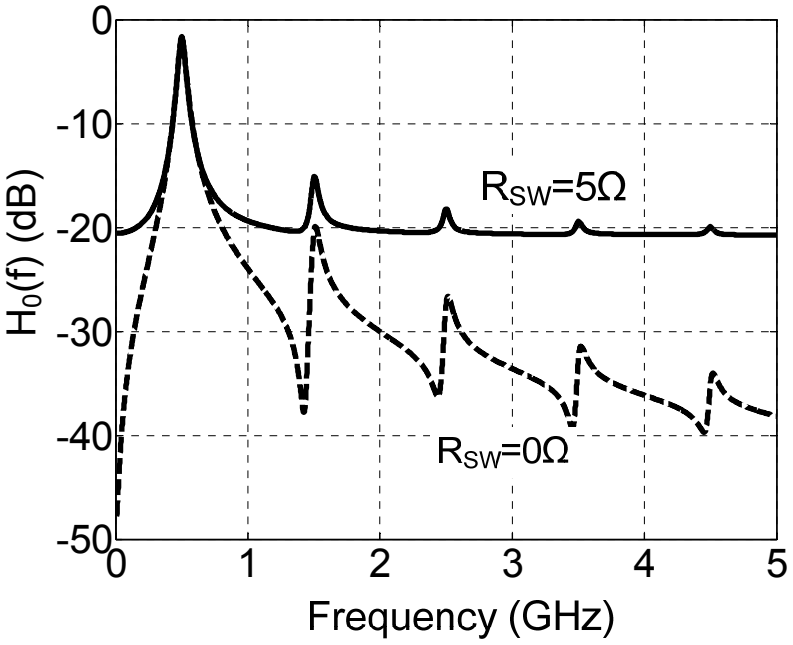

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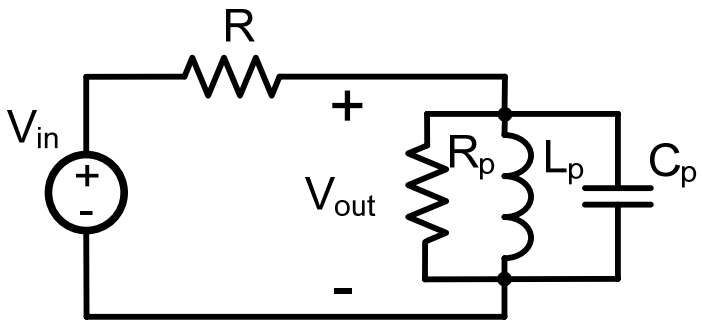

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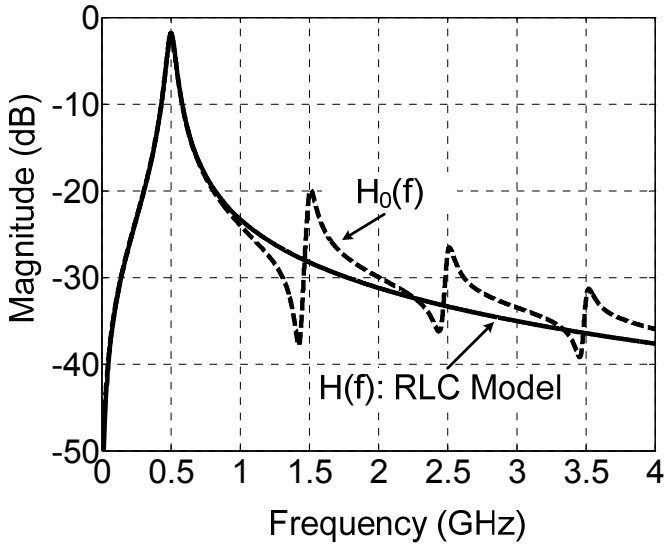
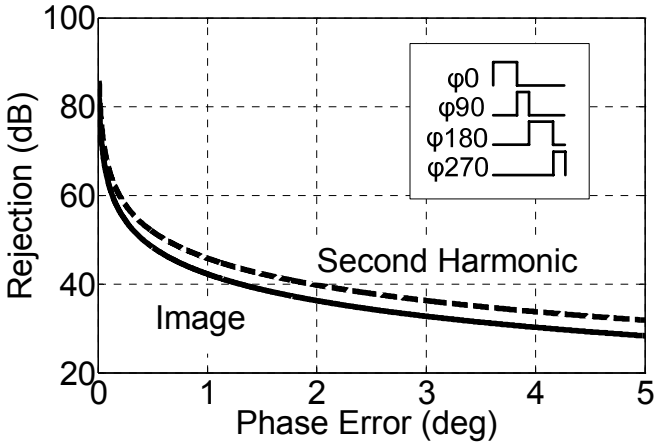


Fig. 11 Comparison of the transfer of the RLC model with the full N-path filter model (11).



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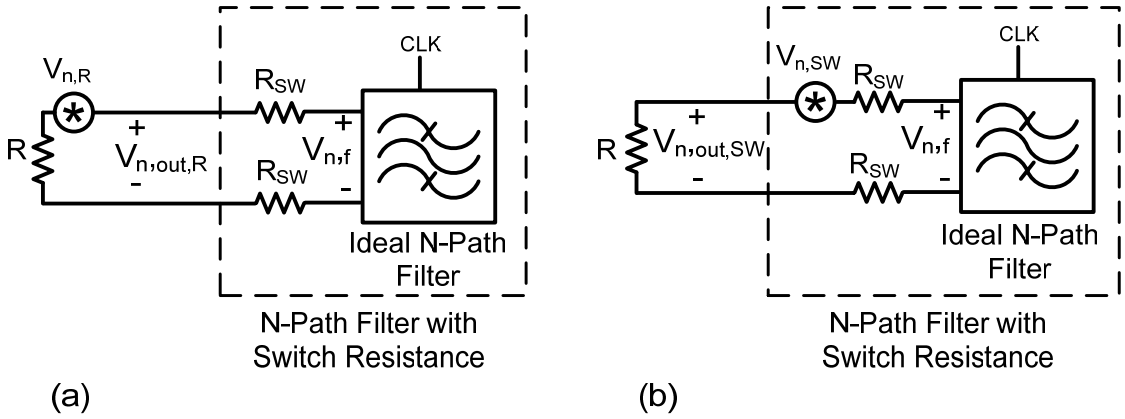

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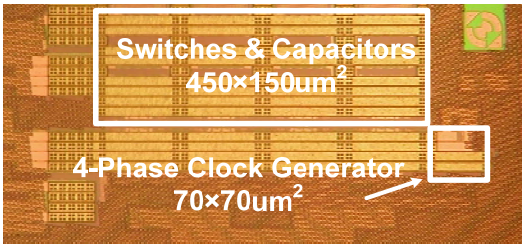
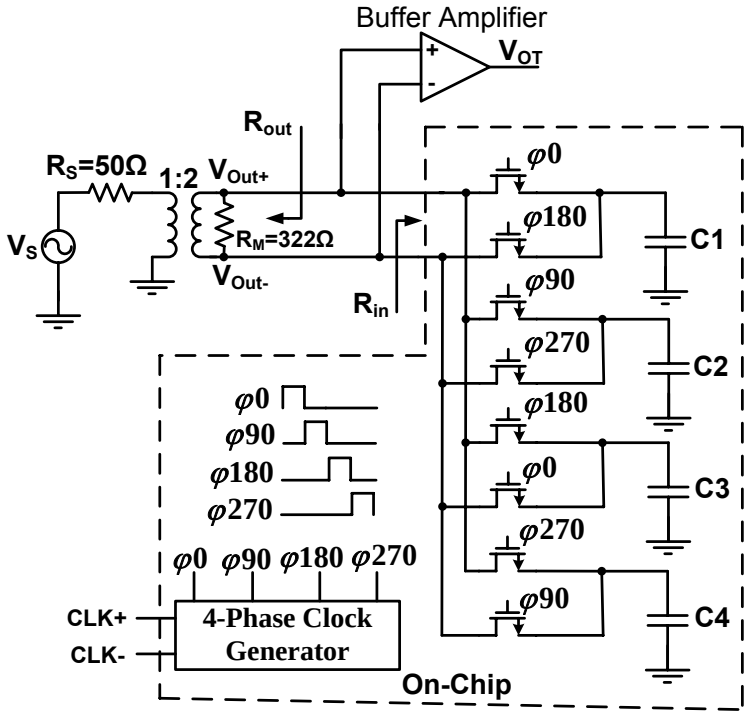


Fig. 14 Micrograph of the 65nm CMOS chip.



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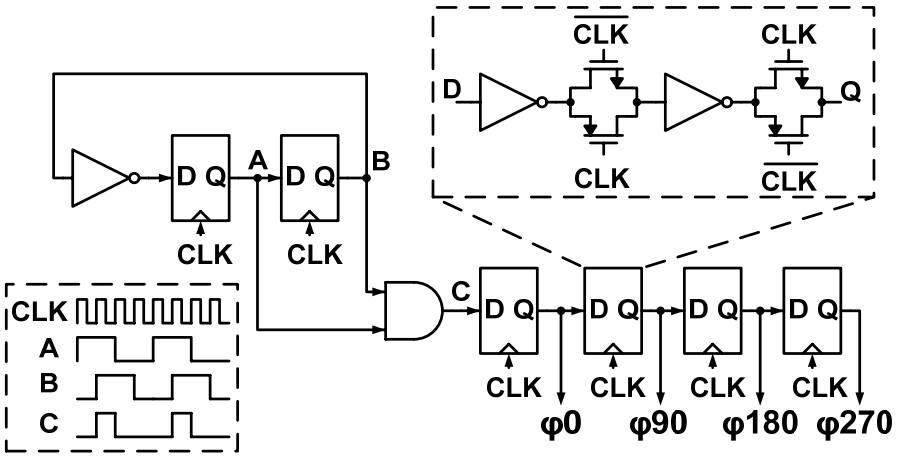


Fig. 16 Multiphase clock generator.

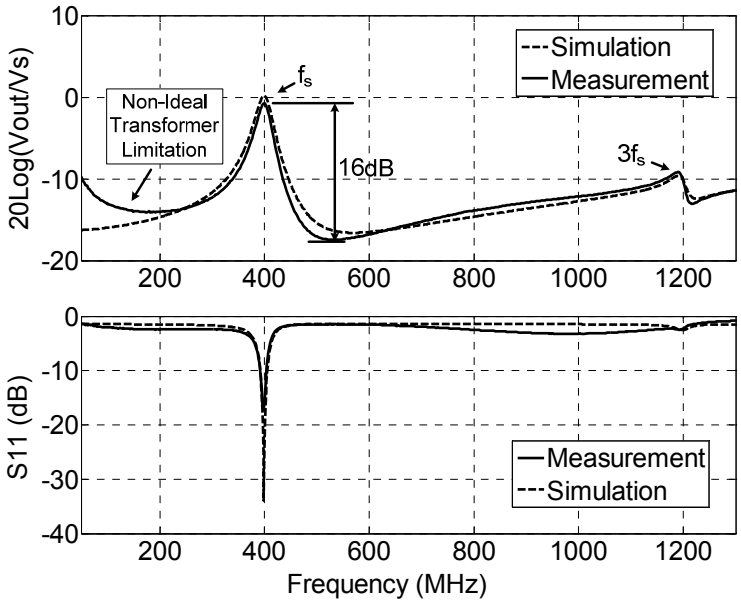
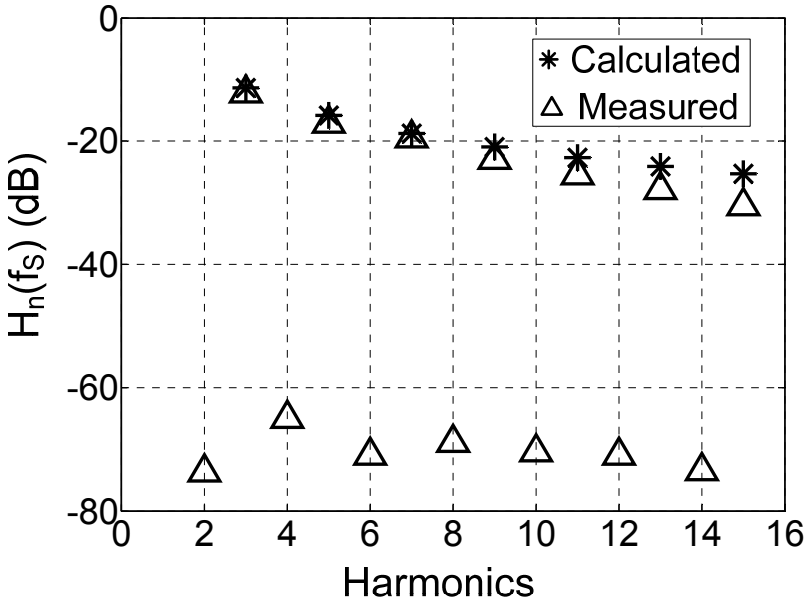


Fig. 17 Frequency transfer and S_{11} at $f_S = 400MHz$.



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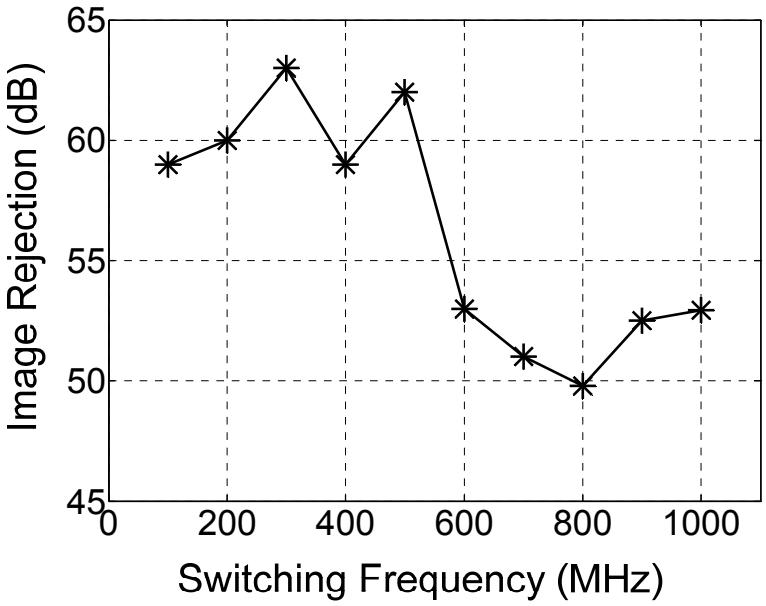
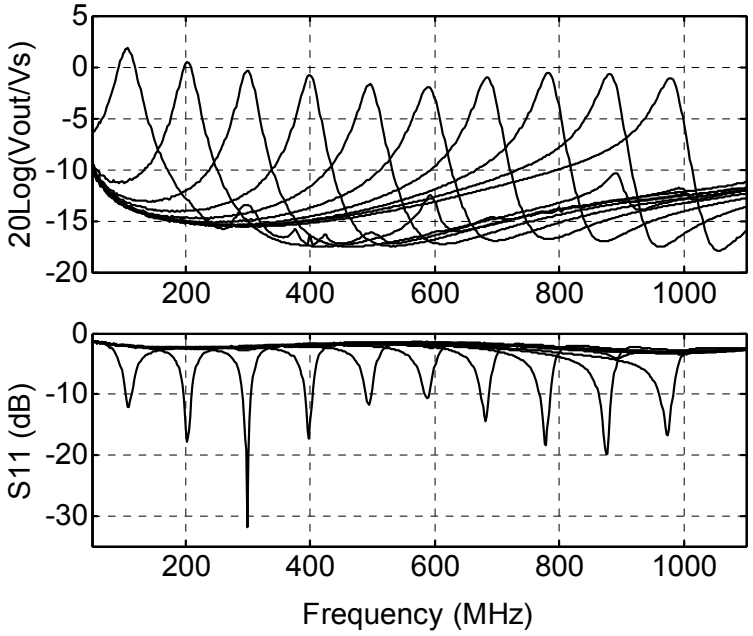


Fig. 19. Measured in-band image rejection for $f_S = 0.1 - 1GHz$.



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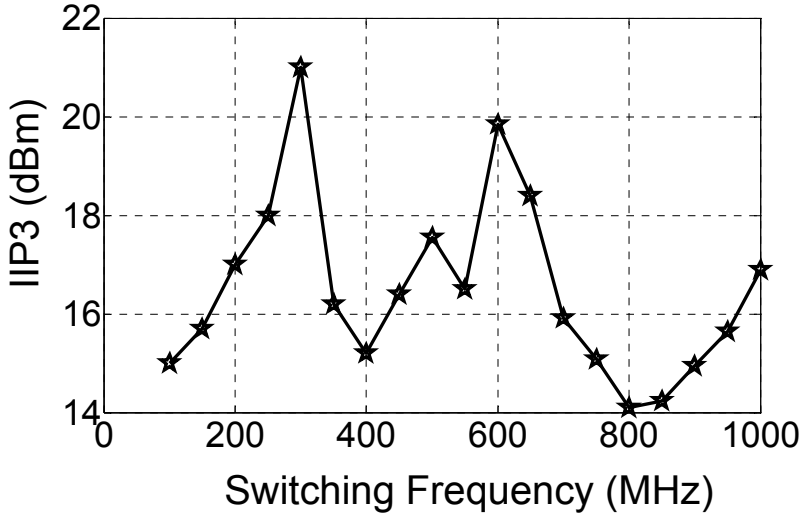

Fig. 21. Measured minimum IIP3 for $f_S = 0.1 - 1GHz$.

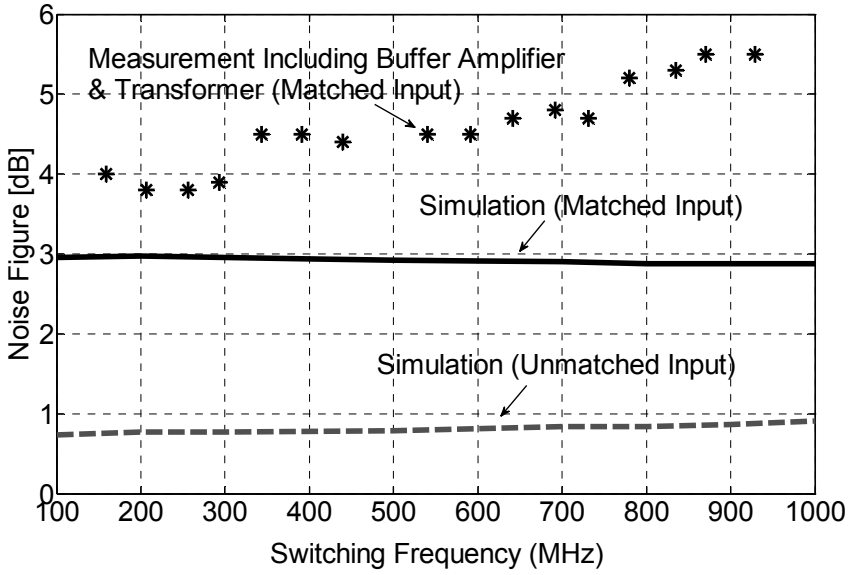

Fig. 22 Measured and simulated noise figure.

TABLE I

COMPARISON WITH OTHER DESIGNS

Performance	**This Work**	**[9]**	**[4]**
Process	65nm CMOS	0.35um CMOS	0.18um CMOS
Active Area	0.07 mm^2	1.9mm^2	0.81mm^2
Power Consumption	2 to 16mW	63mW	17mW
Frequency Tuning Range	0.1 to 1GHz	240 to 530MHz	2 to 2.06GHz
-3dB Band Width	35MHz	1.75 to 4.6MHz	130MHz
Voltage Gain	-2dB	-2dB	0dB
Quality Factor (Q)	3 to 29	301 to 114	15.4 to 15.8
P_{1dB}	2dBm	-5dBm	-6.6dBm
IIP3	14dBm	NA	2.5dBm
Noise Figure	<5.5dB	9dB	15dB

REFERENCES

[1] Nekovee, M.; , "Cognitive Radio Access to TV White Spaces: Spectrum Opportunities, Commercial Applications and Remaining Technology Challenges," *New Frontiers in Dynamic Spectrum, 2010 IEEE Symposium on* , vol., no., pp.1-10, 6-9 April 2010 doi: 10.1109/DYSPAN.2010.5457902

[2] W. B. Kuhn, A. Nobbe, D. Kelly, A. W. Orsborn, "Dynamic Range Performance of On-Chip RF Bandpass Filters," IEEE Trans. Circuits Syst. II, vol. 50, no. 10, pp. 685–694, Oct. 2003.

[3] X. He, W. B. Kuhn, "A 2.5-GHz Low-Power, High Dynamic Range, Self-Tuned Q-Enhanced LC Filter in SOI," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp 1618-1628, Aug. 2005.

[4] B. Georgescu, I. G. Finvers, F. Ghannouchi, "2 GHz Q-Enhanced Active Filter with Low Passband Distortion and High Dynamic Range," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp 2029-2039, Sep. 2006.

[5] L. E. Franks and I. W. Sandberg, "An alternative approach to the realization of network transfer functions: The N-path Filters," *Bell Sys. Tech. J.*, vol. 39, pp. 1321-1350, September 1960.

[6] L. E. Franks and F. J. Witt, "Solid-state sampled data band-pass filters," *Proc. Solid-Slate Circuits Conf*. (Philadelphia, Pa.), Feb. 1960.

[7] Y. Sun, I. T. Frisch, "A general theory of commutated networks," IEEE Trans. Circuit Theory, vol. CT-16, no. 4, pp. 502-508, Nov. 1969.

[8] M. B. Ghaderi, J. A. Nossek, G. C. Temes, "Narrow-band switched-capacitor bandpass filters," *IEEE Trans. Circuits Syst.*, vol. CAS-29, no. 8, pp. 557–572, Aug. 1982.

[9] A. El Qualkadi, M. El Kaamouchi, J. M. Paillot, D. V. Janvier, D. Flandre, "Fully integrated high-Q switched capacitor bandpass filter with center frequency and bandwidth tuning", *IEEE RFIC Sym.*, pp. 681-684, 2007.

[10] A. Ghaffari, E. A. M. Klumperink, B. Nauta, "A Differential 4-Path Highly Linear Widely Tunable On-Chip Band-Pass Filter," *IEEE RFIC Sym.*, pp. 299-302, May 2010.

[11] A. Mirzaei, A. Yazdi, Z. Zhou, E. Chang, P. Suri, and H. Darabi , "A 65nm CMOS quad-band SAW-less receiver for GSM/GPRS/EDGE," *IEEE VLSI Sym.* , pp. 179-180, June 2010.

[12] B. W. Cook, A. Berny, A. Molnar, "Low-Power 2.4-GHz Transceiver with Passive RX Front-End and 400-mV Supply," *IEEE J. Solid-State Circuits* , vol. 41, no. 12, pp. 2757-2766, Dec. 2006.

[13] M.C.M. Soer, E.A.M. Klumperink, Z. Ru, F.E van Vliet, B. Nauta "A 0.2-to-2.0GHz CMOS receiver without LNA achieving >11dBm IIP3 and <6.5 dB NF," *ISSCC Dig. Tech. Papers*, pp. 222-223, Feb. 2009.

[14] T. Ström and S. Signell, "Analysis of periodically switched linear circuits," *IEEE Trans. Circuits Syst.*, vol. CAS-24, no. 10, pp. 531–541, Oct. 1977.

[15] M.C.M. Soer, E.A.M. Klumperink, PT de Boer, F.E. van Vliet, B. Nauta, "Unified frequency domain analysis of switched-series-RC passive mixers and samplers," IEEE Transactions on Circuits and Systems I: Regular Papers, vol.PP, no.99, pp.1-1, 0 doi: 10.1109/TCSI.2010.2046968

[16] B. Leung, VLSI for Wireless Communication. Englewood Cliffs, NJ: Prentice-Hall, 2002.

[17] Z. Ru, N.A. Moseley, E.A.M. Klumperink and B. Nauta , " Digitally Enhanced Software-Defined Radio Receiver Robust to Out-of-Band Interference", IEEE J. Solid-State Circuits, vol. 44, no. 12, pp. 3359-3375, dec. 2009