PENTEK®

Setting the Standard for Digital Signal Processing

Software Defined Radio Handbook
Eighth Edition

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by

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Preface

SDR (Software Defined Radio) has revolutionized electronic systems for a
variety of applications including communications, data acquisition and signal processing.

This handbook shows how DDCs (Digital Downconverters) and DUCs (Digital Upconverters),
the fundamental building blocks of SDR, can replace conventional analog receiver designs,
offering significant benefits in performance, density and cost.

In order to fully appreciate the benefits of SDR, a conventional analog receiver
system will be compared to its digital receiver counterpart, highlighting similarities and differences.

The inner workings of the SDR will be explored with an in-depth description of the internal
structure and the devices used. Finally, some actual board- and system-level implementations and available
off-the-shelf SDR products for embedded systems will be described.
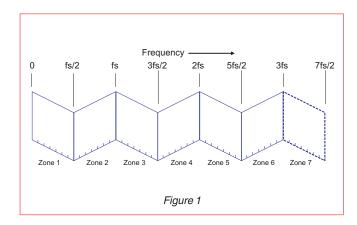
Sampling

Nyquist's Theorem and Sampling

Before we look at SDR and its various implementations in embedded systems, we'll review a theorem fundamental to sampled data systems such as those encountered in software defined radios.

Nyquist's Theorem:

"Any signal can be represented by discrete samples if the sampling frequency is at least twice the bandwidth of the signal."

Notice that we highlighted the word bandwidth rather than frequency. In what follows, we'll attempt to show the implications of this theorem and the correct interpretation of sampling frequency, also known as sampling rate.
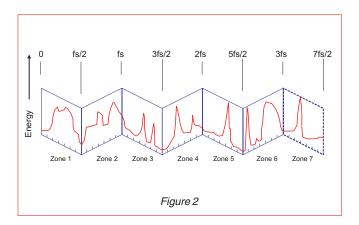
A Simple Technique to Visualize Sampling
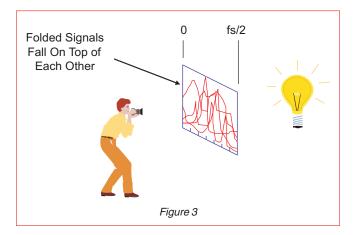

Figure 1

To visualize what happens in sampling, imagine that you are using transparent "fan-fold" computer paper. Use the horizontal edge of the paper as the frequency axis and scale it so that the paper folds line up with integer multiples of one-half of the sampling frequency f_s. Each sheet of paper now represent what we will call a "Nyquist Zone", as shown in Figure 1.
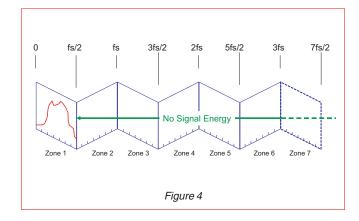
Sampling

Sampling Basics

Figure 2

Use the vertical axis of the fan-fold paper for signal energy and plot the frequency spectrum of the signal to be sampled, as shown in Figure 2. To see the effects of sampling, collapse the transparent fan-fold paper into a stack.

Figure 3

The resulting spectrum can be seen by holding the transparent stack up to a light and looking through it. You can see that signals on all of the sheets or zones are "folded" or "aliased" on top of each other — and they can no longer be separated.

Once this folding or aliasing occurs during sampling, the resulting sampled data is corrupted and can never be recovered. The term "aliasing" is appropriate because after sampling, a signal from one of the higher zones now appears to be at a different frequency.

Baseband Sampling

Figure 4

A baseband signal has frequency components that start at $f = 0$ and extend up to some maximum frequency.

To prevent data destruction when sampling a baseband signal, make sure that all the signal energy falls ONY in the 1st Nyquist band, as shown in Figure 4.

There are two ways to do this:
1. Insert a lowpass filter to eliminate all signals above $f_s/2$, or
2. Increase the sampling frequency so all signals present fall below $f_s/2$.

Note that $f_s/2$ is also known as the "folding frequency".

Sampling Bandpass Signals

Let's consider bandpass signals like the IF frequency of a communications receiver that might have a 70 MHz center frequency and 10 MHz bandwidth. In this case, the IF signal contains signal energy from 65 to 75 MHz.

If we follow the baseband sampling rules above, we must sample this signal at twice the highest signal frequency, meaning a sample rate of at least 150 MHz.

However, by taking advantage of a technique called "undersampling", we can use a much lower sampling rate.

Sampling

Undersampling

Figure 5

Figure 6

Undersampling allows us to use aliasing to our advantage, providing we follow the strict rules of the Nyquist Theorem.
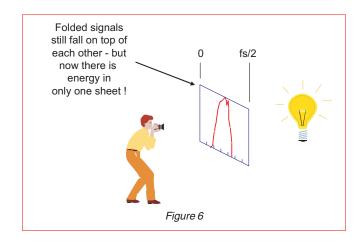
In our previous IF signal example, suppose we try a sampling rate of 40 MHz.

Figure 5 shows a fan-fold paper plot with Fs = 40 MHz. You can see that zone 4 extends from 60 MHz to 80 MHz, nicely containing the entire IF signal band of 65 to 75 MHz.

Now when you collapse the fan fold sheets as shown in Figure 6, you can see that the IF signal is preserved after sampling because we have no signal energy in any other zone.

Also note that the odd zones fold with the lower frequency at the left (normal spectrum) and the even zones fold with the lower frequency at the right (reversed spectrum).

In this case, the signals from zone 4 are frequency reversed. This is usually very easy to accommodate in the following stages of SDR systems.

The major rule to follow for successful undersampling is to make sure all of the energy falls entirely in one Nyquist zone.

There two ways to do this:
1. Insert a bandpass filter to eliminate all signals outside the one Nyquist zone.
2. Increase the sampling frequency so all signals fall entirely within one Nyquist zone.

Summary

Baseband sampling requires the sample frequency to be at least twice the signal bandwidth. This is the same as saying that all of the signals fall within the first Nyquist zone.
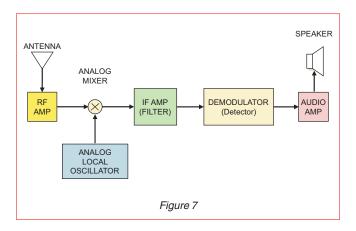
In real life, a good rule of thumb is to use the 80% relationship:

$$\text{Bandwidth} = 0.8 \text{ x } f_s/2$$

Undersampling allows a lower sample rate even though signal frequencies are high, PROVIDED all of the signal energy falls within one Nyquist zone.

To repeat the Nyquist theorem: The sampling frequency must be at least twice the signal bandwidth — not the signal frequency.

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Analog Radio Receiver Block Diagram

Figure 7

Analog Radio Receiver Mixer

Figure 8

The conventional heterodyne radio receiver shown in Figure 7, has been in use for nearly a century. Let's review the structure of the analog receiver so comparison to a digital receiver becomes apparent.

First the RF signal from the antenna is amplified, typically with a tuned RF stage that amplifies a region of the frequency band of interest.

This amplified RF signal is then fed into a mixer stage. The other input to the mixer comes from the local oscillator whose frequency is determined by the tuning control of the radio.
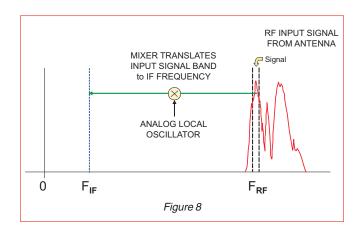
The mixer translates the desired input signal to the IF (Intermediate Frequency) as shown in Figure 8.

The IF stage is a bandpass amplifier that only lets one signal or radio station through. Common center frequencies for IF stages are 455 kHz and 10.7 MHz for commercial AM and FM broadcasts.

The demodulator recovers the original modulating signal from the IF output using one of several different schemes.

For example, AM uses an envelope detector and FM uses a frequency discriminator. In a typical home radio, the demodulated output is fed to an audio power amplifier which drives a speaker.

The mixer performs an analog multiplication of the two inputs and generates a difference frequency signal.

The frequency of the local oscillator is set so that the difference between the local oscillator frequency and the desired input signal (the radio station you want to receive) equals the IF.

For example, if you wanted to receive an FM station at 100.7 MHz and the IF is 10.7 MHz, you would tune the local oscillator to:

$$100.7 - 10.7 = 90 \text{ MHz}$$

This is called "downconversion" or "translation" because a signal at a high frequency is shifted down to a lower frequency by the mixer.

The IF stage acts as a narrowband filter which only passes a "slice" of the translated RF input. The bandwidth of the IF stage is equal to the bandwidth of the signal (or the "radio station") that you are trying to receive.

For commercial FM, the bandwidth is about 100 kHz and for AM it is about 5 kHz. This is consistent with channel spacings of 200 kHz and 10 kHz, respectively.

Principles of SDR

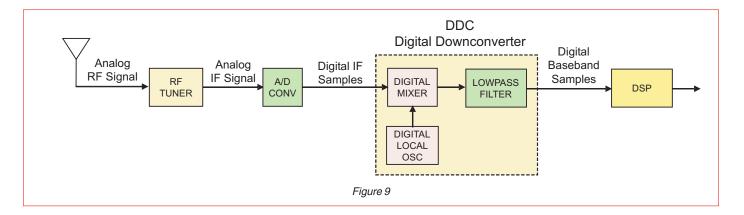## SDR Receiver Block Diagram

Figure 9

Figure 9 shows a block diagram of a software defined radio receiver. The RF tuner converts analog RF signals to analog IF frequencies, the same as the first three stages of the analog receiver.

The A/D converter that follows digitizes the IF signal thereby converting it into digital samples. These samples are fed to the next stage which is the digital downconverter (DDC) shown within the dotted lines.

The digital downconverter is typically a single monolithic chip or FPGA IP, and it is a key part of the SDR system.

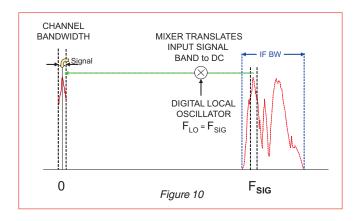A conventional DDC has three major sections:

- **A digital mixer**
- **A digital local oscillator**
- **An FIR lowpass filter**

The digital mixer and local oscillator translate the digital IF samples down to baseband. The FIR lowpass filter limits the signal bandwidth and acts as a decimating lowpass filter. The digital downconverter includes a lot of hardware multipliers, adders and shift register memories to get the job done.

The digital baseband samples are then fed to a block labeled DSP which performs tasks such as demodulation, decoding and other processing tasks.

Traditionally, these needs have been handled with dedicated application specific ICs (ASICs), and programmable DSPs.

SDR Receiver Mixer

Figure 10

At the output of the mixer, the high frequency wideband signals from the A/D input (shown in Figure 10 above) have been translated down to DC as complex I and Q components with a frequency shift equal to the local oscillator frequency.

This is similar to the analog receiver mixer except *there*, the mixing was done down to an IF frequency. *Here*, the complex representation of the signal allows us to go right down to DC.

By tuning the local oscillator over its range, any portion of the RF input signal can be mixed down to DC.

In effect, the wideband RF signal spectrum can be "slid" around 0 Hz, left and right, simply by tuning the local oscillator. Note that upper and lower sidebands are preserved.

DDC Local Oscillator and Decimation

Figure 11A Local Oscillator Frequency Switching

Figure 11B FIR Filter Decimation

Because the local oscillator uses a digital phase accumulator, it has some very nice features. It switches between frequencies with phase continuity, so you can generate FSK signals or sweeps very precisely with no transients as shown in Figure 11A.

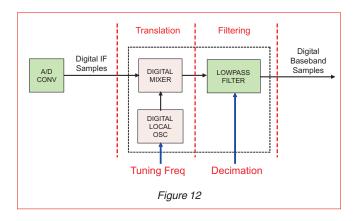The frequency accuracy and stability are determined entirely by the A/D clock so it's inherently synchronous to the sampling frequency. There is no aging, drift or calibration since it's implemented entirely with digital logic.

Since the output of the FIR filter is band limited, the Nyquist theorem allows us to lower the sample rate. If we are keeping only one out of every N samples, as shown in Figure 11B above, we have dropped the sampling rate by a factor of N.

DDC Signal Processing

Figure 12

This process is called *decimation* and it means keeping one out of every N signal samples. If the decimated output sample rate is kept higher than twice the output bandwidth, no information is lost.

The clear benefit is that decimated signals can be processed easier, can be transmitted at a lower rate, or stored in less memory. As a result, decimation can dramatically reduce system costs!

As shown in Figure 12, the DDC performs two signal processing operations:

1. Frequency translation with the tuning controlled by the local oscillator.

2. Lowpass filtering with the bandwidth controlled by the decimation setting.

We will next turn our attention to the Software Defined Radio Transmitter.

Principles of SDR

SDR Transmitter Block Diagram

Figure 13

The input to the transmit side of an SDR system is a digital baseband signal, typically generated by a DSP stage as shown in Figure 13 above.

The digital hardware block in the dotted lines is a DUC (digital upconverter) that translates the baseband signal to the IF frequency.

The D/A converter that follows converts the digital IF samples into the analog IF signal.

Next, the RF upconverter converts the analog IF signal to RF frequencies.

Finally, the power amplifier boosts signal energy to the antenna.

DUC Signal Processing

Figure 14

Inside the DUC shown in Figure 14, the digital mixer and local oscillator at the right translate baseband samples up to the IF frequency. The IF translation frequency is determined by the local oscillator.

The mixer generates one output sample for each of its two input samples. And, the sample frequency at the mixer output must be equal to the D/A sample frequency f_s.

Therefore, the local oscillator sample rate and the baseband sample rate must be equal to the D/A sample frequency f_s.

The local oscillator already operates at a sample rate of f_s, but the input baseband sample frequency at the left is usually much lower. This problem is solved with the *Interpolation Filter*.

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Interpolation Filter: Time domain

Figure 15

Interpolation Filter: Frequency Domain

Figure 16

The interpolation filter must boost the baseband input sample frequency of f_s/N up to the required mixer input and D/A output sample frequency of f_s.

The interpolation filter increases the sample frequency of the baseband input signal by a factor N, known as the interpolation factor.

At the bottom of Figure 15, the effect of the interpolation filter is shown in the time domain.

Notice the baseband signal frequency content is completely preserved by filling in additional samples in the spaces between the original input samples.

The signal processing operation performed by the interpolation filter is the inverse of the decimation filter we discussed previously in the DDC section.
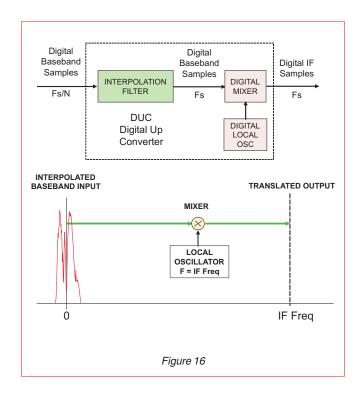
Figure 16 is a frequency domain view of the digital upconversion process.

This is exactly the opposite of the frequency domain view of the DDC in Figure 10.

The local oscillator setting is set equal to the required IF signal frequency, just as with the DDC.

Principles of SDR

DDC Processing

Figure 17

DUC Processing

Figure 18

Figure 17 shows the two-step processing performed by the digital downconverter.

Frequency translation from IF down to baseband is performed by the local oscillator and mixer.

The "tuning" knob represents the programmability of the local oscillator frequency to select the desired signal for downconversion to baseband.

The baseband signal bandwidth is set by setting decimation factor N and the lowpass FIR filter:

- Baseband sample frequency $f_b = f_s/N$
- Baseband bandwidth = 0.8 x f_b

The baseband bandwidth equation reflects a typical 80% passband characteristic, and complex (I+Q) samples.

The "bandwidth" knob represents the programmability of the decimation factor to select the desired baseband signal bandwidth.

Figure 18 shows the two-step processing performed by the digital upconverter:

The ratio between the required output sample rate and the sample rate input baseband sample rate determines the interpolation factor N.

- Baseband bandwidth = 0.8 x f_b
- Output sample frequency $f_s = f_b$ x N

Again, the bandwidth equation assumes a complex (I+Q) baseband input and an 80% filter.

The "bandwidth" knob represents the programmability of the interpolation factor to select the desired input baseband signal bandwidth.

Frequency translation from baseband up to IF is performed by the local oscillator and mixer.

The "tuning" knob represents the programmability of the local oscillator frequency to select the desired IF frequency for translation up from baseband.

Principles of SDR

Key DDC and DUC Benefits

Figure 19

SDR Tasks

Figure 20
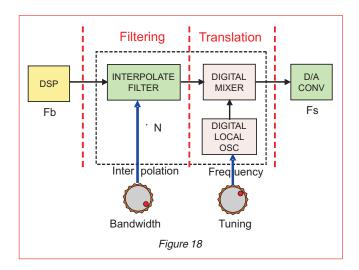
Think of the DDC as a hardware preprocessor for programmable DSP or GPP processor. It preselects only the signals you are interested in and removes all others. This provides an optimum bandwidth and minimum sampling rate into the processor.

The same applies to the DUC. The processor only needs to generate and deliver the baseband signals sampled at the baseband sample rate. The DUC then boosts the sampling rate in the interpolation filter, performs digital frequency translation, and delivers samples to the D/A at a very high sample rate.

The number of processors required in a system is directly proportional to the sampling frequency of input and output data. As a result, by reducing the sampling frequency, you can dramatically reduce the cost and complexity of the programmable DSPs or GPPs in your system.

Not only do DDCs and DUCs reduce the processor workload, the reduction of bandwidth and sampling rate helps save time in data transfers to another subsystem. This helps minimize recording time and disk space, and reduces traffic and bandwidth across communication channels.

Here we've ranked some of the popular signal processing tasks associated with SDR systems on a two axis graph, with compute Processing Intensity on the vertical axis and Flexibility on the horizontal axis.

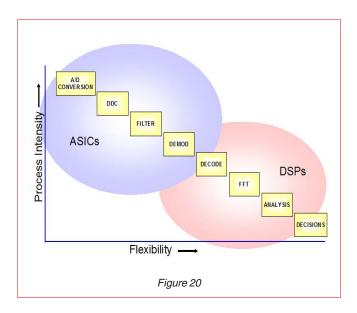What we mean by process intensity is the degree of highly-repetitive and rather primitive operations. At the upper left, are dedicated functions like A/D converters and DDCs that require specialized hardware structures to complete the operations in real time. ASICs are usually chosen for these functions.

Flexibility pertains to the uniqueness or variability of the processing and how likely the function may have to be changed or customized for any specific application. At the lower right are tasks like analysis and decision making which are highly variable and often subjective.

Programmable general-purpose processors or DSPs are usually chosen for these tasks since these tasks can be easily changed by software.

Now let's temporarily step away from the software radio tasks and take a deeper look at programmable logic devices.

Early Roles for FPGAs

- Used primarily to replace discrete digital hardware circuitry for:
  - Control logic
  - Glue logic
  - Registers and gates
  - State machines
  - Counters and dividers
- Devices were selected by hardware engineers
- Programmed functions were seldom changed after the design went into production

Figure 21

Legacy FPGA Design Methodologies

- Tools were oriented to hardware engineers
  - Schematic processors
  - Boolean processors
  - Gates, registers, counters, multipliers
- Successful designs required high-level hardware engineering skills for:
  - Critical paths and propagation delays
  - Pin assignment and pin locking
  - Signal loading and drive capabilities
  - Clock distribution
  - Input signal synchronization and skew analysis

Figure 22

As true programmable gate functions became available in the 1970's, they were used extensively by hardware engineers to replace control logic, registers, gates, and state machines which otherwise would have required many discrete, dedicated ICs.

Often these programmable logic devices were one-time factory-programmed parts that were soldered down and never changed after the design went into production.

These programmable logic devices were mostly the domain of hardware engineers and the software tools were tailored to meet their needs. You had tools for accepting boolean equations or even schematics to help generate the interconnect pattern for the growing number of gates.

Then, programmable logic vendors started offering predefined logic blocks for flip-flops, registers and counters that gave the engineer a leg up on popular hardware functions.

Nevertheless, the hardware engineer was still intimately involved with testing and evaluating the design using the same skills he needed for testing discrete logic designs. He had to worry about propagation delays, loading, clocking and synchronizing—all tricky problems that usually had to be solved the hard way—with oscilloscopes or logic analyzers.

Technology

FPGAs: New Device Technology

- 500+ MHz DSP Slices and Memory Structures
- Over 1000 dedicated on-chip hardware multipliers
- On-board GHz Serial Transceivers
- Partial Reconfigurability Maintains Operation During Changes
- Switched Fabric Interface Engines
- Over 330,000 Logic Cells
- Gigabit Ethernet media access controllers
- On-chip 405 PowerPC RISC micro-controller cores
- Memory densities approaching 15 million bits
- Reduced power with core voltages at 1 volt
- Silicon geometries to 65 nanometers
- High-density BGA and flip-chip packaging
- Over 1200 user I/O pins
- Configurable logic and I/O interface standards

Figure 23

FPGAs: New Development Tools

- High Level Design Tools
  - Block Diagram System Generators
  - Schematic Processors
  - High-level language compilers for VHDL & Verilog
  - Advanced simulation tools for modeling speed, propagation delays, skew and board layout
  - Faster compilers and simulators save time
  - Graphically-oriented debugging tools
- IP (Intellectual Property) Cores
  - FPGA vendors offer both free and licensed cores
  - FPGA vendors promote third party core vendors
  - Wide range of IP cores available

Figure 24

It's virtually impossible to keep up to date on FPGA technology, since new advancements are being made every day.

The hottest features are processor cores inside the chip, computation clocks to 500 MHz and above, and lower core voltages to keep power and heat down.

About five years ago, dedicated hardware multipliers started appearing and now you'll find literally hundreds of them on-chip as part of the DSP initiative launched by virtually all FPGA vendors.

High memory densities coupled with very flexible memory structures meet a wide range of data flow strategies. Logic slices with the equivalent of over ten million gates result from silicon geometries shrinking down to 0.1 micron.

BGA and flip-chip packages provide plenty of I/O pins to support on-board gigabit serial transceivers and other user-configurable system interfaces.

New announcements seem to be coming out every day from chip vendors like Xilinx and Altera in a never-ending game of outperforming the competition.

To support such powerful devices, new design tools are appearing that now open up FPGAs to both hardware and software engineers. Instead of just accepting logic equations and schematics, these new tools accept entire block diagrams as well as VHDL and Verilog definitions.

Choosing the best FPGA vendor often hinges heavily on the quality of the design tools available to support the parts.

Excellent simulation and modeling tools help to quickly analyze worst case propagation delays and suggest alternate routing strategies to minimize them within the part. This minimizes some of the tricky timing work for hardware engineers and can save one hours of tedious troubleshooting during design verification and production testing.

In the last few years, a new industry of third party IP (Intellectual Property) core vendors now offer thousands of application-specific algorithms. These are ready to drop into the FPGA design process to help beat the time-to-market crunch and to minimize risk.

Technology

FPGAs for SDR

- Parallel Processing
- Hardware Multipliers for DSP
  - FPGAs can now have over 500 hardware multipliers
- Flexible Memory Structures
  - Dual port RAM, FIFOs, shift registers, look up tables, etc.
- Parallel and Pipelined Data Flow
  - Systolic simultaneous data movement
- Flexible I/O
  - Supports a variety of devices, buses and interface standards
- High Speed
- Available IP cores optimized for special functions

Figure 25

FPGAs Bridge the SDR Application Space

Figure 26

Like ASICs, all the logic elements in FPGAs can execute in parallel. This includes the hardware multipliers, and you can now get over 1000 of them on a single FPGA.

This is in sharp contrast to programmable DSPs, which normally have just a handful of multipliers that must be operated sequentially.

FPGA memory can now be configured with the design tool to implement just the right structure for tasks that include dual port RAM, FIFOs, shift registers and other popular memory types.

These memories can be distributed along the signal path or interspersed with the multipliers and math blocks, so that the whole signal processing task operates in parallel in a systolic pipelined fashion.

Again, this is dramatically different from sequential execution and data fetches from external memory as in a programmable DSP.

As we said, FPGAs now have specialized serial and parallel interfaces to match requirements for high-speed peripherals and buses.

As a result, FPGAs have significantly invaded the application task space as shown by the center bubble in the task diagram above.

They offer the advantages of parallel hardware to handle some of the high process-intensity functions like DDCs and the benefit of programmability to accommodate some of the decoding and analysis functions of DSPs.

These advantages may come at the expense of increased power dissipation and increased product costs. However, these considerations are often secondary to the performance and capabilities of these remarkable devices.

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Technology

Typical Pentek Products with Installed SDR IP Cores

Model / Feature	7141-430	7141-420	7142-428	7151	7152	7153
Input Channels	1	2	4	4	4	4
Max Sample Rate	125 MHz	125 MHz	125 MHz	200 MHz	200 MHz	200 MHz
Input Resolution	14-Bit	14-Bit	14-Bit	16-Bit	16-Bit	16-Bit
DDC Channels	256	2 or 4	4	256	32	2 or 4
Decimation Range	1K-10K	Core: 2,4,8,16,32,64 GC4016: 32to 16k	2 to 64K Steps of 1	128 to 1024 Steps of 64	16 to 8192 Steps of 8	2 Ch: 2 to 65536 4 Ch: 2 to 256
No. of Filter Taps	24*DEC/512	Core: 28*DEC	28*DEC	24*DEC/64	28*DEC/8	28*DEC
Power Meters	None	None	None	None	32	2 or 4
Thresh Detectors	None	None	None	None	32	2 or 4
Channel Summers	None	None	None	None	32 channels	2 or 4 channels
Output Format	Normal I/Q	I/Q, Offset, Inverse, Real	I/Q, Offset, Inverse	I/Q, Offset, Inverse	I/Q, Offset, Inverse	I/Q, Offset, Inverse
Output Resolution	16-Bit	16-Bit, 24-Bit	16-Bit, 24-Bit	16-Bit, 24-Bit	16-Bit, 24-Bit	16-Bit, 24-Bit
Tuning Frequency	32-bits - 0 to Fs	32-bits - 0 to Fs	32-bits - 0 to Fs	32-bits - 0 to Fs	32-bits - 0 to Fs	32-bits - 0 to Fs
Phase Offset	-	32-bits ± 180 deg	32-bits ± 180 deg	32-bits ± 180 deg	32-bits ± 180 deg	32-bits ± 180 deg
Gain Control	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits
DAC Interpolation	None	2 - 32768	2 - 32768	None	None	None

Figure 27

The above chart shows the salient characteristics for some of Pentek's SDR products with IP cores installed in their FPGAs. The chart provides information regarding the number of input channels, maximum sampling frequency of their A/Ds, and number of DDC channels in each one. This information is followed by DDC characteristics regarding the decimation range and available steps along with the output format and resolution.

Other information that's specific to each core is included as well as an indication of the Models that include an interpolation filter and output D/A. As shown in the chart, some of these Models include power meters, threshold detectors, and gain along with phase offset control for optimizing results in applications such as direction-finding and beamforming.

All the Models shown here are PMC or PMC/XMC modules. These products are also available in PCI, cPCI and PCIe formats as well.

Technology

FPGA Resource Comparison

	Virtex-II Pro VP50, VP70	Virtex-4 FX, LX, SX	Virtex-5 FXT, LXT, SXT	Virtex-6 LXT, SXT
Logic Cells	53K–74K	41K–152K	46K–156K	128K–476K
Slices*	24K–33K	18K–68K	7K–24K	20K–74K
CLB Flip-Flops	47K–66K	49K–93K	150K–207K	160K–595K
Block RAM (kb)	4,176–5,904	1,728–6,768	2,160–8,784	9,504–38,304
DSP Hard IP	18x18 Multipliers	DSP48	DSP48E	DSP48E
DSP Slices	132–328	64–512	48–640	480–2,016
Serial Gbit Transceivers	–	0–20	12–16	20
PCI Express Blocks	–	–	–	2
SelectIO	–	448–768	480–640	600

*Virtex-II Pro and Virtex-4 Slices actually require 2.25 Logic Cells;
Virtex-5 and Virtex-6 Slices actually require 6.4 Logic Cells

Figure 28

The above chart compares the available resources in the four Xilinx FPGA families that are used in most of the Pentek products.
- Virtex-II Pro: VP50 and VP70
- Virtex-4: FX, LX and SX
- Virtex-5: FXT, LXT and SXT
- Virtex-6: LXT and SXT

The Virtex-II family includes hardware multipliers that support digital filters, averagers, demodulators and FFTs—a major benefit for software radio signal processing. The Virtex-II Pro family dramatically increased the number of hardware multipliers and also added embedded PowerPC microcontrollers.

The Virtex-4 family is offered as three subfamilies that dramatically boost clock speeds and reduce power dissipation over previous generations.

The Virtex-4 LX family delivers maximum logic and I/O pins while the SX family boasts of 512 DSP slices for maximum DSP performance. The FX family is a generous mix of all resources and is the only family to offer RocketIO, PowerPC cores, and the newly added gigabit Ethernet ports.
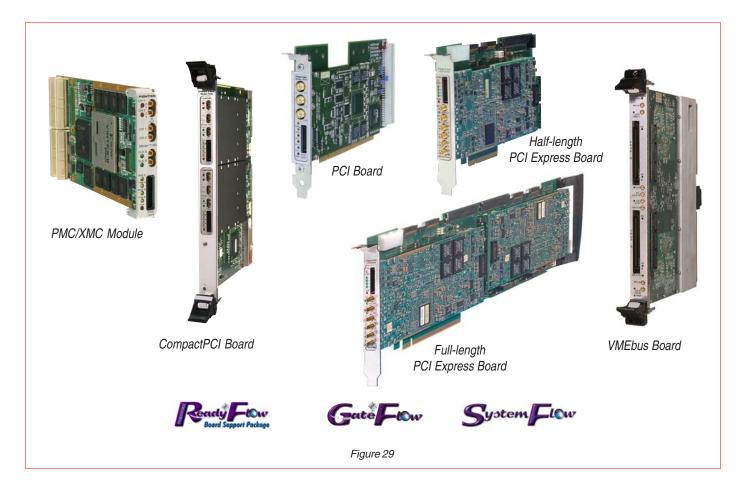
The Virtex-5 family LXT devices offer maximum logic resources, gigabit serial transceivers, and Ethernet media access controllers. The SXT devices push DSP capabilities with all of the same extras as the LXT. The FXT devices follow as the embedded system resource devices.

The Virtex-5 devices offer lower power dissipation, faster clock speeds and enhanced logic slices. They also improve the clocking features to handle faster memory and gigabit interfaces. They support faster single-ended and differential parallel I/O buses to handle faster peripheral devices.

The Virtex-6 devices offer higher density, more processing power, lower power consumption, and updated interface features to match the latest technology I/O requirements including PCI Express. Virtex-6 supports PCI Express 2.0 in x1 through x8 configurations.

The ample DSP slices are responsible for the majority of the processing power of the Virtex-6 family. Increases in operating speed from 500 MHz in V-4 to 550 MHz in V-5 to 600 MHz in V-6 and increasing density allows more DSP slices to be included in the same-size package. As shown in the chart, Virtex-6 tops out at an impressive 2016 DSP slices.

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Products

PMC, PMC/XMC, CompactPCI, PCI, PCI Express and VMEbus Software Radio

PMC/XMC Module

PCI Board

Half-length
PCI Express Board

CompactPCI Board

Full-length
PCI Express Board

VMEbus Board

Figure 29

The Pentek family of board-level software radio products is the most comprehensive in the industry. Most of these products are available in several formats to satisfy a wide range of requirements.

In addition to their commercial versions, many software radio products are available in ruggedized and conduction-cooled versions.

All of the software radio products include input A/D converters. Some of these products are software radio receivers in that they include only DDCs. Others are software radio transceivers and they include DDCs as well as DUCs with output D/A converters. These come with independent input and output clocks.

All Pentek software radio products include multiboard synchronization that facilitates the design of multichannel systems with synchronous clocking, gating and triggering.

Pentek's comprehensive software support includes the ReadyFlow® Board Support Package, the GateFlow® FPGA Design Kit and high-performance factory-installed IP cores that expand the features and range of many Pentek software radio products. In addition, Pentek software radio recording systems are supported with SystemFlow® recording software that features a graphical user interface.

A complete listing of these products with active links to their datasheets on Pentek's website is included at the end of this handbook.

Multiband Receivers

Model 7131 PMC • Model 7231 6U cPCI • Model 7331 3U cPCI • Model 7631A PCI

Model 7631A PCI

Model 7131 PMC

Model 7331 3U cPCI

Model 7231D 6U cPCI

Figure 30

The Model 7131, a 16-Channel Multiband Receiver, is a PMC module. The 7131 PMC may be attached to a wide range of industry processor platforms equipped with PMC sites.

Two 14-bit 105 MHz A/D Converters accept transformer-coupled RF inputs through two front panel SMA connectors. Both inputs are connected to four TI/GC4016 quad DDC chips, so that all 16 DDC channels can independently select either A/D.
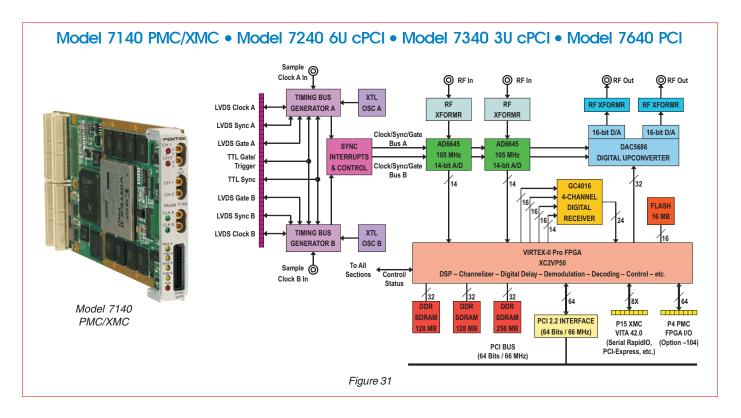
Four parallel outputs from the four DDCs deliver data into the Virtex-II FPGA which can be either the XC2V1000 or XC2V3000. The outputs of the two A/D converters are also connected directly to the FPGA to support the DDC bypass path to the PCI bus and for direct processing of the wideband A/D signals by the FPGA.

The unit supports the channel combining mode of the 4016s such that two or four individual 2.5 MHz channels can be combined for output bandwidths of 5 MHz or 10 MHz, respectively.

The sampling clock can be sourced from an internal 100 MHz crystal oscillator or from an external clock supplied through an SMA connector or the LVDS clock/sync bus on the front panel. The LVDS bus allows multiple modules to be synchronized with the same sample clock, gating, triggering and frequency switching signals. Up to 80 modules can be synchronized with the Model 9190 Clock and Sync Generator. Custom interfaces can be implemented by using the 64 user-defined FPGA I/O pins on the P4 connector.

Versions of the 7131 are also available as a PCI board (Model 7631A), 6U cPCI (Models 7231 and 7231D dual density), or 3U cPCI (Model 7331). All these products have similar features.

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Products

Multiband Transceivers with Virtex-II Pro FPGA

Model 7140 PMC/XMC • Model 7240 6U cPCI • Model 7340 3U cPCI • Model 7640 PCI

Model 7140 PMC/XMC

Figure 31

The Model 7140 PMC module combines both receive and transmit capability with a high-performance Virtex II-Pro FPGA and supports the VITA 42 XMC standard with optional switched fabric interfaces for high-speed I/O.

The front end of the module accepts two RF inputs and transformer-couples them into two 14-bit A/D converters running at 105 MHz. The digitized output signals pass to a Virtex-II Pro FPGA for signal processing or routing to other module resources.

These resources include a quad digital down-converter, a digital upconverter with dual D/A converters, 512 MB DDR SDRAM delay memory and the PCI bus. The FPGA also serves as a control and status engine with data and programming interfaces to each of the on-board resources. Factory-installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering, and SDRAM memory control.
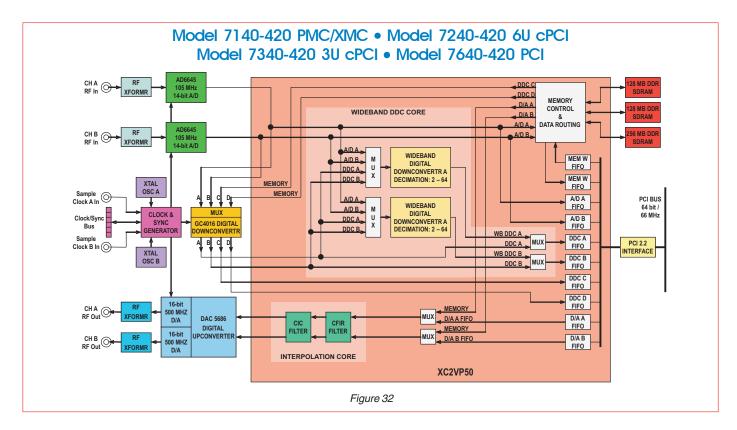
In addition to acting as a simple transceiver, the module can perform user-defined DSP functions on the baseband signals, developed using Pentek's GateFlow and ReadyFlow development tools.

The module includes a TI/GC4016 quad digital downconverter along with a TI DAC5686 digital upconverter with dual D/A converters.

Each channel in the downconverter can be set with an independent tuning frequency and bandwidth. The upconverter translates a real or complex baseband signal to any IF center frequency from DC to 160 MHz and can deliver real or complex (I + Q) analog outputs through its two 16-bit D/A converters. The digital upconverter can be bypassed for two interpolated D/A outputs with sampling rates to 500 MHz.

Versions of the 7140 are also available as a PCI board (Model 7640), 6U cPCI (Models 7240 and 7240D dual density), or 3U cPCI (Model 7340). All these products have similar features.

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Transceivers with Dual Wideband DDC and Interpolation Filter Installed Cores

Model 7140-420 PMC/XMC • Model 7240-420 6U cPCI
Model 7340-420 3U cPCI • Model 7640-420 PCI

Figure 32

The Pentek IP Core 420 includes a dual high-performance wideband DDC and an interpolation filter. Factory-installed in the Model 7140 FPGA, they extend the range of both the GC4016 ASIC DDC and the DAC5686 DUC.

Like the GC4016, each of the core 420 DDCs translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter removes any out-of-band frequency components. An output decimator and formatter deliver either complex or real data. An input gain block scales both I and Q data streams by a 16-bit gain term.

The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent sets of 18-bit coefficients for each decimation value. These coefficients are user-programmable by using RAM structures within the FPGA.
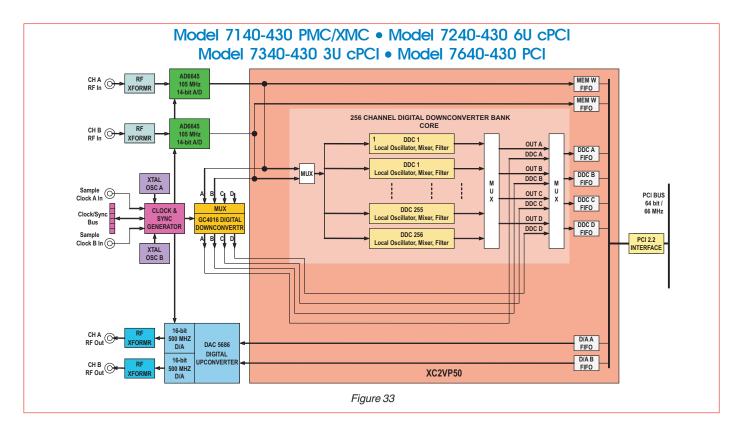
The decimation settings of 2, 4, 8, 16, 32, and 64 provide output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling of 100 MHz. A multiplexer in front of the Core 420 DDCs allows data to be sourced from either the A/Ds or the GC4016, extending the maximum cascaded decimation range to 1,048,576.

The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 32,768 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 32,768 which is comparable to the maximum decimation of the GC4016 narrowband DDC.

In addition to the Core 420, all the standard features of the 7140 are retained.

Versions of the 7140-420 are also available as a PCI board (Model 7640-420), 6U cPCI (Models 7240-420 and 7240D-420 dual density), or 3U cPCI (Model 7340-420). All these products have similar features.

Products

Transceivers with 256-Channel Narrowband DDC Installed Core

Model 7140-430 PMC/XMC • Model 7240-430 6U cPCI
Model 7340-430 3U cPCI • Model 7640-430 PCI

Figure 33

For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-channel digital downconverter bank. Factory installed in the Model 7140 FPGA, Core 430 creates a flexible, very high-channel count receiver system in a small footprint.

Unlike classic channelizer methods, the Pentek 430 core allows for completely independent programmable tuning of each individual channel with 32-bit resolution as well as filter characteristics comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 8192 in steps of 256, and 18-bit user programmable FIR decimating filter coefficients for the DDCs. Default DDC filter coefficient sets are included with the core for all possible decimation settings.

Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequen-
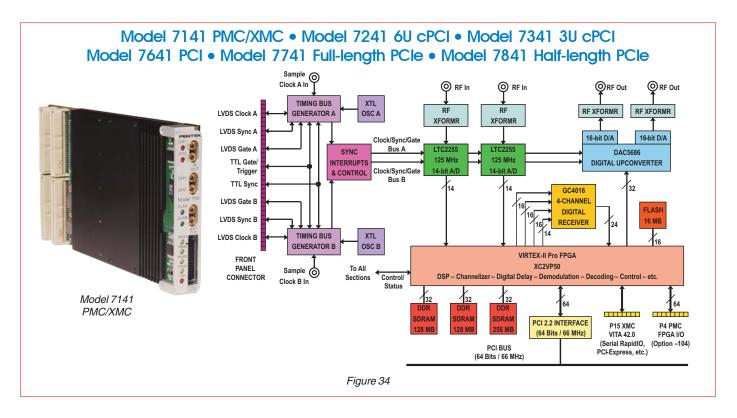
cies need not be at fixed intervals, and are independently programmable to any value.

Core 430 DDC comes factory installed in the Model 7140-430. A multiplexer in front of the core allows data to be sourced from either A/D converter A or B. At the output, a multiplexer allows the 7140-430 to route either the output of the GC4016 or the Core 430 DDC to the PCI Bus.

In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any integer value between 1 and 4096. A TI DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 40 MHz.

Versions of the 7140-430 are also available as a PCI board (Model 7640-430), 6U cPCI (Models 7240-430 and 7240D-430 dual density), or 3U cPCI (Model 7340-430). All these products have similar features.

Multiband Transceivers with Virtex-II Pro FPGA

Model 7141 PMC/XMC • Model 7241 6U cPCI • Model 7341 3U cPCI
Model 7641 PCI • Model 7741 Full-length PCIe • Model 7841 Half-length PCIe

Model 7141
PMC/XMC

Figure 34

The Model 7141 PMC/XMC module combines both receive and transmit capabilities with a high-performance Virtex II-Pro FPGA and supports the VITA 42 XMC standard with optional switched fabric interfaces for high-speed I/O.

The front end of the module accepts two RF inputs and transformer-couples them into two 14-bit A/D converters running at 125 MHz. The digitized output signals pass to a Virtex-II Pro FPGA for signal processing or routing to other module resources.

These resources include a quad digital down-converter, a digital upconverter with dual D/A converters, 512 MB DDR SDRAM delay memory and the PCI bus. The FPGA also serves as a control and status engine with data and programming interfaces to each of the on-board resources. Factory-installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering, and SDRAM memory control.

In addition to acting as a simple transceiver, the module can perform user-defined DSP functions on the baseband signals, developed using Pentek's GateFlow and ReadyFlow development tools.
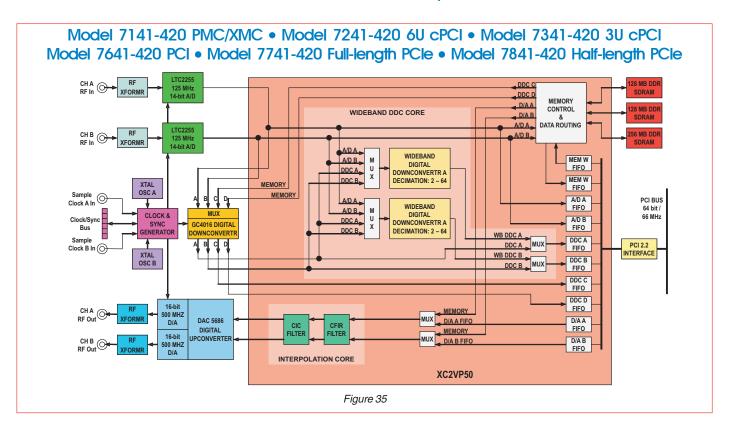
The module includes a TI/GC4016 quad digital downconverter along with a TI DAC5686 digital upconverter with dual D/A converters.

Each channel in the downconverter can be set with an independent tuning frequency and bandwidth. The upconverter translates a real or complex baseband signal to any IF center frequency from DC to 160 MHz and can deliver real or complex (I + Q) analog outputs through its two 16-bit D/A converters. The digital upconverter can be bypassed for two interpolated D/A outputs with sampling rates to 500 MHz.

Versions of the 7141 are also available as a PCIe full-length board (Models 7741 and 7741D dual density), PCIe half-length board (Model 7841), PCI board (Model 7641), 6U cPCI (Models 7241 and 7241D dual density), and 3U cPCI (Model 7341).

Model 7141-703 is a conduction-cooled version.

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Products

Transceivers with Dual Wideband DDC and Interpolation Filter Installed Cores

Model 7141-420 PMC/XMC • Model 7241-420 6U cPCI • Model 7341-420 3U cPCI
Model 7641-420 PCI • Model 7741-420 Full-length PCIe • Model 7841-420 Half-length PCIe

Figure 35

The Pentek IP Core 420 includes a dual high-performance wideband DDC and an interpolation filter. Factory-installed in the Model 7141 FPGA, they extend the range of both the GC4016 ASIC DDC and the DAC5686 DUC.

Each of the core 420 DDCs translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter removes any out-of-band frequency components. An output decimator and formatter deliver either complex or real data. An input gain block scales both I and Q data streams by a 16-bit gain term.

The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent sets of 18-bit coefficients for each decimation value. These coefficients are user-programmable by using RAM structures within the FPGA.
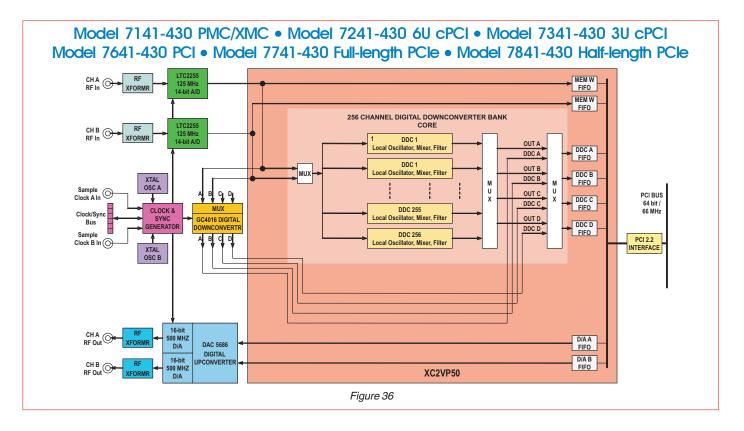
The decimation settings of 2, 4, 8, 16, 32, and 64 provide output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling of 100 MHz. A multiplexer in front of the Core 420 DDCs allows data to be sourced from either the A/Ds or the GC4016, extending the maximum cascaded decimation range to 1,048,576.

The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 32,768 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 32,768 which is comparable to the maximum decimation of the GC4016 narrowband DDC.

Versions of the 7141-420 are also available as a PCIe full-length board (Models 7741-420 and 7741D-420 dual density), PCIe half-length board (Model 7841-420), PCI board (Model 7641-420), 6U cPCI (Models 7241-420 and 7241D-420 dual density), or 3U cPCI (Model 7341-420).

Model 7141-703-420 is a conduction-cooled version.

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Products

Transceivers with 256-Channel Narrowband DDC Installed Core

Model 7141-430 PMC/XMC • Model 7241-430 6U cPCI • Model 7341-430 3U cPCI
Model 7641-430 PCI • Model 7741-430 Full-length PCIe • Model 7841-430 Half-length PCIe

Figure 36

For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-channel digital downconverter bank. Factory installed in the Model 7141 FPGA, Core 430 creates a flexible, very high-channel count receiver system in a small footprint.

Unlike classic channelizer methods, the Pentek 430 core allows for completely independent programmable tuning of each individual channel with 32-bit resolution as well as filter characteristics comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 8192 in steps of 256, and 18-bit user programmable FIR decimating filter coefficients for the DDCs. Default DDC filter coefficient sets are included with the core for all possible decimation settings.

Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequen-
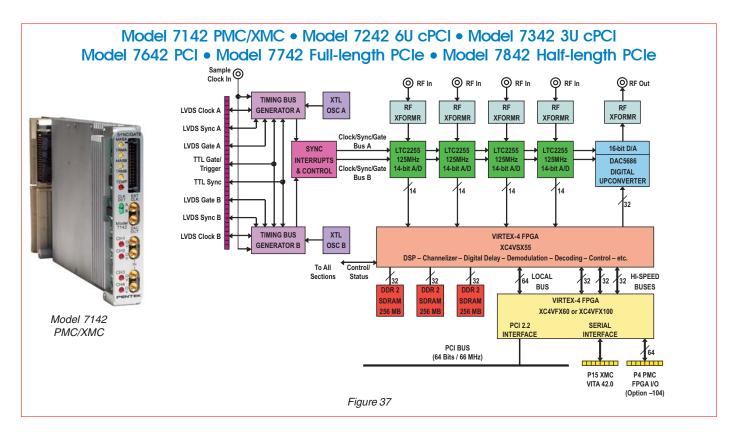
cies need not be at fixed intervals, and are independently programmable to any value.

Core 430 DDC comes factory installed in the Model 7141-430. A multiplexer in front of the core allows data to be sourced from either A/D converter A or B. At the output, a multiplexer allows the 7141-430 to route either the output of the GC4016 or the Core 430 DDC to the PCI Bus.

In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any integer value between 1 and 4096. A TI DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 50 MHz.

Versions of the 7141-430 are also available as a PCIe full-length board (Models 7741-430 and 7741D-430 dual density), PCIe half-length board (Model 7841-430), PCI board (Model 7641-430), 6U cPCI (Models 7241-430 and 7241D-430 dual density), or 3U cPCI (Model 7341-430). Model 7141-703-430 is a conduction-cooled version.

Products

Multichannel Transceivers with Virtex-4 FPGAs

Model 7142 PMC/XMC • Model 7242 6U cPCI • Model 7342 3U cPCI
Model 7642 PCI • Model 7742 Full-length PCIe • Model 7842 Half-length PCIe

Model 7142 PMC/XMC

Figure 37

The Model 7142 is a Multichannel PMC/XMC module. It includes four 125 MHz 14-bit A/D converters and one upconverter with a 500 MHz 16-bit D/A converter to support wideband receive and transmit communication channels.

Two Xilinx Virtex-4 FPGAs are included: an XC4VSX55 or LX100 and an XC4VFX60 or FX100. The first FPGA is used for control and signal processing functions, while the second one is used for implementing board interface functions including the XMC interface.

It also features 768 MB of SDRAM for implementing up to 2.0 sec of transient capture or digital delay memory for signal intelligence tracking applications at 125 MHz.

A 16 MB flash memory supports the boot code for the two on-board IBM 405 PowerPC microcontroller cores within the FPGA.

A 9-channel DMA controller and 64 bit / 66 MHz PCI interface assures efficient transfers to and from the module.
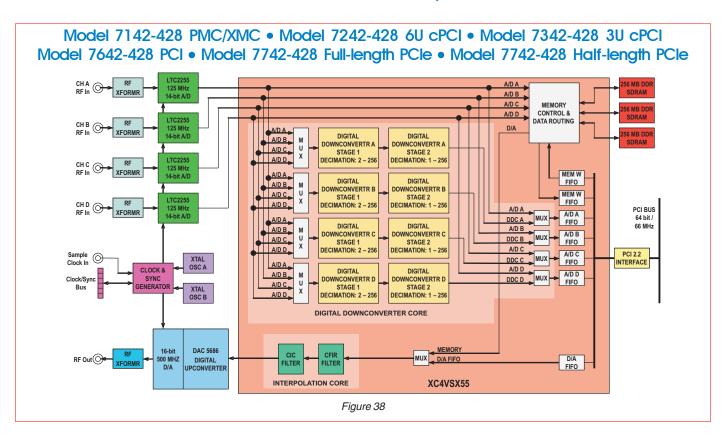
A high-performance 160 MHz IP core wideband digital downconverter may be factory-installed in the first FPGA.

Two 4X switched serial ports, implemented with the Xilinx Rocket I/O interfaces, connect the second FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows separate clocks, gates and synchronization signals for the A/D and D/A converters. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7142 are also available as a PCIe full-length board (Models 7742 and 7742D dual density), PCIe half-length board (Model 7842), PCI board (Model 7642), 6U cPCI (Models 7242 and 7242D dual density), and 3U cPCI (Model 7342).

Products

Transceivers with Four Multiband DDCs and Interpolation Filter Installed Cores

Model 7142-428 PMC/XMC • Model 7242-428 6U cPCI • Model 7342-428 3U cPCI
Model 7642-428 PCI • Model 7742-428 Full-length PCIe • Model 7742-428 Half-length PCIe

Figure 38

The Pentek IP Core 428 includes four high-performance multiband DDCs and an interpolation filter. Factory-installed in the Model 7142 FPGA, they add DDCs to the Model 7142 and extend the range of its DAC5686 DUC.

The Core 428 downconverter translates any frequency band within the input bandwidth range down to zero frequency. The DDCs consist of two cascaded decimating FIR filters. The decimation of each DDC can be set independently. After each filter stage is a post filter gain stage. This gain may be used to amplify small signals after out-of-band signals have been filtered out.
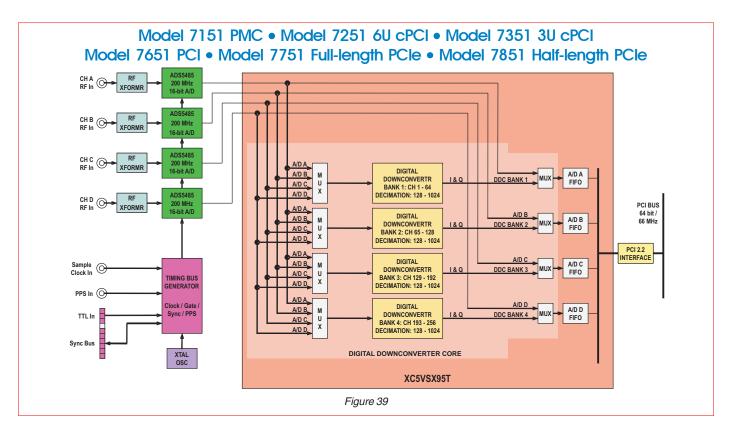
The NCO provides over 108 dB spurious-free dynamic range (SFDR). The FIR filter is capable of storing and utilizing two independent sets of 18-bit coefficients. These coefficients are user-programmable by using RAM structures within the FPGA. NCO tuning frequency, decimation and filter coefficients can be changed dynamically.

Four identical Core 428 DDCs are factory installed in the 7142-428 FPGA. An input multiplexer allows any DDC to independently select any of the four A/D sources. The overal decimation range from 2 to 65,536, programmable in steps of 1, provides output bandwidths from 50 MHz down to 1.52 kHz for an A/D sampling rate of 125 MHz and assuming an 80% filter.

The Core 428 interpolation filter increases the sampling rate of real or complex baseband signals by a factor of 16 to 2048, programmable in steps of 4, and relieves the host processor from performing upsampling tasks. The interpolation filter can be used in series with the DUC's built-in interpolation, creating a maximum interpolation factor of 32,768.

Versions of the 7142-428 are also available as a PCIe full-length board (Models 7742-428 and 7742D-428 dual density), PCIe half-length board (Model 7842-428), PCI board (Model 7642-428), 6U cPCI (Models 7242-428 and 7242D-428 dual density), or 3U cPCI (Model 7342-428).

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256-Channel DDC Installed Core with Quad 200 MHz, 16-bit A/D

Figure 39

The Model 7151 PMC module is a 4-channel high-speed digitizer with a factory-installed 256-channel DDC core. The front end of the module accepts four RF inputs and transformer-couples them into four 16-bit A/D converters running at 200 MHz. The digitized output signals pass to a Virtex-5 FPGA for routing, formatting and DDC signal processing.

The Model 7151 employs an advanced FPGA-based digital downconverter engine consisting of four identical 64-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. Each of the 256 DDCs has an independent 32-bit tuning frequency setting.

All of the 64 channels within a bank share a common decimation setting that can range from 128 to 1024, programmable in steps of 64. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 156.25 kHz to 1.25 MHz. Each 64-channel bank can have its own unique decimation setting
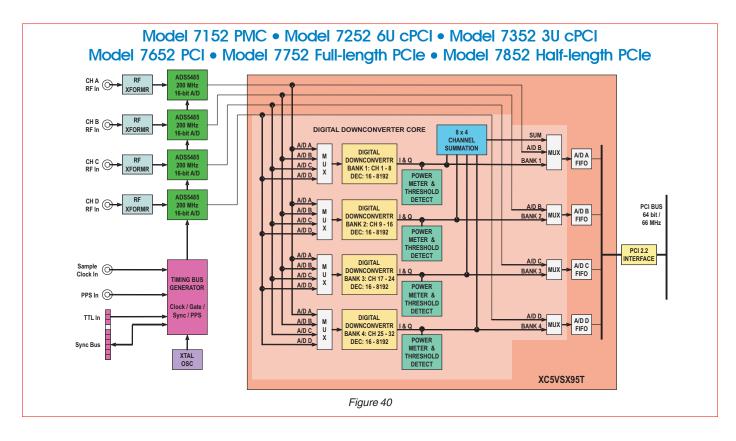
supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples. Any number of channels can be enabled within each bank, selectable from 0 to 64. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Versions of the 7151 are also available as a PCIe full-length board (Models 7751 and 7751D dual density), PCIe half-length board (Model 7851), PCI board (Model 7651), 6U cPCI (Models 7251 and 7251D dual density), or 3U cPCI (Model 7351).

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Products

32-Channel DDC Installed Core with Quad 200 MHz, 16-bit A/D

Model 7152 PMC • Model 7252 6U cPCI • Model 7352 3U cPCI
Model 7652 PCI • Model 7752 Full-length PCIe • Model 7852 Half-length PCIe

Figure 40

The Model 7152 PMC module is a 4-channel high-speed digitizer with a factory-installed 32-channel DDC core. The front end of the module accepts four RF inputs and transformer-couples them into four 16-bit A/D converters running at 200 MHz. The digitized output signals pass to a Virtex-5 FPGA for routing, formatting and DDC signal processing.

The Model 7152 employs an advanced FPGA-based digital downconverter engine consisting of four identical 8-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. Each of the 32 DDCs has an independent 32-bit tuning frequency setting.

All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can
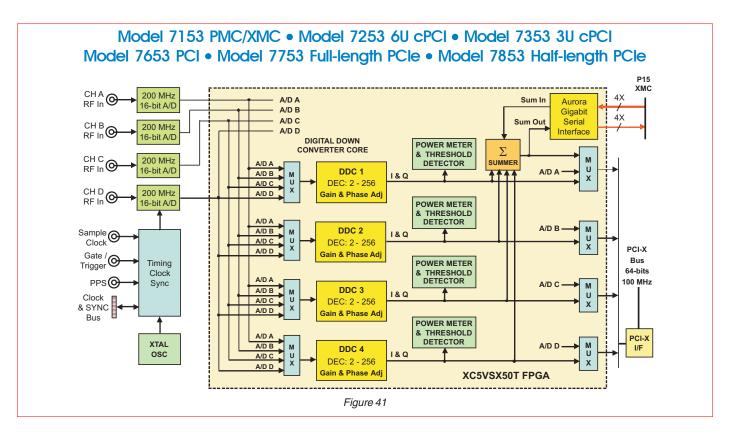
have its own unique decimation setting supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output band-width is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank. Gain and phase control, power meters and threshold detectors are included.

Versions of the 7152 are also available as a PCIe full-length board (Models 7752 and 7752D dual density), PCIe half-length board (Model 7852), PCI board (Model 7652), 6U cPCI (Models 7252 and 7252D dual density), or 3U cPCI (Model 7352).

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4-Channel Beamformer Installed Core with four 200 MHz, 16-bit A/Ds

Model 7153 PMC/XMC • Model 7253 6U cPCI • Model 7353 3U cPCI
Model 7653 PCI • Model 7753 Full-length PCIe • Model 7853 Half-length PCIe

Figure 41

Model 7153 is a 4-channel, high-speed software radio module designed for processing baseband RF or IF signals. It features four 200 MHz 16-bit A/Ds supported by a high-performance 4-channel DDC (digital downconverter) installed core and a complete set of beamforming functions. With built-in multiboard synchronization and an Aurora gigabit serial interface, it provides everything needed for implementing multichannel beamforming systems.

The Model 7153 employs an advanced FPGA-based DDC engine consisting of four identical multiband banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. Each of the 4 DDCs has an independent 32-bit tuning frequency setting.
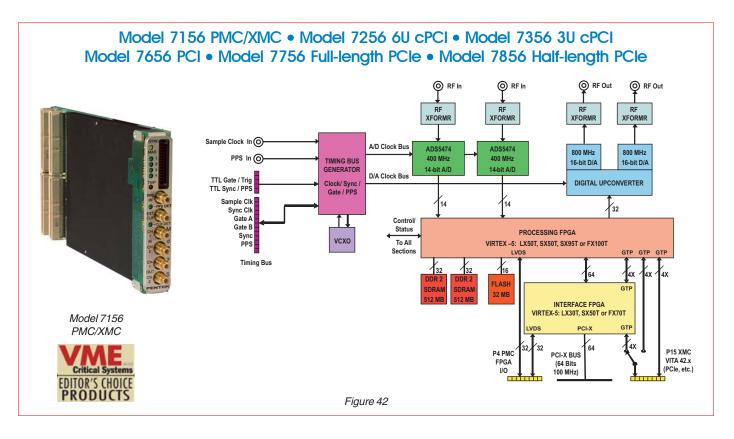
All four DDCs have a decimation setting that can range from 2 to 256, programmable independently in steps of 1. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of

$0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output band-width is better than 100 dB.

In addition to the DDCs, the 7153 features a complete beamforming subsystem. Each channel contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8 ksamples. The power meters present average power measurements for each channel in easy-to-read registers. Each channel also includes a threshold detector that sends an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold.

Versions of the 7153 are also available as a PCIe full-length board (Models 7753 and 7753D dual density), PCIe half-length board (Model 7853), PCI board (Model 7653), 6U cPCI (Models 7253 and 7253D dual density), or 3U cPCI (Model 7353).

Dual SDR Transceivers with 400 MHz A/D, 800 MHz D/A, and Virtex-5 FPGAs

Model 7156 PMC/XMC • Model 7256 6U cPCI • Model 7356 3U cPCI
Model 7656 PCI • Model 7756 Full-length PCIe • Model 7856 Half-length PCIe

Model 7156 PMC/XMC

Figure 42

Model 7156 is a dual high-speed data converter suitable for connection as the HF or IF input of a communications system. It features two 400 MHz 14-bit A/Ds, a DUC with two 800 MHz 16-bit D/As, and two Virtex-5 FPGAs. Model 7156 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

The Model 7156 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions such as data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Two independent 512 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface.

A high-performance IP core wideband DDC may be factory-installed in the processing FPGA.
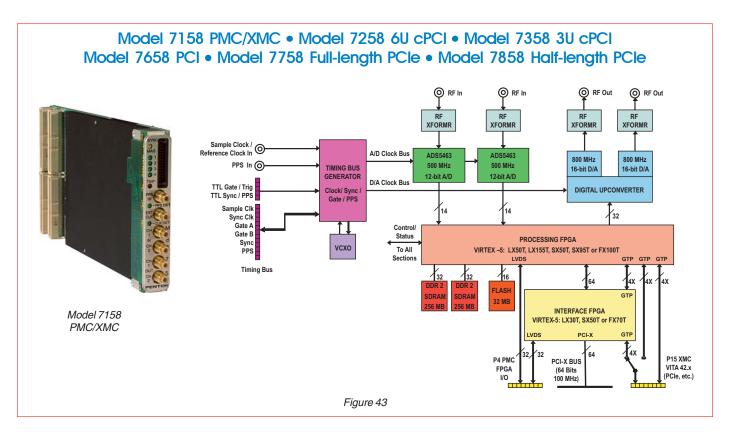
A 5-channel DMA controller and 64 bit/100 MHz PCI-X interface assures efficient transfers to and from the module.

Two 4X switched serial ports implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows separate clocks, gates and synchronization signals for the A/D and D/A converters. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7156 are also available as a PCIe full-length board (Models 7756 and 7756D dual density), PCIe half-length board (Model 7856), PCI board (Model 7656), 6U cPCI (Models 7256 and 7256D dual density), or 3U cPCI (Model 7356). All these products have similar features.

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Products

Dual SDR Transceivers with 500 MHz A/D, 800 MHz D/A, and Virtex-5 FPGAs

Model 7158 PMC/XMC • Model 7258 6U cPCI • Model 7358 3U cPCI
Model 7658 PCI • Model 7758 Full-length PCIe • Model 7858 Half-length PCIe

Model 7158 PMC/XMC

Figure 43

Model 7158 is a dual high-speed data converter suitable for connection as the HF or IF input of a communications system. It features two 500 MHz 12-bit A/Ds, a digital upconverter with two 800 MHz 16-bit D/As, and two Virtex-5 FPGAs. Model 7158 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

The Model 7158 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions such as data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Two independent 256 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface.
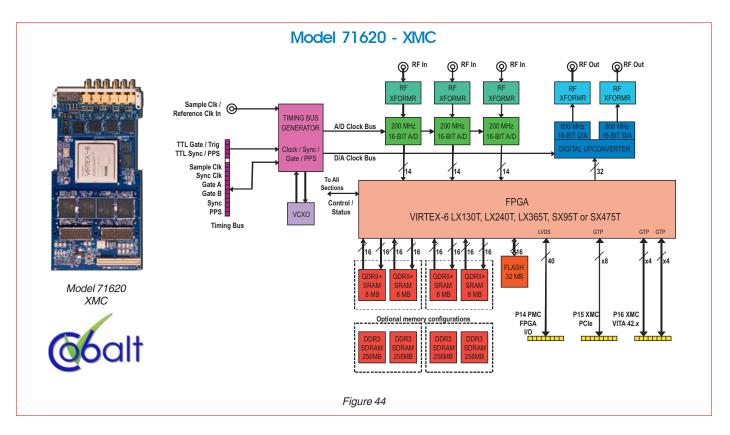
A 5-channel DMA controller and 64 bit / 100 MHz PCI-X interface assures efficient transfers to and from the module.

Two 4X switched serial ports implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows separate clocks, gates and synchronization signals for the A/D and D/A converters. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7158 are also available as a PCIe full-length board (Models 7758 and 7758D dual density), PCIe half-length board (Model 7858), PCI board (Model 7658), 6U cPCI (Models 7258 and 7258D dual density), or 3U cPCI (Model 7358). All these products have similar features.

Products

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA

Figure 44

Model 71620 is the first member of the Cobalt™ family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications and radar system. It includes three 200 MHz, 16-bit A/Ds, one DUC, two 800 MHz 16-bit D/As, and four banks of memory. The Model 71620 is compatible with the VITA 42.0 XMC format and supports PCI Express Gen. 2.

The Model 71620 Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

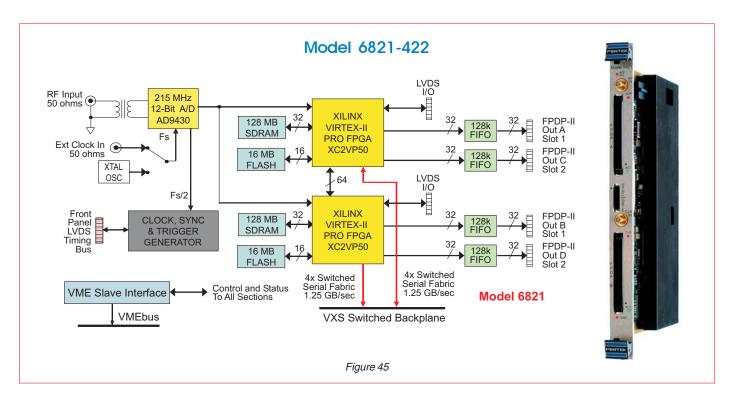The FPGA serves as a control and status engine with data and programming interfaces to each of the on-board

resources including the data converters, DDR3 SDRAM or QDRII+ SRAM memory, PCIe interface, programmable LVDS I/O and clock, gate, and synchronization circuits. The FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-6 LX130T, LX240T, LX365T, SX315T, or SX475T.

Multiple 71620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

The 71620 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

The Model 71620 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

33

Products

215 MHz, 12-bit A/D with Wideband DDCs - VME/VXS

Figure 45

The Model 6821 is a 6U single slot board with the AD9430 12-bit, 215 MHz A/D converter.

Capable of digitizing input signal bandwidths up to 100 MHz, it is ideal for wideband applications including radar and spread spectrum communication systems.

The sampling clock can be supplied either from a front panel input or from an internal crystal oscillator. Data from the A/D converter flows into two Xilinx Virtex-II Pro FPGAs where optional signal processing functions can be performed. The size of the FPGAs can range from the XC2VP20 to the XC2VP50.

Because the sampling rate is well beyond conventional ASIC digital downconverters, none are included on the board.

Instead, the Pentek GateFlow IP Core 422 Ultra Wideband Digital Downconverter can be factory-

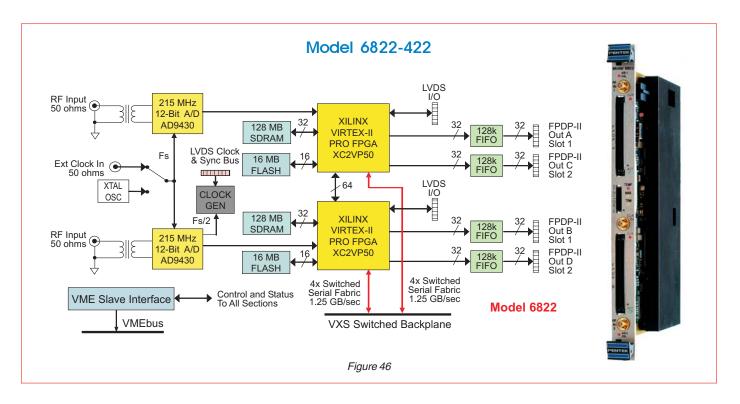installed in one or both of the FPGAs to perform this function.

Two 128 MB SDRAMs, one for each FPGA, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGAs to external digital destinations such as processor boards, memory boards or storage devices.

A VMEbus interface supports configuration of the FPGAs over the backplane and also provides data and control paths for runtime applications. A VXS interface is optionally available.

This Model is available in commercial as well as conduction-cooled versions.

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Products

Dual 215 MHz, 12-bit A/D with Wideband DDCs - VME/VXS

Model 6822-422

Figure 46

The Model 6822 is a 6U single slot VME board with two AD9430 12-bit 215 MHz A/D converters.

Capable of digitizing input signal bandwidths up to 100 MHz, it is ideal for wideband applications including radar and spread spectrum communication systems.

The sampling clock can be supplied either from a front panel input or from an internal crystal oscillator. Data from each A/D converter flows into a Xilinx Virtex-II Pro FPGA where optional signal processing functions can be performed. The size of the FPGAs can range from the XC2VP20 to the XC2VP50.

Because the sampling rate is well beyond conventional ASIC digital downconverters, none are included on the board.

Instead, the Pentek GateFlow IP Core 422 Ultra Wideband Digital Downconverter can be factory-installed in one or both of the FPGAs to perform this function.

Two 128 MB SDRAMs, one for each FPGA, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGAs to external digital destinations such as processor boards, memory boards or storage devices.
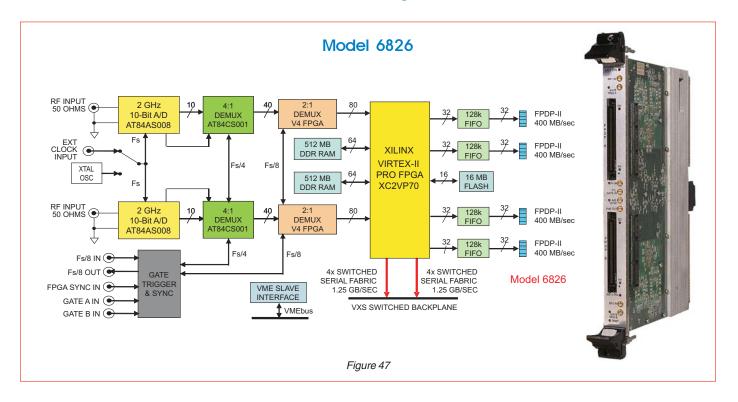
A VMEbus interface supports configuration of the FPGAs over the backplane and also provides data and control paths for runtime applications. A VXS interface is optionally available.

This Model is available in commercial as well as conduction-cooled versions.

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Products

Dual 2 GHz, 10-bit A/D with Very High-Speed DDCs - VME/VXS

Model 6826

Figure 47

The Model 6826 is a 6U single slot VME board with two Atmel AT84AS008 10-bit 2 GHz A/D converters.

Capable of digitizing input signals at sampling rates up to 2 GHz, it is ideal for extremely wideband applications including radar and spread spectrum communication systems. The sampling clock is an externally supplied sinusoidal clock at a frequency from 200 MHz to 2 GHz.

Data from each of the two A/D converters flows into an innovative dual-stage demultiplexer that packs groups of eight data samples into 80-bit words for delivery to the Xilinx Virtex-II Pro XC2VP70 FPGA at one eighth the sampling frequency. This advanced circuit features the Atmel AT84CS001 demultiplexer which represents a significant improvement over previous technology.

Because the sampling rate is well beyond conventional digital downconverters, none are included on the board. A very high-speed digital downconverter IP core

for the Model 6826 can be developed for a customer who is interested in one.

The customer will be able to incorporate this core into the Model 6826 by ordering it as a factory-installed option.
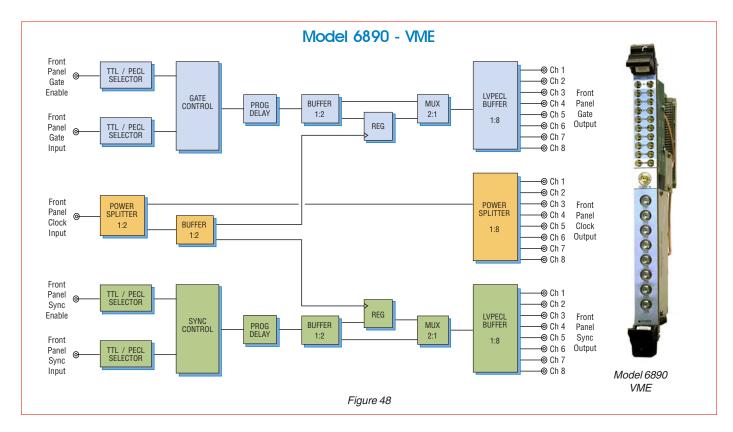
Two 512 MB or 1 GB SDRAMs, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGA to external digital destinations such as processor boards, memory boards or storage devices.

A VMEbus interface supports configuration of the FPGA over the backplane and also provides data and control paths for runtime applications. A VXS interface is optionally available.

This Model is also available in a single-channel version and in commercial as well as conduction-cooled versions.

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Products

2.2 GHz Clock, Sync and Gate Distribution Board

Model 6890 - VME

Figure 48

Model 6890 VME

Model 6890 Clock, Sync and Gate Distribution Board synchronizes multiple Pentek I/O boards within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications. Up to eight boards can be synchronized using the 6890, each receiving a common clock of up to 2.2 GHz along with timing signals that can be used for synchronizing, triggering and gating functions.

Clock signals are applied from an external source such as a high performance sine wave generator. Gate and sync signals can come from an external source, or from one supported board set to act as the master.

The 6890 accepts clock input at +10 dBm to +14 dBm with a frequency range from 800 MHz to 2.2 GHz and uses a 1:2 power splitter to distribute the clock. The first output of this power splitter sends the clock signal to a 1:8 splitter for distribution to up to eight boards using SMA connectors. The second output of the 1:2 power splitter feeds a 1:2 buffer which distributes the clock signal to both the gate and synchronization circuits.
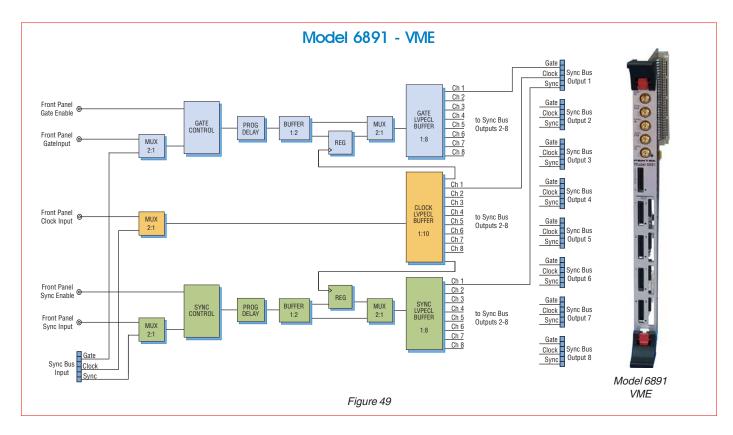
The 6890 features separate inputs for gate/trigger and sync signals with user-selectable polarity. Each of these inputs can be TTL or LVPECL. Separate Gate Enable and Sync Enable inputs allow the user to enable or disable these circuits using an external signal.

A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer. A bank of eight MMCX connectors at the output of each buffer delivers signals to up to eight boards.

A 2:1 multiplexer in each circuit allows the gate/trigger and sync signals to be registered with the input clock signal before output, if desired.

Sets of input and output cables for two to eight boards are available from Pentek.

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Products

System Synchronizer and Distribution Board

Model 6891 - VME

Figure 49

Model 6891
VME

Model 6891 System Synchronizer and Distribution Board synchronizes multiple Pentek I/O modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight modules can be synchronized using the 6891, each receiving a common clock up to 500 MHz along with timing signals that can be used for synchronizing, triggering and gating functions. For larger systems, up to eight 6891's can be linked together to provide synchronization for up to 64 I/O modules producing systems with up to 256 channels.
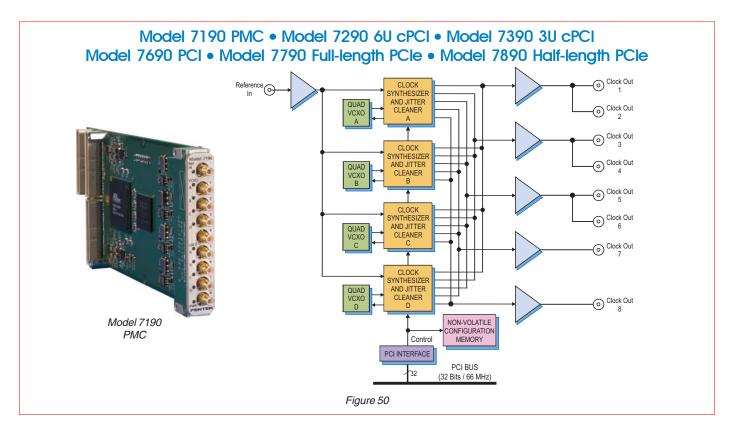
Model 6891 accepts three TTL input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Two additional inputs are provided for separate gate and sync enable signals.

Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. Alternately, a Sync Bus connector accepts LVPECL inputs from any compatible Pentek products to drive the clock, sync and gate/trigger signals.

The 6891 provides eight front panel Sync Bus output connectors, compatible with a wide range of Pentek I/O modules. The Sync Bus is distributed through ribbon cables, simplifying system design. The 6891 accepts clock input at +10 dBm to +14 dBm with a frequency range from 1 kHz to 800 MHz. This clock is used to register all sync and gate/trigger signals as well as providing a sample clock to all connected I/O modules.

A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer for output through the Sync Bus connectors.

Products

Multifrequency Clock Synthesizer

Model 7190 PMC • Model 7290 6U cPCI • Model 7390 3U cPCI
Model 7690 PCI • Model 7790 Full-length PCIe • Model 7890 Half-length PCIe

*Model 7190
PMC*

Figure 50

Model 7190 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from an input reference signal using phase-locked oscillators.

The 7190 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each device includes phase-locking circuitry that locks the frequency of its associated quad VCXO (Voltage Controlled Crystal Oscillator) to the input reference clock. This reference is a 5 or 10 MHz signal supplied to a front panel SMC connector. Each quad VCXO is programmed to generate one of four base frequencies.

Each CDC7005 generates five output signals. Each signal is independently programmable as a submultiple of the associated VCXO base frequency using divisors of 1, 2, 4, 8 or 16.
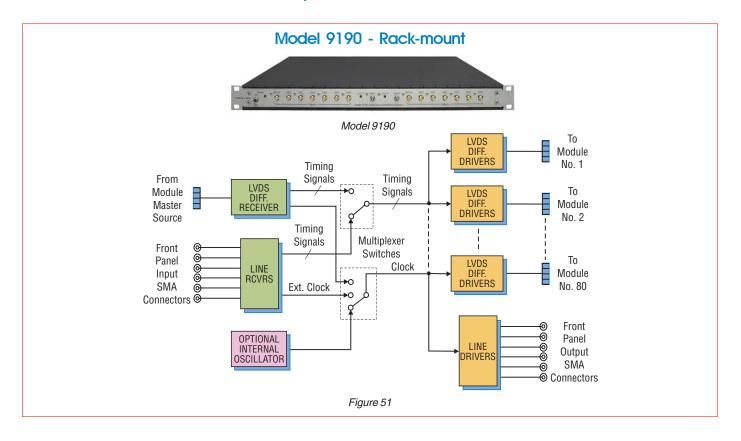
The five clock output signals from each of the four CDC7005s are joined into five clock buses. Each output can be independently enabled to drive each bus, thereby allowing any combination of output signals from the four CDC7005s.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock buses, as shown in the block diagram. This supports a single identical clock to all eight outputs or five different clocks to various outputs; numerous other combinations are possible.

The 7190 is equipped with a non-volatile memory. Once configured, the settings return to the saved configuration upon power up.

Versions of the 7190 are also available as a PCIe full-length board (Models 7790 and 7790D dual density), PCIe half-length board (Model 7890), PCI board (Model 7690), 6U cPCI (Models 7290 and 7290D dual density), or 3U cPCI (Model 7390).

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Products

Clock and Sync Generator for I/O Modules

Model 9190 - Rack-mount

Model 9190

Figure 51

Model 9190 Clock and Sync Generator synchronizes multiple Pentek I/O modules within a system to provide synchronous sampling and timing for a wide range of high-speed, multichannel data acquisition, DSP and software radio applications. Up to 80 I/O modules can be driven from the Model 9190, each receiving a common clock and up to five different timing signals which can be used for synchronizing, triggering and gating functions.
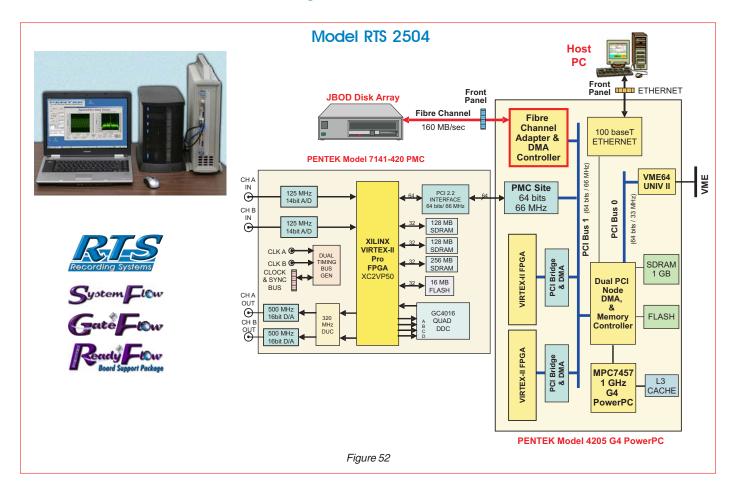
Clock and timing signals can come from six front panel SMA user inputs or from one I/O module set to act as the timing signal master. (In this case, the master I/O module will not be synchronous with the slave modules due to delays through the 9190.) Alternately, the master clock can come from a socketed, user-replaceable crystal oscillator within the Model 9190.

Buffered versions of the clock and five timing signals are available as outputs on the 9190's front panel SMA connectors.

Model 9190 is housed in a line-powered, 1.75 in. high metal chassis suitable for mounting in a standard 19 in. equipment rack, either above or below the cage holding the I/O modules.

Separate cable assemblies extend from openings in the front panel of the 9190 to the front panel clock and sync connectors of each I/O module. Mounted between two standard rack-mount card cages, Model 9190 can drive a maximum of 80 clock and sync cables, 40 to the card cage above and 40 to the card cage below. Fewer cables may be installed for smaller systems.

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Products

Real-Time Recording and Playback Transceiver System

Model RTS 2504

Figure 52

The Pentek RTS 2504 is a highly scalable real-time recording and playback system. It utilizes the Model 7141 multiband transceiver PMC/XMC module with two 14-bit 125 MHz A/Ds, ASIC DDC, and DUC with two 16-bit 500 MHz D/As.

The factory-installed IP core 420 provides a dual wideband DDC and expands the decimation range of the ASIC DDC. The core also includes an interpolation filter that expands the interpolation factor of the ASIC DUC. The Model 7141-420 combines downconverter and upconverter functions in one PCI module and offers real-time recording and playback capabilities.
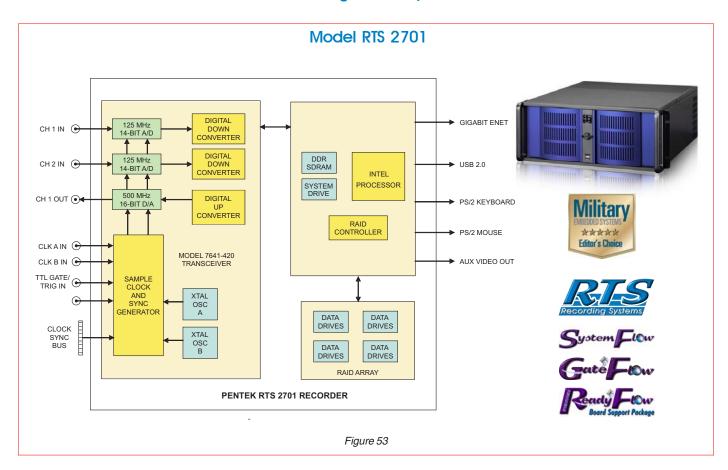
The heart of the RTS 2504 is the Pentek Model 4205 I/O Processor featuring a 1 GHz MPC7457 G4 PowerPC, mezzanine sites for two PMC modules, and two Xilinx Virtex-II FPGAs. The G4 PowerPC acts both as an executive for managing data transfer tasks as well as performing digital signal processing or formatting functions.

A built-in Fibre Channel interface connects directly to JBOD arrays for real time storage to 500 gigabytes at rates up to 160 MB/sec. Standard RS-232 and 100 baseT Ethernet ports allow the PowerPC to communicate with a wide range of host workstations for control and software development applications.

Fully supported by Pentek's SystemFlow recording software and scalable from 2 to 40 channels in a single 6U VMEbus chassis, the RTS 2504 serves equally well as a development platform for advanced research projects and proof-of-concept prototypes, or as a cost-effective strategy for deploying high-performance, multichannel embedded systems.

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Products

Rack-mount Real-Time Recording and Playback Transceiver Instrument

Model RTS 2701

Figure 53

The Pentek RTS 2701 is a highly scalable recording and playback system in an industrial rack-mount PC server chassis. Built on the Windows XP professional workstation, it utilizes the Model 7641-420 multiband transceiver PCI module with two 14-bit 125 MHz A/Ds, ASIC DDC, and DUC with two 16-bit 500 MHz D/As.
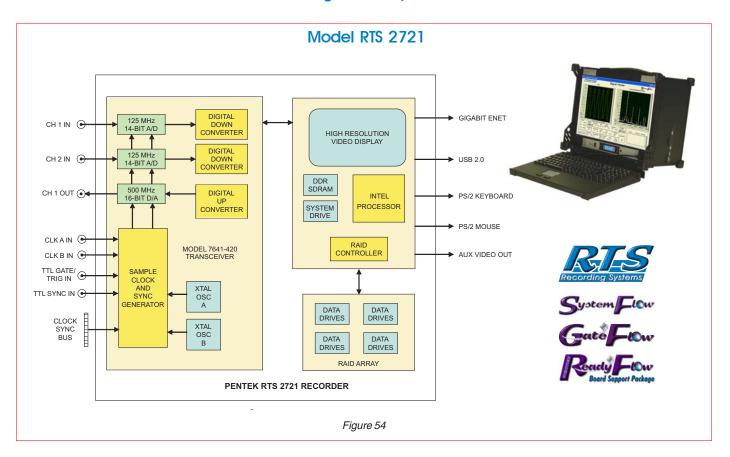
The factory-installed IP core 420 provides a dual wideband DDC and expands the decimation range of the ASIC DDC. The core also includes an interpolation filter that expands the interpolation factor of the ASIC DUC. The Model 7641-420 combines downconverter and upconverter functions in one PCI module and offers recording and playback capabilities.

Included with this instrument is Pentek's System-Flow recording software. The RTS 2701 uses a native NTFS record/playback file format for easy access by user applications for analysis, signal processing, and waveform generation. File headers include recording parameter settings and time stamping so that the signal viewer correctly formats and annotates the displayed signals.

A high-performance PCI Express SATA RAID controller connects to multiple SATA hard drives to support storage to 5 terabytes and real-time recording rates to 480 MB/sec.

Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy. The Pentek RTS 2701 serves equally well as a development platform for advanced research projects and proof-of-concept prototypes, or as a cost-effective strategy for deploying high-performance, multichannel embedded systems.

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Portable Real-Time Recording and Playback Transceiver Instrument

Model RTS 2721

Figure 54

The Pentek RTS 2721 is a turnkey real-time recording instrument supplied in a convenient briefcase-size package that weighs just 30 pounds. Built on the Windows XP professional workstation, it includes an Intel processor, a high-resolution 17 in. LCD monitor and a high-performance SATA RAID controller.

The RTS 2721 utilizes the Model 7641 multiband transceiver PCI module with two 14-bit 125 MHz A/Ds, ASIC DDC, and DUC with two 16-bit 500 MHz D/As. The factory-installed IP core 420 provides a dual wideband DDC and expands the decimation range of the ASIC DDC. The core also includes an interpolation filter that expands the interpolation factor of the ASIC DUC.

The Model 7641-420 combines downconverter and upconverter functions in one PCI module and offers recording and playback capabilities.

Fully supported by Pentek's SystemFlow recording software, the RTS 2721 uses a native NTFS record/playback file format for easy access by user applications for analysis, signal processing, and waveform generation. File headers include recording parameter settings and time stamping so that the signal viewer correctly formats and annotates the displayed signals.

A high-performance PCI Express SATA RAID controller connects to multiple SATA hard drives to support storage to 3 terabytes and real-time recording rates up to 480 MB/sec.

Pentek's portable recorder instrument provides a flexible architecture that is easily customized to meet special needs. Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy. With its wide range of programmable decimation and interpolation, the system supports signal bandwidths from 8 kHz to 60MHz.

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Applications

Applications of Software Defined Radio

- Tracking Receiver System
- Software Radio Transceiver System
- 512-Channel SDR System in a single VMEbus Slot
- Radar Signal Processing System
- 8-Channel Beamforming System

Software Radio can be used in many different systems:

Tracking receivers can be highly automated because software radio allows DSPs to perform the signal identification and analysis functions as well as the adaptable tuning functions.
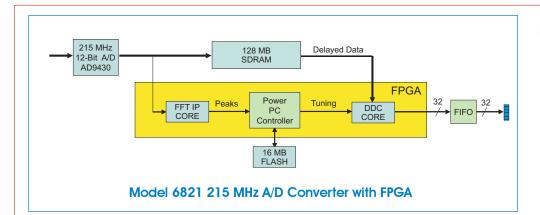
Signal intelligence applications and radar benefit from the tight coupling of the A/D, DDC, DUC, and DSP functions to process wideband signals.

Cellular phone applications are one of the strongest high-volume applications because of the high density of tightly-packed frequency division multiplexed voice channels.

Direction finding and beamforming are ideal applications for digital receivers because of their excellent channel-to-channel phase and gain matching and consistent delay characteristics.

As a general capability, any system requiring a tunable bandpass filter should be considered a candidate for using DDCs. Take a look at the following application examples to give you some more details.
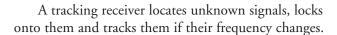
Applications

Tracking Receiver System

Model 6821 215 MHz A/D Converter with FPGA

System Highlights

- **A/D data delivered into SDRAM acts as a digital delay memory**
- **A/D data also delivered into a Pentek FFT IP core in FPGA**
- **FFT core detects the strength of signals at each analysis frequency**
- **PowerPC controller in FPGA sorts signals according to peak strenth**
- **PowerPC controller also tunes DDC IP core in FPGA to the strongest signal frequencies**
- **Delayed data from SDRAM feeds DDC IP core to compensate for FFT calculation time**
- **DDC captures these moving signals in real time and downconverts them to baseband**

Model 6821 commercial (left) and conduction-cooled version

Figure 55

A tracking receiver locates unknown signals, locks onto them and tracks them if their frequency changes.

As shown above, to implement this receiver, we use the 128 MB SDRAM of the Model 6821 to create a delay memory function.

Samples from the A/D are sent into a circular buffer within the SDRAM and also to a Pentek FFT IP core implemented in the FPGA. The spectral peaks of the FFT indicate the frequencies of signals of interest present at the input.

The PowerPC microcontroller of the FPGA digests this frequency list and decides which signals to track. It then tunes the Pentek DDC core, also implemented in

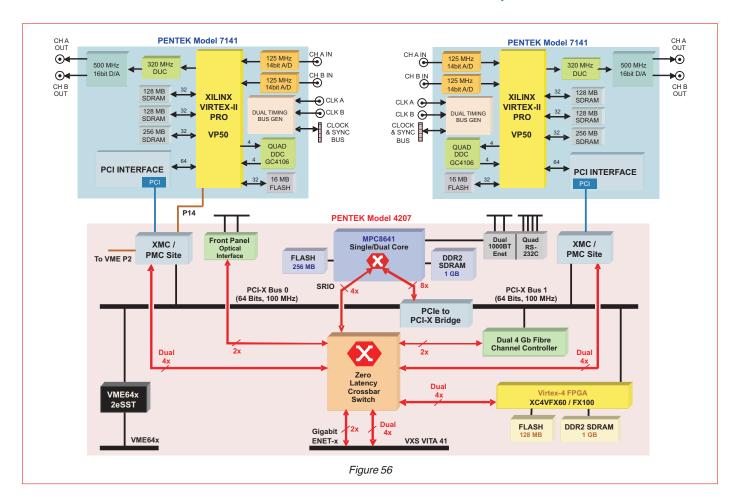the FPGA, accordingly. The delayed data from the circular buffer feeds the input of this DDC core.

The digital delay can be set to match the time it takes for the FFT energy detection and the processor algorithm for the tuning frequency decision, so that frequency-agile or transient signals can be recovered from their onset. The dehopped baseband output is delivered to the rest of the system through the FPDP port or, optionally, across a VXS link.

This Model is also available in a dual-channel version as Model 6822. Both Models are available in commercial and conduction-cooled versions.

Applications

4-Channel Software Radio Transceiver System

Figure 56

This system accepts four analog inputs from baseband or IF signals with bandwidths up to 50 MHz and IF center frequencies up to 150 MHz. A total of eight DDC channels are independently tunable across the input band and can deliver downconverted output signal bandwidths from audio up to 2.5 MHz.
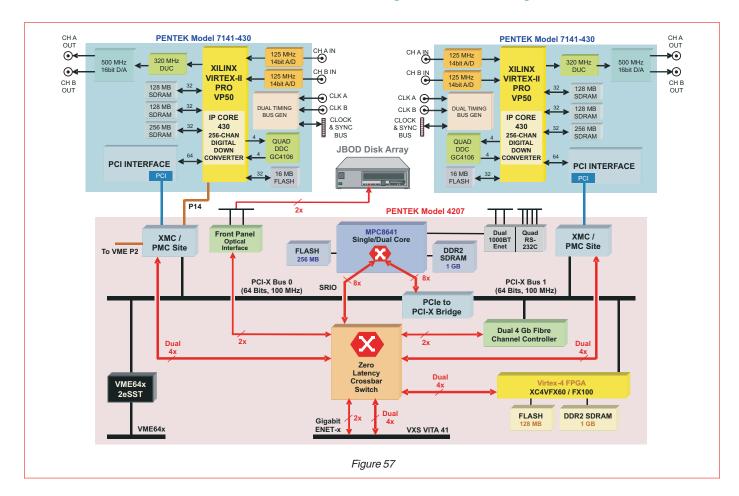
Four analog outputs can deliver baseband or IF signals with bandwidths up to about 50 MHz and IF center frequencies up to 100 MHz. The system supports four independent D/A channels or two upconverted channels with real or quadrature outputs.

Signal processing resources include the Freescale MPC8641 AltiVec processor and an FX60 or FX100 Virtex-4 FPGA on the Model 4207 I/O processor, plus a Virtex-II VP-50 FPGA on each PMC module.

Using these on-board processing resources this powerful system can process analog input data locally and deliver it to the analog outputs. It can also be used as a pre- and post-processing I/O front end for sending and receiving data to other system boards connected over the VMEbus or through switched fabric links using the VXS interface.

Ruggedized and conduction-cooled versions of the boards used in this system are available.

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Applications

512-Channel Software Radio Recording System in a Single VMEbus Slot

Figure 57

Each Model 7141 PMC features the Xilinx Virtex-II Pro VP50 with a Pentek 256-Channel Digital Down-converter (DDC) IP Core 430. Each channel provides independent tuning frequency with a global decimation from 1024 to 9984. Either one of the two 14-bit A/D converters operating at 125 MHz sample rate can feed this core producing a range of output bandwidths from 10 kHz to 100 kHz.
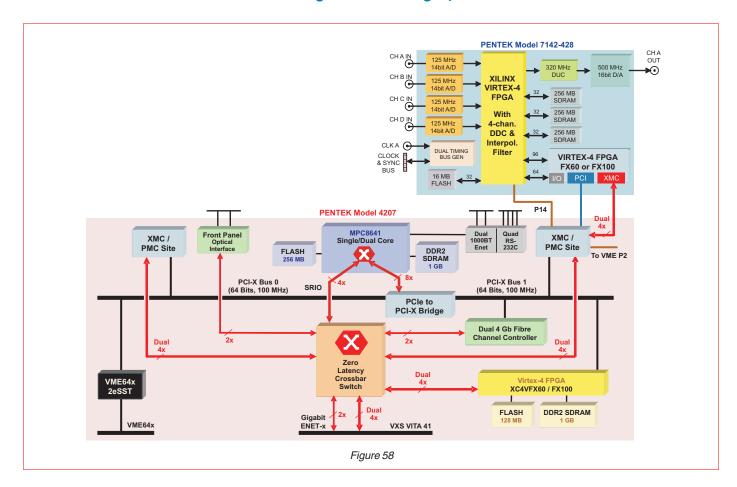
A dual 4-Gbit Fibre Channel copper interface allows wideband A/D data or DDC outputs from all 512 channels to be recorded in real time to a RAID or JBOD disk array at aggregate rates up to 640 MB/sec.

Pentek's SystemFlow® software presents an intuitive graphical user interface (GUI) to set up the DDC channels and recording mode. The GUI executes on a Windows host PC connected to the 4207 via Ethernet.

A SystemFlow signal viewer on the PC allows previewing of data prior to recording and viewing of recorded data files in both time and frequency domains. Files can be moved between the Fibre Channel disk and the PC over Ethernet.

This system is ideal for downconverting and capturing real time signal data from a very large number of channels in an extremely compact, low cost system.

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Applications

Radar Signal Processing System

Figure 58

Radar is well served by high-speed A/D converters and wideband digital downconverters. The channelized system shown above, takes advantage of a Model 7142-428 multichannel transceiver with an installed FPGA core that includes four wideband DDCs and an interpolation filter.

Operating at sampling rates up to 125 MHz, the A/D converters can digitize baseband signals with bandwidths up to 50 MHz. After frequency translation and filtering, the DDCs deliver complex (I & Q) data to the Model 4207 processor board. Here, data may be processed by custom user-defined algorithms before it is sent across the VXS interface for recording and off-line processing.

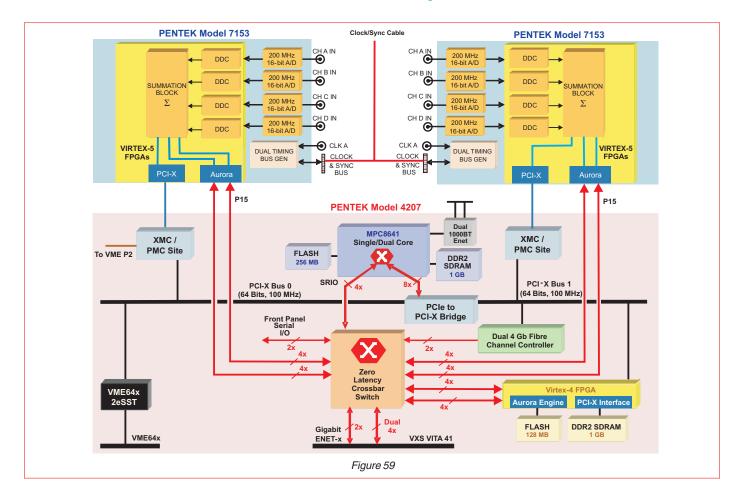The optional GateFlow FPGA Design Kit can be used to install custom algorithms in the Model 4207

FPGA. Factory-installed IP cores such as pulse compression and FFT are available and can be factory installed in this FPGA.

The upconverter with the interpolation filter can be used to generate arbitrary radar pulse waveforms that can be used to calibrate the system. The D/A output can also be used for countermeasures, such as jamming or spoofing.

Jamming blasts energy that disables radars, and spoofing deceives radars by making it seem that the target is a different shape, speed, direction or distance by using DSP techniques. This is especially useful for a jet or UAV to prevent it from getting shot down.

Note that one more PMC/XMC site is available for installation of an additional module.

Applications

8-Channel Beamforming System

Figure 59

Two Model 7153 Beamformer PMC/XMC modules are installed on the Model 4207 I/O Processor board. The eight signals to be beamformed are connected to the eight analog inputs of these modules. Joining the two 7153 modules is a clock/sync cable that synchronizes the DDCs and guarantees synchronous sampling across all eight channels.

Signals from the first four channels of the left 7153 module are summed in the left summation block; signals from the second four channels of the right 7153 are summed in the right summation block. The summation output from the left XMC module is delivered using the Aurora 4x link into one port of the crossbar switch. Each red 4x link is capable of data rates up to 1.25 GBytes/sec. The left 4-channel sum is connected through the crossbar switch and delivered into the summation input port of the right XMC module.

The Aurora summation from the left four channels is combined with the right four channels and then delivered to the crossbar switch from the right summation output port. The eight-channel combined sum is delivered through the crossbar switch into the Aurora engine implemented in the Virtex-4 FPGA of the 4207 processor board.

This Aurora engine decodes the stream and delivers it to a designated block in the DDR2 memory attached to the FPGA. The PCI-X interface in this FPGA presents the SDRAM memory as a mapped resource appearing on the processor PCI-X bus 1. The Power PC reads the data from the FPGA DDR2 memory across the PCI-X bus, creates the beamformed pattern display and presents it via its front panel gigabit Ethernet port to an attached PC for display.

Summary

DSP Boards for VMEbus

- Freescale Altivec G4 PowerPC
- Texas Instruments C6000 DSPs
- Single, Dual, Quad and Octal Processor versions
- PMC, PMC/XMC, PCI and cPCI I/O peripherals
- VME/VXS platforms

Figure 60

SDR Benefits

Benefits of Software Defined Radio:

- Reduction of DSP processing demands
- Very fast tuning
- Fast bandwidth selection
- Zero frequency drift and error
- Precise, stable filter characteristics
- Excellent dynamic range

Figure 61

Pentek offers a comprehensive array of VMEbus DSP boards featuring the AltiVec G4 PowerPC from Freescale and the TMS320C6000 family of processor products from Texas Instruments.

On-board processor densities range from one to eight DSPs with many different memory and interface options available.

The Models 4205 and 4207 I/O processor boards feature the latest G4 PowerPCs, accept PMC mezzanines and include built-in Fibre Channel interfaces.

The Models 4294 and 4295 processor boards feature four MPC74xx G4 PowerPC processors utilizing the AltiVec vector processor capable of delivering several GFLOPS of processing power.

The Models 4292 and 4293 processor boards feature the Texas Instruments latest TMS320C6000 family of fixed-point DSPs that represent a 10-fold increase in processing power over previous designs.

Once again, the ability of the system designer to freely choose the most appropriate DSP processor for each software radio application, facilitates system requirement changes and performance upgrades.

Full software development tools are available for workstations running Windows and Linux with many different development system configurations available.

To summarize, we restate the major benefits:

SDRs can dramatically reduce the DSP requirements for systems which need to process signals contained within a certain frequency band of a wideband signal.

The fast tuning of the digital local oscillator and the easy bandwidth selection in the decimating digital filter and interpolation filter make the SDR easy to control.

Since the entire circuitry uses digital signal processing, the characteristics are precise, predictable, and will not drift with time, temperature or aging. This also means excellent channel-to-channel matching and no need for calibration, alignment or maintenance.

With the addition of FPGA technology, dramatic increases in system density have been coupled with a significantly lower cost per channel. Furthermore, FPGA technology allows one to incorporate custom algorithms right at the front end of these systems.

As we have seen, there are inherently many benefits and advantages to when using SDR. We hope that this introduction has been informative. We stand ready to discuss your requirements and help you configure a complete SDR system.

For all the latest information about Pentek SDRs, DSP boards and data acquisition products, be sure to visit Pentek's comprehensive website regularly.

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Links

The following links provide you with additional information about the Pentek products presented in this handbook: just click on the Model number. Links are also provided to other handbooks or brochures that may be of interest in your software radio development projects.

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