A Software Defined Radio for the Masses, Part 4

We conclude this series with a description of a dc-60 MHz transceiver that will allow open-software experimentation with software defined radios.

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It has been a pleasure to receive feedback from so many *QEX* readers that they have been inspired to experiment with software-defined radios (SDRs) through this article series. SDRs truly offer opportunities to reinvigorate experimentation in the service and attract new blood from the ranks of future generations of computer-literate young people.[1] It is encouraging to learn that many readers see the opportunity to return to a love of experimentation left behind because of the complexity of modern hardware. With SDRs, the opportunity again exists for the experimenter to achieve results that exceed the performance of existing commercial equipment.

Most respondents indicated an interest in gaining access to a complete SDR hardware solution on which they can experiment in software. Based on this feedback, I have decided to offer the SDR-1000 transceiver described in this article as a semi-assembled, three-board set. The SDR-1000 software will also be made available in open-source form along with support for the GNU Radio project on *Linux*.[2] Table 1 outlines preliminary specifications for the SDR-1000 transceiver. I expect to have the hardware available by the time this article is in print.

The ARRL SDR Working Group includes in its mission the encouragement of SDR experimentation through educational articles and the availability of SDR hardware on which to experiment. A significant advance toward this end has been seen in the pages of *QEX* over the last year, and it continues into 2003.

This series began in Part 1 with a general description of digital signal processing (DSP) in SDRs.[3] Part 2 described *Visual Basic* source code to implement a full-duplex, quadrature interface on a PC sound card.[4] Part 3 described the use of DSP to make the PC sound-card interface into a functional software-defined radio.[5] It also explored the filtering technique called FFT fast-convolution filtering. In this final article, I will describe the SDR-1000 transceiver hardware including an analysis of gain distribution, noise figure and dynamic range. There is also a discussion of frequency control using the AD9854 quadrature DDS.

[1]Notes appear on page 28.

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To further support the interest generated by this series, I have established a Web site at **home.earthlink.net/~g_youngblood**. As you experiment in this interesting technology, please e-mail suggested enhancements to the site.

Is the "Tayloe Detector" Really New?

In Part 1, I described what I knew at the time about a potentially new approach to detection that was dubbed the "Tayloe Detector." In the same issue, Rod Green described the use of the same circuit in a multiple conversion scheme he called the "Dirodyne".[6] The question has been raised: Is this new technology or rediscovery of prior art? After significant research, I have concluded that both the "Tayloe Detector" and the "Dirodyne" are simply rediscovery of prior art; albeit little known or understood. In the September 1990 issue of *QEX*, D. H. van Graas, PAØDEN, describes "The Fourth Method: Generating and Detecting SSB Signals."[7] The three previous methods are commonly called the *phasing method*, the *filter method* and the *Weaver method*. The "Tayloe Detector" uses *exactly* the same concept as that described by van Grass with the exception that van Grass uses a double-balanced version of the circuit that is actually superior to the singly-balanced detector described by Dan Tayloe[8] in 2001.

In his article, van Graas describes how he was inspired by old frequency-converter systems that used ac motor-generators called "selsyn" motors. The selsyn was one part of an electric axle formerly used in radar systems. His circuit used the CMOS 4052 dual 1-4 multiplexer (an early version of the more modern 3253 multiplexers referenced in Part 1 of this series) to provide the four-phase switching. The article describes circuits for both transmit and receive operation.

Phil Rice, VK3BKR, published a nearly identical version of the van Graas transmitter circuit in *Amateur Radio* (Australia) in February 1998, which may be found on the Web.[9] While he only describes the transmit circuitry, he also states, "... the switching modulator should be capable of acting as a demodulator."

It's the Capacitor, Stupid!

So why is all this so interesting? First, it appears that this truly is a "fourth method" that dates back to at least 1990. In the early 1990s, there was a saying in the political realm: "It's the economy, stupid!" Well, in this case, it's the capacitor, stupid! Traditional commutating mixers do not have capacitors (or integrators) on their output. The capacitor converts the commutating switch from a mixer into a sampling detector (more accurately a track-and-hold) as discussed on page 8 of Part 1 (see Note 3). Because the detector operates according to sampling theory, the mixing products sum aliases back to the same frequency as the difference product, thereby limiting conversion loss. In reality, a switching detector is simply a modified version of a digital commutating filter as described in previous *QEX* articles.[10, 11, 12]

Instead of summing the four or more phases of the commutating filter into a single output, the sampling detector sums the 0° and 180° phases into the in-phase (I) channel and the 90° and 270° phases into the quadrature (Q) channel. In fact, the mathematical analysis described in Mike Kossor's article (see Note 10) applies equally well to the sampling detector.

Is the "Dirodyne" Really New?

The Dirodyne is in reality the sampling detector driving the sampling generator as described by van Graas, forming the architecture first described by Weaver in 1956.[13] The Weaver method was covered in a series of *QEX* articles[14, 15, 16] that are worth reading. Other interesting reading on the subject may be found on the Web in a Phillips Semiconductors application note[17] and an article in *Microwaves & RF*.[18]

Peter Anderson in his Jul/Aug 1999 letter to the *QEX* editor specifically describes the use of back-to-back commutating filters to perform frequency shifting for SSB generation or reception.[19] He states that if, on the output of a commutating filter, we can, "...add a second commutator connected to the same set of capacitors, and take the output from the second commutator. Run the two commutators at different frequencies and find that the input passband is centered at a frequency set by the input commutator; the output passband is centered at a frequency set by the output commutator. Thus, we have a device that shifts the signal frequency, an SSB generator or receiver." This is exactly what the Dirodyne does. He goes on to state, "The frequency-shifting commutating filter is a generalization of the Weaver method of SSB generation."

So What Shall We Call It?

Although Dan Tayloe popularized the sampling detector, it is probably not appropriate to call it the Tayloe detector, since its origin was at least 10 years earlier, with van Graas. Should we call it the "van Graas Detector" or just the "Fourth Method?" Maybe we should, but since I don't know if van Graas originally invented it, I will simply call it the quadrature-sampling detector (QSD) or quadrature-sampling exciter (QSE).

Dynamic Range—How Much is Enough?

The QSD is capable of exceptional dynamic range. It is possible to design a QSD with virtually no loss and 1-dB compression of at least 18 dBm (5 V_{P-P}). I have seen postings on e-mail

Table 1—SDR-1000 Preliminary Hardware Specifications

Frequency Range	0-60 MHz
Minimum Tuning Step	1 μHz
DDS Clock	200 MHz, <1 ps RMS jitter
1dB Compression	+6 dBm
Max. Receive Bandwidth	44 kHz-192 kHz (depends on PC sound card)
Transmit Power	1 W PEP
PC Control Interface	PC parallel port (DB-25 connector)
Rear Panel Control Outputs	7 open-collector Darlington outputs
Input Controls	PTT, Code Key, 2 Spare TTL Inputs
Sound Card Interface	Line in, Line out, Microphone in
Power	13.8 V dc

Table 2—Acceptable Noise Figure for Terrestrial Communications

Frequency (MHz)	*Acceptable NF (dB)*
1.8	45
3.5	37
4.0	27
14.0	24
21.0	20
28.0	15
50.0	9
144.0	2

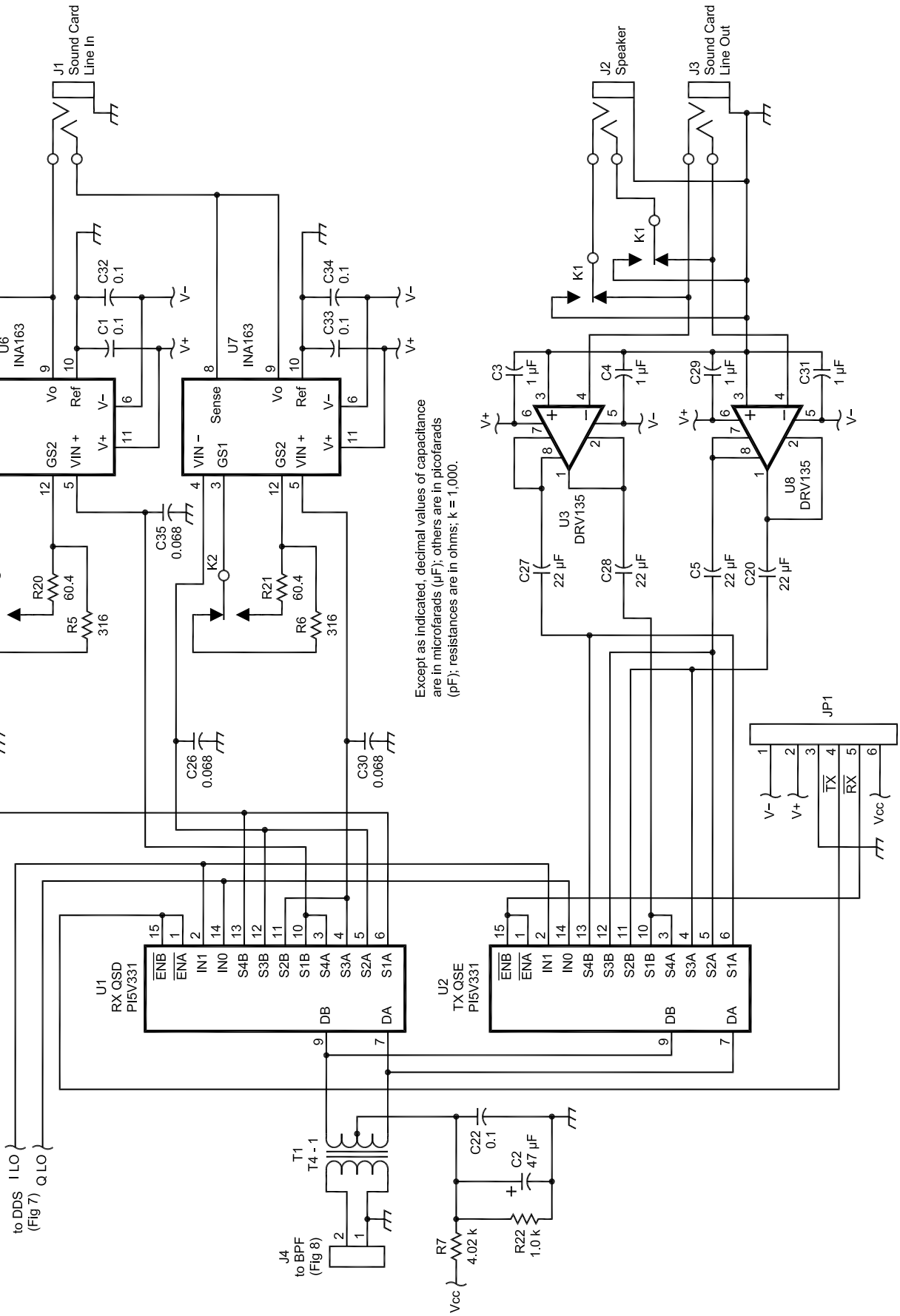


Fig 1—SDR-1000 receiver/exciter schematic.

reflectors claiming measured *IP3* in the +40 dBm range for QSD detectors using 5-V parts. With ultra-low-noise audio op amps, it is possible to achieve an analog noise figure on the order of 1 dB without an RF preamplifier. With appropriately designed analog AGC and careful gain distribution, it is theoretically possible to achieve over 150 dB of total dynamic range. The question is whether that much range is needed for typical HF applications. In reality, the answer is no. So how much is enough?

Several *QEX* writers have done an excellent job of addressing the subject.[20, 21, 22] Table 2 was originally published in an October 1975 *ham radio* article.[23] It provides a straightforward summary of the acceptable receiver noise figure for terrestrial communication for each band from 160 m to 2 m. Table 3 from the same article illustrates the acceptable noise figures for satellite communications on bands from 10 m to 70 cm.

For my objective of dc-60 MHz coverage in the SDR-1000, Table 2 indicates that the acceptable noise figure ranges from 45 dB on 160 m to 9 dB on 6 m. This means that a 1-dB noise figure is overkill until we operate near the 2-m band. Further, to utilize a 1-dB noise figure requires almost 70 dB of analog gain ahead of the sound card. This means that proper gain distribution and analog AGC design is critical to maximize IMD dynamic range.

After reading the referenced articles and performing measurements on the Turtle Beach Santa Cruz sound card, I determined that the complexity of an analog AGC circuit was unwarranted for my application. The Santa Cruz card has an input clipping level of 12 V (RMS, 34.6 dBm, normalized to 50 Ω) when set to a gain of –10 dB. The maximum output available from my audio signal generator is 12 V (RMS). The SDR software can easily monitor the peak signal input and set the corresponding sound card input gain to effectively create a digitally controlled analog AGC with no external hardware. I measured the sound card's 11-kHz SNR to be in the range of 96 dB to 103 dB, depending on the setting of the card's input gain control. The input control is capable of attenuating the gain by up to 60 dB from full scale. Given the large signal-handling capability of the QSD and sound card, the 1-dB compression point will be determined by the output saturation level of the instrumentation amplifier.

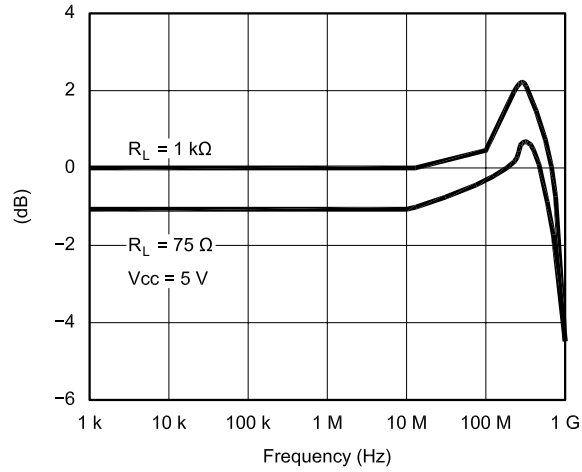
Of note is the fact that DVD sales are driving improvements in PC sound cards. The newest 24-bit sound cards sample at a rate of up to 192 kHz. The Waveterminal 192X from EGO SYS is one example.[24] The manufacturer boasts of a 123 dB dynamic range, but that number should be viewed with caution because of the technical difficulties of achieving that many bits of true resolution. With a 192-kHz sampling rate, it is possible to achieve real-time reception of 192 kHz of spectrum (assuming quadrature sampling).

Quadrature Sampling Detector/ Exciter Design

In Part 1 of this series (Note 3), I described the operation of a single-balanced version of the QSD. When the circuit is reversed so that a quadrature excitation signal drives the sampler, a SSB generator or exciter is created. It is a simple matter to reverse the SDR receiver software so that it transforms microphone input into filtered, quadrature output to the exciter.

While the singly-balanced circuit described in Part 1 is extremely simple, I have chosen to use the double-balanced QSD as shown in Fig 1 because of its superior common mode and even-harmonic rejection. U1, U6 and U7 form the receiver and U2, U3 and U8 form the exciter. In the receive mode, the QSD functions as a two-capacitor commutating filter, as described by Chen Ping in his article (Note 11). A commutating filter works like a comb filter, wherein the circuit responds to harmonics of the commutation frequency. As he notes, ". . . it can be shown that signals having harmonic numbers equal to any of the integer factors of the number of capacitors may pass." Since two capacitors are used in each of the I and Q channels, a two-capacitor commutating filter is formed. As Ping further states, this serves to suppress the even-order harmonic responses of the circuit. The output of a two-capacitor filter is extremely phase-sensitive, therefore allowing the circuit to perform signal detection just as a CW demodulator does. When a signal is near the filter's center frequency, the output amplitude would be modulated at the difference (beat) frequency. Unlike a typical filter, where phase sensitivity is undesirable, here we actually take advantage of that capability.

The commutator, as described in Part 1, revolves at the center frequency of the filter/detector. A signal tuned exactly to the commutating frequency will result in a zero beat. As the signal is tuned to either side of the commutation frequency, the beat note output will be proportional to the difference frequency. As the signal is tuned toward the second harmonic, the output will decrease until a null occurs at the harmonic frequency. As the signal is tuned



Note: Insertion Log = 20 log | Vo / Vs |

Fig 2—QS4A210 insertion loss versus frequency

Table 3—Acceptable Noise Figure for Satellite Communications

Frequency (MHz)	*Galactic Noise Floor (dBm/Hz)*	*Acceptable NF (dB)*
28	–125	8
50	–130	5
144	–139	1
220	–140	0.7
432	–141	0.2

further, it will rise to a peak at the third harmonic and then decrease to another null at the fourth harmonic. This cycle will repeat indefinitely with an amplitude output corresponding to the $\sin(x)/x$ curve that is characteristic of sampling systems as discussed in DSP texts. The output will be further attenuated by the frequency-response characteristics of the device used for the commutating switch. The PI5V331 multiplexer has a 3-dB bandwidth of 150 MHz. Other parts are available with 3-dB bandwidths of up to 1.4 GHz (from IDT Semiconductor).

Fig 2 shows the insertion loss versus frequency for the QS4A210. The upper frequency limitation is determined by the switching speed of the part (1 ns = T_{on} / T_{off}, best-case or 12.5 ns worst-case for the 1.4-GHz part) and the $\sin(x)/x$ curve for under-sampling applications.

The PI5V331 (functionally equivalent to the IDT QS4A210) is rated for analog operation from 0 to 2 V. The QS4A210 data sheet provides a drain-to-source on-resistance curve versus the input voltage as shown in Fig 3. From the curve, notice that the on resistance (R_{on}) is linear from 0 to 1 V and increases by less than 2 Ω at 2 V. No curve is provided in the PI5V331 data sheet, but we should be able to assume the two are comparable. In fact, the PI5V331 has a R_{on} specification of 3 Ω (typical) versus the 5 Ω (typical) for the QS41210. In the receive application of the QSD, the R_{on} is looking into the 60-MΩ input of the instrumentation amplifier. This means that ΔR_{on} modulation is virtually nonexistent and will have no material effect on circuit linearity.[25] Unlike typical mixers, which are nonlinear, the QSD is a linear detector!

Eq 1 determines the bandwidth of the QSD, where R_{ant} is the antenna impedance, C_S is the sampling capacitor value and n is the total number of sampling capacitors ($1/n$ is effectively the switch duty cycle on each capacitor). In the doubly balanced QSD, n is equal to 2 instead of 4 as in the singly balanced circuit. This is because the capacitor is selected twice during each commutation cycle in the doubly balanced version.

$$BW_{det} = \frac{1}{\pi n R_{ant} C_S} \qquad \text{(Eq 1)}$$

A tradeoff exists in the choice of QSD bandwidth. A narrow bandwidth such as 6 kHz provides increased blocking and IMD dynamic range because of the very high Q of the circuit. When designed for a 6-kHz bandwidth, the response at 30 kHz—one decade from the 3-kHz 3-dB point—either side of the center frequency will be attenuated by 20 dB. In this case, the QSD forms a 6-kHz-wide tracking filter centered at the commutating frequency. This means that strong signals outside the passband of the QSD will be attenuated, thereby dramatically increasing *IP3* and blocking dynamic range.

I am interested in wider bandwidth for several reasons and therefore willing to trade off some of the IMD-reduction potential of the QSD filter. In SDR applications, it is desirable in many cases to receive the widest bandwidth of which the sound card is capable. In my original design, that is 44 kHz with quadrature sampling. This capability increases to 192 kHz with the newest sound cards. Not only does this allow the capability of observing the real-time spectrum of up to 192 kHz, but it also brings the potential for sophisticated noise and interference reduction.[26]

Further, as we will see in a moment, the wider bandwidth allows us to reduce the analog gain for a given sensitivity level. The 0.068-µF sampling capacitors are selected to provide a QSD bandwidth of 22 kHz with a 50-Ω antenna. Notice that any variance in the antenna impedance will result in a corresponding change in the bandwidth of the detector. The only way to avoid this is to put a buffer in front of the detector.

The receiver circuit shown in Part 1 used a differential summing op amp after the detector. The primary advantage of a low-noise op amp is that it can provide a lower noise figure at low gain settings. Its disadvantage is that the inverting input of the op amp will be at virtual ground and the non-inverting input will be high impedance. This means that the sampling capacitor on the inverting input will be loaded differently from the non-inverting input. Thus, the respective passbands of the two inputs will not track one another. This problem is eliminated if an instrumentation amplifier is used. Another advantage of using an instrumentation amplifier as opposed to an op amp is that the antenna impedance is removed from the amplifier gain equation. The single disadvantage of the instrumentation amplifier is that the voltage noise

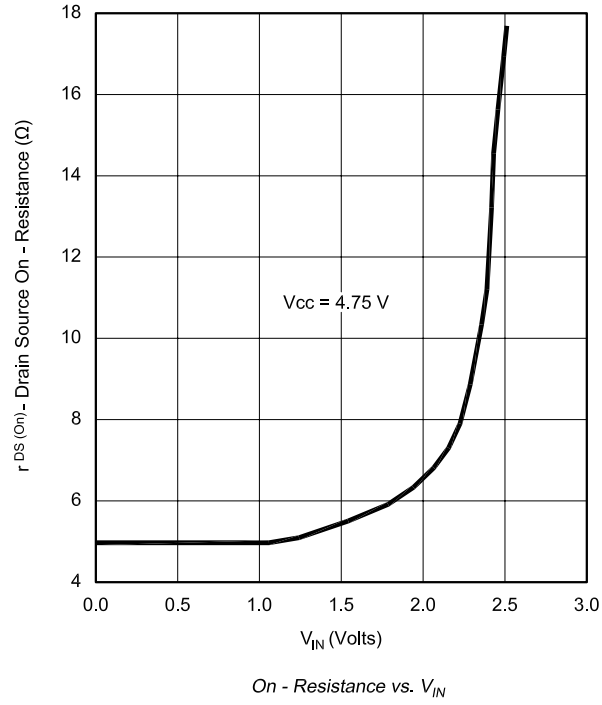


Fig 3—QS4A210 R_{on} versus V_{IN}.

Table 4—INA 163 Noise Data at 10 kHz

Gain (dB)	*e_n*	*i_n*	*NF (dB)*
20	7.5 nV/√ Hz	0.8 pA/√ Hz	12.4
40	1.8 nV/√ Hz	0.8 pA/√ Hz	3.0
60	1.0 nV/√ Hz	0.8 pA/√ Hz	1.3

and thus the noise figure increases with decreasing gain.

Table 4 shows the voltage noise, current noise and noise figure for a 200-Ω source impedance for the TI INA163 instrumentation amplifier. Since a single resistor sets the gain of each amplifier, it is a simple matter to provide two or more gain settings with relay or solid-state switching.

Unlike typical mixers, which are normally terminated in their characteristic impedances, the QSD is a high-impedance, sampling device. Within the passband, the QSD outputs are terminated in the 60-MΩ inputs of the instrumentation amplifiers. The IDT data sheet for the QS4A210 indicates that the switch has *no insertion loss* with loads of 1 kΩ or more! This coincides with my measurements on the circuit. If you apply 1 V of RF into the detector, you get 1 V of audio out on each of the four capacitors—a no-loss detector. Outside the passband, the decreasing reactance of the sampling capacitors will reduce the signal level on the amplifier inputs. While it is possible to insert series resistors on the output of the QSD, so that it is terminated outside the passband, I believe this is unnecessary. For receive operation, filter reflections outside the passband are not very important. Further, the termination resistors would create an additional source of thermal noise.

As stated earlier, the circuitry of the QSD may be reversed to form a quadrature sampling exciter (QSE). To do so, we must differentially drive the I and Q inputs of the QSE. The Texas Instruments DRV135 50-Ω differential audio line driver is ideally suited for the task. Blocking capacitors on the driver outputs prevent dc-offset variation between the phases from creating a carrier on the QSE output. Carrier suppression has been measured to be on the order of –48 dBc relative to the exciter's maximum output of +10 dBm. In transmit mode, the output impedance of the exciter is 50 Ω so that the band-pass filters are properly terminated.

Conveniently, T/R switching is a simple matter since the QSD and QSE can have their inputs connected in parallel to share the same transformer. Logic control of the respective multiplexer-enable lines allows switching between transmit and receive mode.

Level Analysis

The next step in the design process is to perform a system-level analysis of the gain required to drive the sound card A/D converter. One of the better references I have found on the subject is the book by W. Sabin and E. Schoenike, *HF Radio Systems and Circuits.*[27] The book includes an *Excel* spreadsheet that allows interactive examination of receiver performance using various A/D converters, sample rates, bandwidths and gain distributions. I have placed a copy of the SDR-1000 Level Analysis spreadsheet (by permission, a highly modified version of the one provided in the book) for download from ARRLWeb.[28] Another excellent resource on the subject is the Digital Receiver/Exciter Design chapter from the book *Digital Signal Processing in Communication Systems.*[29]

Notice that the former reference has a better discussion of the minimum gain required for thermal noise to transition the quantizing level as discussed here. Neither text deals with the effects of atmospheric noise on the noise floor and hence on dynamic range. This is—in my opinion—a major oversight for HF communications since atmospheric noise will most likely limit the minimum discernable signal, not thermal noise.

For a weak signal to be recovered, the minimum analog gain must be great enough so that the weakest signal to be received, plus thermal and atmospheric noise, is greater than at least one A/D converter quantizing level (the least-significant usable bit). For the A/D converter quantizing noise to be evenly distributed, several quantizing levels must be traversed. There are two primary ways to achieve this: Out-of-band dither noise may be added and then filtered out in the DSP routines, or in-band thermal and atmospheric noise may be amplified to a level that accomplishes the same. While the first approach offers the best sensitivity at the lowest gain, the second approach is simpler and was chosen for my application. *HF Radio Systems and Circuits* states, "Normally, if the noise is Gaussian distributed, and the RMS level of the noise at the A/D converter is greater than or equal to the level of a sine wave which just bridges a single quantizing level, an adequate number of quantizing levels will be bridged to guarantee uniformly distributed quantizing noise." Assuming uniform noise distribution, Eq 2 is used to determine the quantizing noise density, N_{0q}:

$$N_{0q} = \frac{\left(\frac{V_{pp}}{2^b}\right)^2}{6 f_s R} \text{ W/Hz} \qquad \text{(Eq 2)}$$

where
$V_{P\text{-}P}$= peak-to-peak voltage range
b = number of valid bits of resolution
f_s = A/D converter sampling rate
R = input resistance
N_{0q} = quantizing noise density

The quantizing noise decreases by 3 dB when doubling the sampling rate and by 6 dB for every additional bit of resolution added to the A/D converter. Notice that just because a converter is specified to have a certain number of bits does not mean that they are all usable bits. For example, a converter may be specified to have 16 bits; but in reality, only be usable to 14-bits. The Santa Cruz card utilizes an 18-bit A/D converter to deliver 16 usable bits of resolution. The maximum signal-to-noise ratio may be determined from Eq 3:

$$SNR = 6.02b + 1.75 \text{ dB} \qquad \text{(Eq 3)}$$

For a 16-bit A/D converter having a maximum signal level (without input attenuation) of 12.8 $V_{P\text{-}P}$, the minimum quantum level is –70.2 dBm. Once the quantizing level is known, we can compute the minimum gain required from Eq 4:

$$Gain = quantizing\ level - kTB + analog\ NF + atmospheric\ NF - 10\log_{10} BW \qquad \text{(Eq 4)}$$

where:

$$\underset{level}{quantizing} = 10\log_{10}\left(\frac{\left(\frac{V_{pp}\times 0.707}{2^b\times 2}\right)^2}{50\times 0.001}\right) \text{dBm}$$

kTB / Hz = –174 dBm/Hz
analog NF = analog receiver noise figure, in decibels
atmospheric NF = atmospheric noise figure for a given frequency
BW = the final receive filter bandwidth in hertz

Table 5, from the SDR-1000 Level Analysis spreadsheet, provides the cascaded noise figure and gain for the circuit shown if Fig 1. This is where things get interesting.

Fig 4 shows an equivalent circuit for the QSD and instrumentation amplifier during a respective switch period. The transformer was selected to have a 1:4 impedance ratio. This means that the turns ratio from the primary to the secondary for each switch to ground is 1:1, and therefore the voltage on each switch is equal to the input signal voltage. The differential impedance across the transformer secondary will be 200 Ω, providing a good noise match to the INA163 amplifier. Since the input impedance of the INA163 is 60 MΩ, power loss through the circuit is virtually nonexistent. We must therefore analyze the circuit based on voltage gain, not power gain.

Table 5 –Cascaded Noise Figure and Gain Analysis from the SDR-1000 Level Analysis Spreadsheet

		BPF	*T1-4*	*PI5V331*	*INA163*	*ADC*
dB	Noise Figure	0.0	0.0	0.0	3.0	58.6
dB	Gain	0.0	6.0	0.0	40.0	0.0
Equivalent Power Factor	Noise Factor	1.00	1.00	1.00	1.99	720,482
Equivalent Power Factor	Gain	1	4	1	10,000	1
Clipping Level	Vpk			1.0	13.0	6.4
Clipping Level	dBm			10.0	32.3	26.1
Cascaded Gain	dB	0.0	6.0	6.0	46.0	46.0
Cascaded Noise Factor		1.00	1.00	1.00	1.25	19.06
Cascaded Noise Figure	dB	0.0	0.0	0.0	1.0	12.8
Output Noise	dBm/Hz	–174.0	–174.0	–174.0	–173.0	–161.2

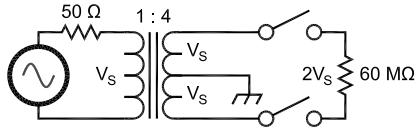


Fig 4—Doubly balanced QSD equivalent circuit.

That means that we get a 6-dB differential voltage gain from the input transformer—the equivalent of a 0-dB noise figure amplifier! Further, there is no loss through the QSD switches due to the high-impedance load of the INA. With a source impedance of 200 Ω, the INA163 has a noise figure of approximately 12.4 dB at 20 dB of gain, 3 dB at 40 dB of gain and 1.3 dB at 60 dB of gain.

In fact, the noise figure of the analog front end is so low that if it were not for the atmospheric noise on the HF bands, we would need to add a lot of gain to amplify the thermal noise to the quantizing level. The textbook references ignore this fact. In addition to the *ham radio* article (Note 23) and Peter Chadwick's *QEX* article (Note 20), John Stephenson in his *QEX* article[30] about the ATR-2000 HF transceiver provides further insight into the subject. Table 6 provides a summary of the external noise figure for a by-band quiet location as determined from Fig 1 in Stephenson's article. As can be seen from the table, it is counterproductive to have high gain and low receiver noise figure on most of the HF bands.

Table 6—Atmospheric Equivalent Noise Figure By Band

Band (Meters)	*Ext Noise (dBm/Hz)*	*Ext NF (dB)*
160	–128	46
80	–136	38
40	–144	30
30	–146	28
20	–146	28
17	–152	22
15	–152	22
12	–154	20
10	–156	18
6	–162	12

Table 7—SDR-1000 Level Analysis Assumptions for the 10-Meter Band with 40 dB of INA Gain

Receiver Gain Distribution and Noise Performance	
Turtle Beach Santa Cruz Audio Card	
Band Number	9
Band	10 Meters
Include External NF? (True=1, False=0)	1
External (Atmospheric) Noise Figure	18 dB
A/D Converter Resolution (bits)	16 bits (98.1 dB)
A/D Converter Full–Scale Voltage	6.4 V-peak (26.1 dBm)
A/D Converter Quantizing Signal Level	–70.2 dBm
Quantizing Gain Over/(Under)	7.2 dB
A/D Converter Sample Frequency	44.1 kHz
A/D Converter Input Bandwidth (BW1)	40.0 kHz
Information Bandwidth (BW2)	0.5 kHz
Signal at Antenna for INA Saturation	–13.7 dBm
Nominal DAC Output Level	0.5 V peak (4.0 dBm)
AGC Threshold at Ant (40 dB Headroom)	–51.4 dBm
Sound Card AGC Range	60.0 dB

Tables 7 and 8 are derived from the *SDR-1000 Level Analysis* spreadsheet (Note 28) for the 10-m band. The spreadsheet tables interact with one another so that a change in an assumption will flow through all the other tables. A detailed discussion of the spreadsheet is beyond the scope of this text. The best way to learn how to use the spreadsheet is to plug in values of your own. It is also instructive to highlight cells of interest to see how the formulas are derived. Based on analysis using the spreadsheet, I have chosen to make the gain setting relay-selectable between INA gain settings of 20 dB for the lower bands and 40 dB for the higher bands.

It is important to remember that my noise and dynamic-range calculations include external noise figure in addition to the thermal noise figure. This is much more realistic for HF applications than the typical lab testing and calculations you see in most references. With the INA163 gain set to 40 dB, the cascaded analog thermal NF is calculated to be just 1 dB at the input to the sound card. If it were not for the external noise, nearly 70 dB of analog gain would be required to amplify the thermal noise

Table 8—SDR-1000 Level Analysis Detail for the 10-Meter Band with 40dB of INA Gain

Antenna Signal Level (dBm)	*INA Output Level (dBm)*	*Antenna Overload Level (dBm)*	*Total Analog Gain (dB)*	*Sound Card AGC Reduction (dB)*	*Noise at A/D Input in BW1 (dBm)*	*A/D Signal Level (dBm)*	*Noise in A/D Input in BW2 (dBm)*	*Quantizing Noise of A/D in BW2 (dBm)*	*Total Noise in BW2 (dBm)*	*Output S/N Ratio in BW2 (dB)*	*Digital Gain Required (dB)*
–128	–82		46.0	0.0	–63.0	–82.0	–82.0	–88.4	–81.1	–0.9	86.0
–118	–72		46.0	0.0	–63.0	–72.0	–82.0	–88.4	–81.1	9.1	76.0
–108	–62		46.0	0.0	–63.0	–62.0	–82.0	–88.4	–81.1	19.1	66.0
–98	–52		46.0	0.0	–63.0	–52.0	–82.0	–88.4	–81.1	29.1	56.0
–88	–42		46.0	0.0	–63.0	–42.0	–82.0	–88.4	–81.1	39.1	46.0
–78	–32		46.0	0.0	–63.0	–32.0	–82.0	–88.4	–81.1	49.1	36.0
–68	–22		46.0	0.0	–63.0	–22.0	–82.0	–88.4	–81.1	59.1	26.0
–58	–12		46.0	0.0	–63.0	–12.0	–82.0	–88.4	–81.1	69.1	16.0
–48	–2		42.7	–3.3	–66.4	–5.4	–85.4	–88.4	–83.6	78.2	9.4
–38	8		32.7	–13.3	–76.4	–5.4	–95.4	–88.4	–87.6	82.2	9.4
–28	18		22.7	–23.3	–86.4	–5.4	–105.4	–88.4	–88.3	82.9	9.4
–18	28		12.7	–33.3	–96.4	–5.4	–115.4	–88.4	–88.4	83.0	9.4
–8	38	6	2.7	–43.3	–106.4	–5.4	–125.4	–88.4	–88.4	83.0	9.4
2	48	16	–7.3	–53.3	–116.4	–5.4	–135.4	–88.4	–88.4	83.0	9.4
12	58	26	–14.0	–60.0	–123.0	–2.0	–142.0	–88.4	–88.4	86.4	6.0
22	68	36	–14.0	–60.0	–123.0	8.0	–142.0	–88.4	–88.4	96.4	–4.0
32	78	46	–14.0	–60.0	–123.0	18.0	–142.0	–88.4	–88.4	106.4	–14.0

to the quantizing level or dither noise would have to be added outside the passband. Fig 6 illustrates the signal-to-noise ratio curve with external noise for the 10-m band and 40 dB of INA gain. Fig 5 shows the same curve without external noise and with INA gain of 60 dB. This much gain would not improve the sensitivity in the presence of external noise but would reduce blocking and IMD dynamic range by 20 dB. On the lower bands, 20 dB or lower INA gain is perfectly acceptable given the higher external noise.

Frequency Control

Fig 7 illustrates the Analog Devices AD9854 quadrature DDS circuitry for driving the QSD/QSE. Quadrature local-oscillator signals allow the elimination of the divide-by-four Johnson counter, described in Part 1, so that the DDS runs at the carrier frequency instead of its fourth harmonic. I have chosen to use the 200-MHz version of the part to minimize heat dissipation, and because it easily meets my frequency coverage requirements of dc-60 MHz. The DDS outputs are connected to seventh-order elliptical low-pass filters that also provide a dc reference for the high-speed comparators. The AD9854 may be controlled either through a SPI port or a parallel interface. There are timing issues in SPI mode that require special care in programming. Analog Devices have developed a protocol that allows the chip to be put into external I/O update mode to work around the serial

About Intel Performance Primitives

Many readers have inquired about Intel's replacement of its Signal Processing Library (SPL) with the Intel Performance Primatives (IPP). The SPL was a free distribution, but the Intel Web site states that IPP requires payment of a $199 fee after a 30 day evaluation period. A fully functional trial version of IPP may be downloaded from the Intel site at **www.intel.com/software/products/global/eval.htm**. The author has confirmed with Intel Product Management that no license fee is required for amateur experimentation using IPP, and there is no limit on the evaluation period for such use. Intel actually encourages this type of experimental use. Payment of the license fee is required if and only if there is a commercial distribution of the DLL code.—*Gerald Youngblood*

timing problem. In the final circuit, I chose to use the parallel mode.

According to Peter Chadwick's article (Note 20), phase-noise dynamic range is often the limiting factor in receivers instead of IMD dynamic range. The AD9854 has a residual phase noise of better than –140 dBc/Hz at a 10-kHz offset when directly clocked at 300 MHz and programmed for an 80-MHz output. A very low-jitter clock oscillator is required so that the residual phase noise is not degraded significantly.

High-speed data communications technology is fortunately driving the introduction of high-frequency crystal oscillators with very low jitter specifications. For example, Valpey Fisher makes oscillators specified at less than 1 ps RMS jitter that operate in the desired 200-300 MHz range. According to Analog Devices, 1 ps is on the order of the residual jitter of the AD9854.

Band-Pass Filters

Theoretically, the QSD will work just fine with low-pass rather than band-pass filters. It responds to the carrier frequency and odd harmonics of the carrier; however, very large signals at half the carrier frequency can be heard in the output. For example, my measurements show that when the receiver is tuned to 7.0 MHz, a signal at 3.5 MHz is attenuated by 49 dB. The measurements show that the attenuation of the second harmonic is 37 dB and the third harmonic is down 9 dB from the 7-MHz reference. While a simple low-pass filter will suffice in some applications, I chose to use band-pass filters.

Fig 8 shows the six-band filter design for the SDR-1000. Notice that only the 2.5-MHz filter has a low-pass characteristic; the rest are band-pass filters.

SDR-1000 Board Layout

For the final PC-board layout, I decided on a 3×4-inch form factor. The receiver, exciter and DDS are located on one board. The band-pass filter and a 1-W driver amplifier are located on a second board. The third board has a PC parallel-port interface for control, and power regulators for operation from a 13.8-V dc power source. The three boards sandwich together into a small 3×4×2-inch module with rear-mount connectors and no interconnection wiring required. The boards use primarily surface-mount components, except for the band-pass filter, which uses mostly through-hole components.

Acknowledgments

I would like to thank David Brandon and Pascal Nelson of Analog Devices for their answering my questions about the AD9854 DDS. My appreciation also goes to Mike Pendley, WA5VTV, for his assistance in design of the band-pass filters as well as his ongoing advice.

Conclusion

This series has presented a practical approach to high-performance SDR development that is intended to spur broad-scale amateur experimentation. It is my hope—and that of the ARRL SDR Working Group—that many will be encouraged to contribute to the technical art in this fascinating area. By making the SDR-1000 hardware and software available to the amateur community, software extensions may be easily and quickly added. Thanks for reading.

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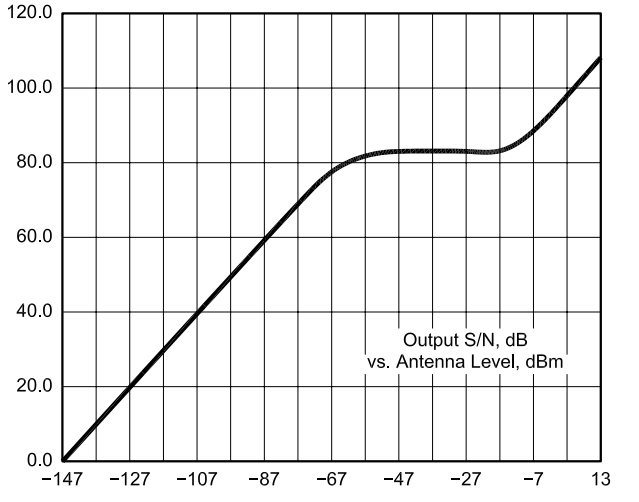

Fig 5—Output signal-to-noise ratio excluding external (atmospheric) noise. INA gain is set to 60 dB. Antenna signal level for saturation is –33.7 dBm.

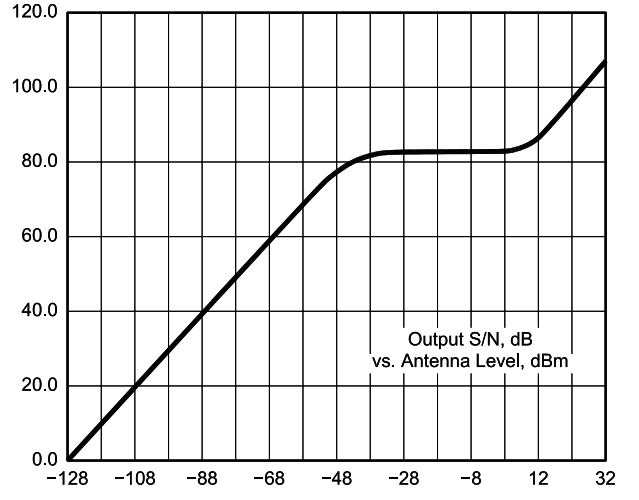

Fig 6—Output signal-to-noise ratio for the 10-m band including external (atmospheric) noise. INA gain is set to 40 dB. Antenna signal level for INA saturation is –13.7dBm.

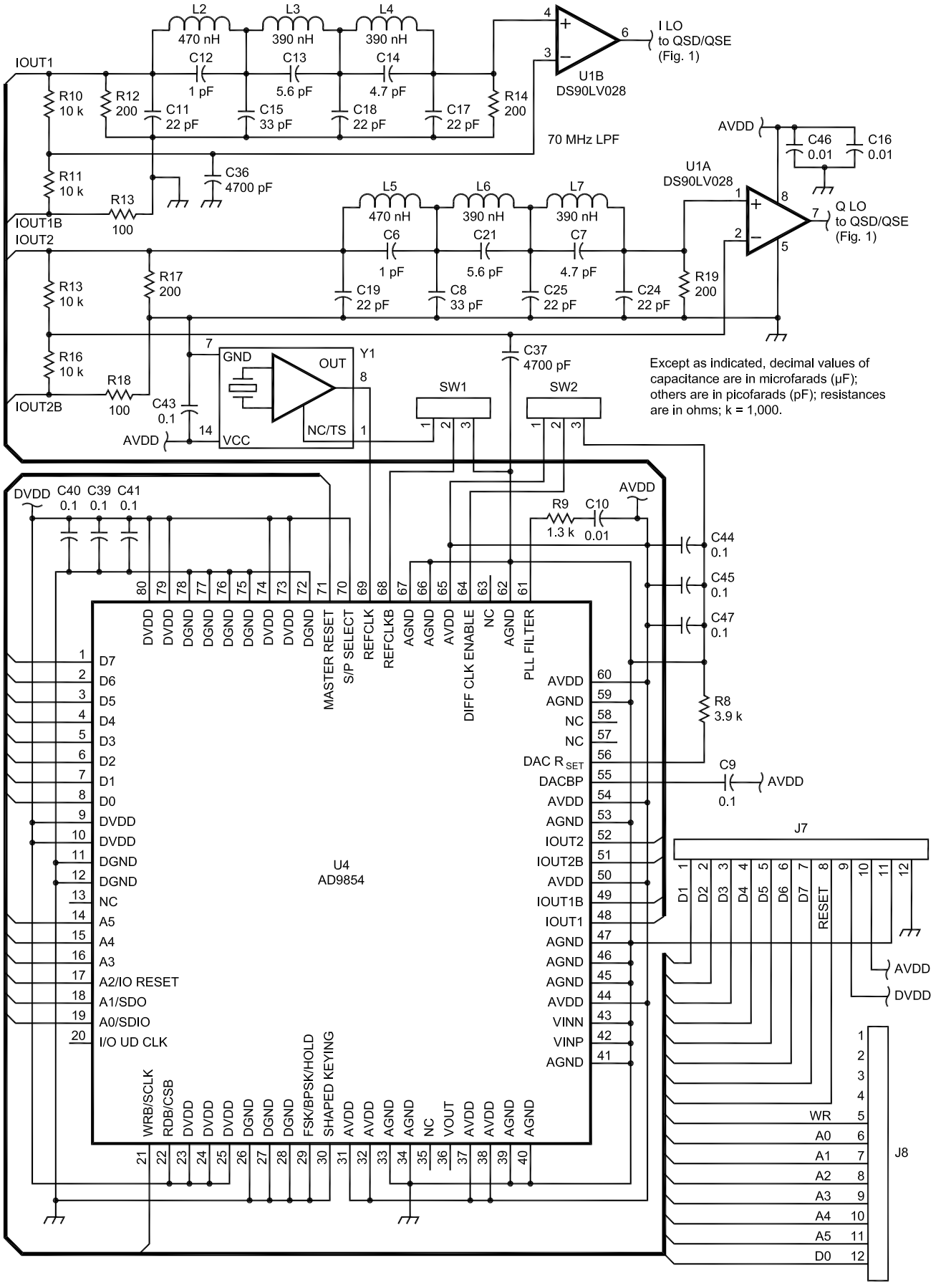

Fig 7—SDR-1000 quadrature DDS schematic.

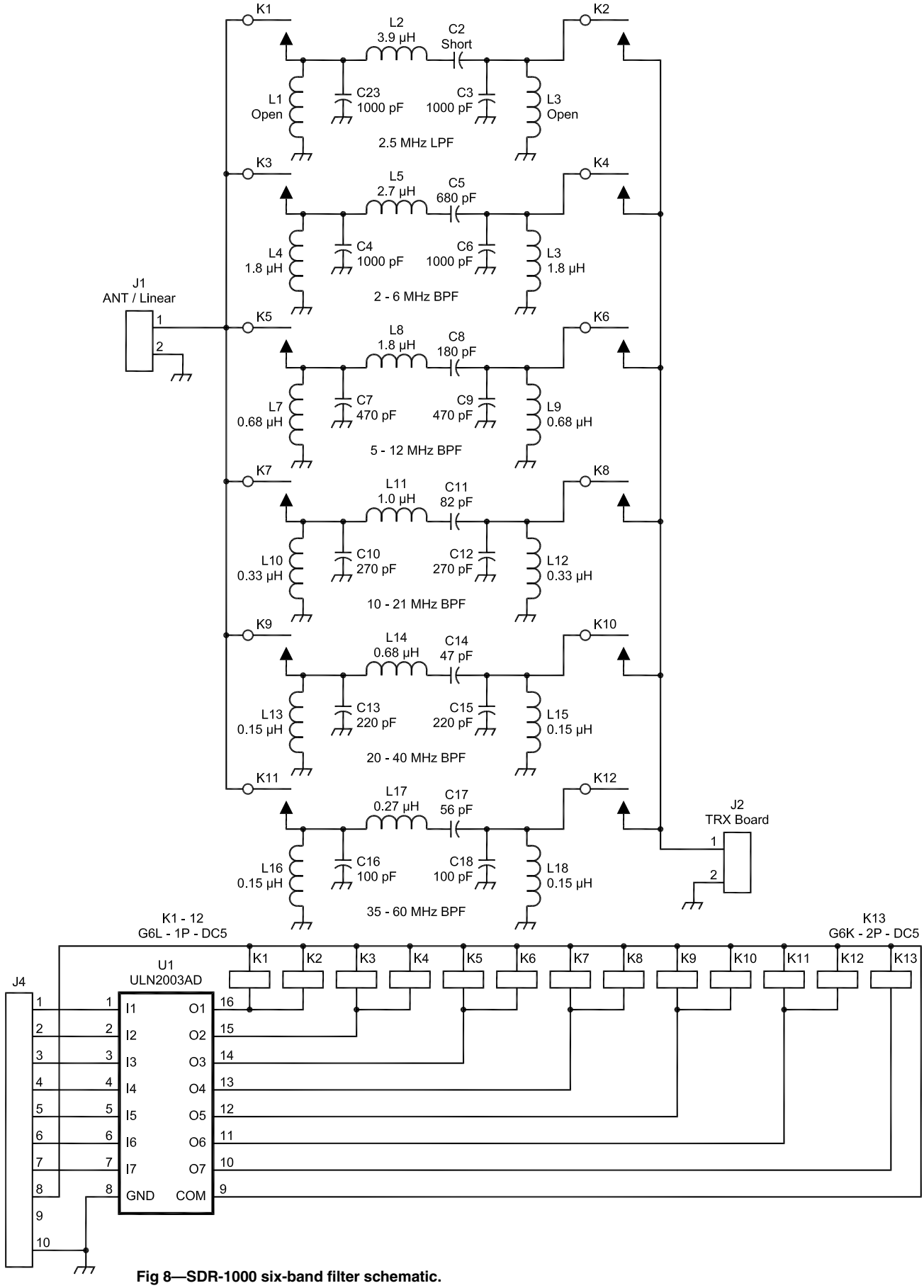

Fig 8—SDR-1000 six-band filter schematic.

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