Ultra High Speed Digital Processing for Wireless Systems using Passive Microwave Logic

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Abstract

This paper proposes two novel high-speed digital logic families that are implemented using passive microwave circuits. The proposed logic gates can process binary information represented in two high frequency carrier modulation formats – Amplitude Shift Keying (ASK), and Binary Phase Shift Keying (BPSK). The fundamental logic gates (NOT, OR, AND) presented for both these data representations can process extremely high speed bit streams (1 - 100 Gbps). The combinational circuits formed from these passive logic gates can operate much faster than traditional electronic gates because they are not limited by the finite carrier mobility that is characteristic of semiconductors. Besides their higher operating speeds, these circuits are well suited for wireless communication systems because they process digital signals in a native high frequency transmission format and it is easy to integrate them with analog RF/microwave circuits.

Introduction

The speed of digital processing becomes more important as carrier frequencies and transmission bandwidths continue to rise in wireless communication systems. The traditional digital circuits that are used in the coding/decoding stages of such systems are limited in speed due to finite carrier mobility in switching semiconductor devices. Silicon-based devices can reach about 1.2 Gbps serial clock rates and even Gallium Arsenide based devices cannot exceed about 7 Gbps.

We propose passive microwave circuits that implement the fundamental Boolean operations NOT, OR, AND. Two logic families are presented: one operating on signals encoded using Amplitude Shift Keying (ASK) and the other operating on Binary Phase Shift Keying (BPSK) signals. These modulation formats are better for high frequency operation because the square pulses seen in traditional digital electronics are distorted at these frequencies. These gates do not use any switching semiconductor circuits because the implementation requires only passive power couplers and phase shifters. Some prior work in the area of passive microwave digital logic has been done by Kouzaev [1].

The logic gate designs presented here are not restricted in frequency range or fabrication technology. They can be implemented for arbitrary carrier frequencies limited only by the cutoff frequencies inherent in the transmission medium.

Designs

Figure 1 shows simplified schematics of the logic gates designed and their corresponding truth tables. In the BPSK gates, the two logic states are distinguished by sinusoids ('A' and 'B') that are 180° out of phase, while in ASK gates the two logic states are distinguished by the presence of a signal ('A') or its absence ('0'). All of these gates are based on wave-interference effects. When an 'A' signal is coupled with a 'B' signal, there is destructive interference, and when two 'A' or two 'B' signals combine there is constructive interference. The power couplers shown in Figure 1 can be implemented in microstrip or stripline, using for example branch line or ring hybrid couplers. The 180° phase shifts are simply $\lambda/2$ lengths of transmission line. The gates are described in more detail below.

BPSK: The NOT gate is simply a length of transmission line corresponding to a 180° phase shift. The operation is fully reversible. The BPSK OR gate consists of two

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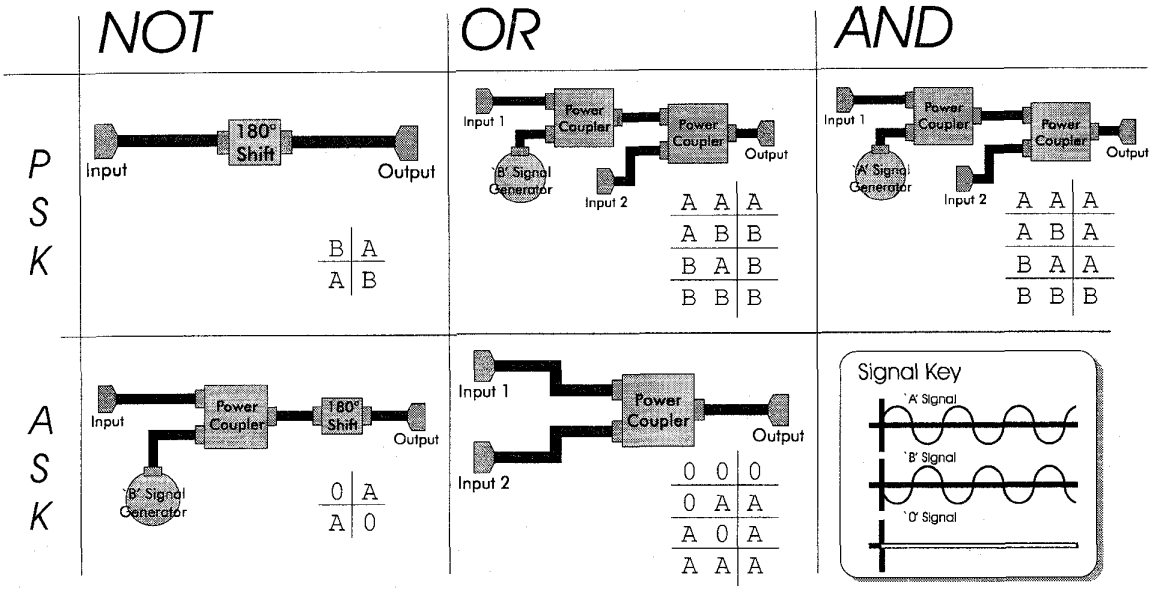

Figure 1: GHz Digital Logic Gate Designs

couplers. If input 1 is 'A', it destructively combines with the 'B' signal at the first coupler so that the output of the first coupler is always '0' which makes the output of the gate the same as input 2. If input 1 is 'B' then it constructively combines with the 'B' signal from the generator at the first coupler to generate a 'B' signal with twice the power as the output of the first coupler. In this case the output of the gate will be 'B' independent of the state of input 2. As can be seen from the designs, the BPSK AND gate is very similar in operation and is a 'dual' of the OR gate.

ASK: In the ASK NOT gate, the input is coupled to a 'B' signal generator and the output of the coupler is phase shifted by 180°. If the input is a '0' signal, the output of the coupler is a 'B' signal which then becomes an 'A' signal because of the phase shift. If the input is an 'A' signal, destructive interference takes place and the output of the coupler is '0' signal which undergoes no change in the phase shifter and emerges as the output of the gate. The ASK OR gate is simply a power coupler. The output is a '0' only if no inputs are presented to the gate and an 'A' signal if one or both inputs is an 'A' signal.

The coupler blocks shown in Figure 1 seem to be three port devices, but all passive microwave couplers are four port networks. There is dissipation of power if only one input presented to a coupler. This results in the signals attenuating as they propagate through cascaded gates. In the worst case half of the power is lost in each gate due to this input-dependent systemic signal degradation (IDSSD). The energy required for the operations is obtained directly from the signals being processed (as power dissipation during destructive interference). In the implementation of these gates, significant power losses are a tradeoff for high speed performance.

One of the advantages of active digital logic over passive logic is that traditional digital electronic signals are regenerated after each gate. There are amplitude variations in the outputs of the passive gates (which can affect performance, particularly in ASK circuits where amplitude level discrimination becomes an issue) and phase variations that will be introduced due to fabrication errors at these high frequencies. To combat the effect of the IDSSD and other variations, active regenerating limiter/amplifier blocks may be needed after four or five cascaded stages of passive logic gates. These active regenerators can be designed to utilize existing microwave analog devices that are capable of operating at extremely high frequencies.

Simulation Results

These circuit designs have been extensively simulated over a wide range of frequencies for implementation in

microstrip and stripline. Some ASK gates have been fabricated, tested and demonstrated previously at 300 Mhz [2]. We are currently working on fabricating and testing higher frequency circuits for both ASK and BPSK. The results shown in this paper are for 10 GHz stripline circuits with a 20-mil ground plane spacing in a dielectric with ε_r of 9.9. The software used for design and simulation was the HP EEsof Series IV Communication Design Suite.

Figure 2 shows simulation results demonstrating the operation of a BPSK AND gate for a carrier frequency of 10 GHz. Five cycles of the carrier wave are chosen to represent one bit, so the circuit operating bit rate is 2 Gbps. The output of the OR/AND gate lags the input changes by one and one quarter carrier cycles. This is due to the physical dimensions of the circuit (5/4 λ) and represents the time delay or latency of the BPSK gates.

Figures 3 and 4 show simulation results for the ASK OR and NOT gates implemented in stripline for a carrier frequency of 10 GHz. The bit rate is again a fifth of the carrier, 2 Gbps. The output in these gates shows a time delay of half a cycle corresponding to the circuit dimensions (λ/2).

Conclusions

Designs for two novel high-speed digital logic families utilizing passive microwave circuits operating on binary information modulated using ASK and BPSK schemes have been presented. Simulations confirming the designs for operating speeds of 2 Gbps have also been shown.

There is room for significant further work in this field, particularly with regard to developing functioning multi-gate combinational circuits, and compatible memory devices. These logic families have a great potential for application in wireless communication systems because of their high operating speeds, processing of data in high frequency transmission formats and ease of integration with analog microwave circuitry.

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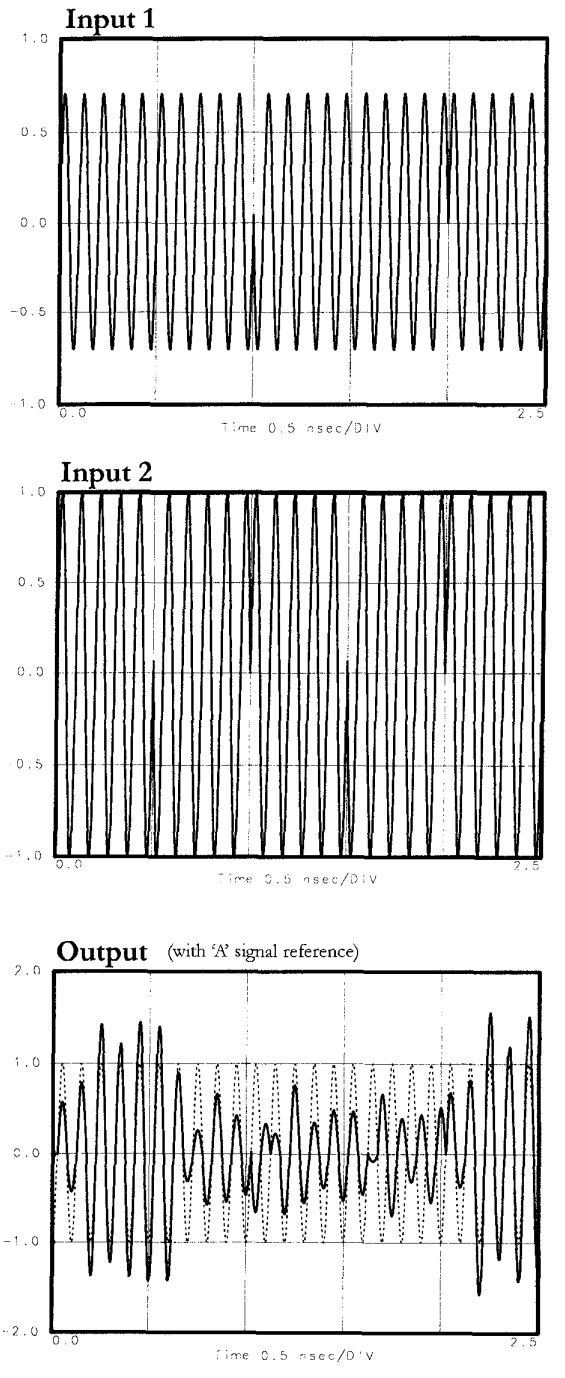

Figure 2: Simulated PSK AND Gate Results (10 GHz, 2 Gbps)

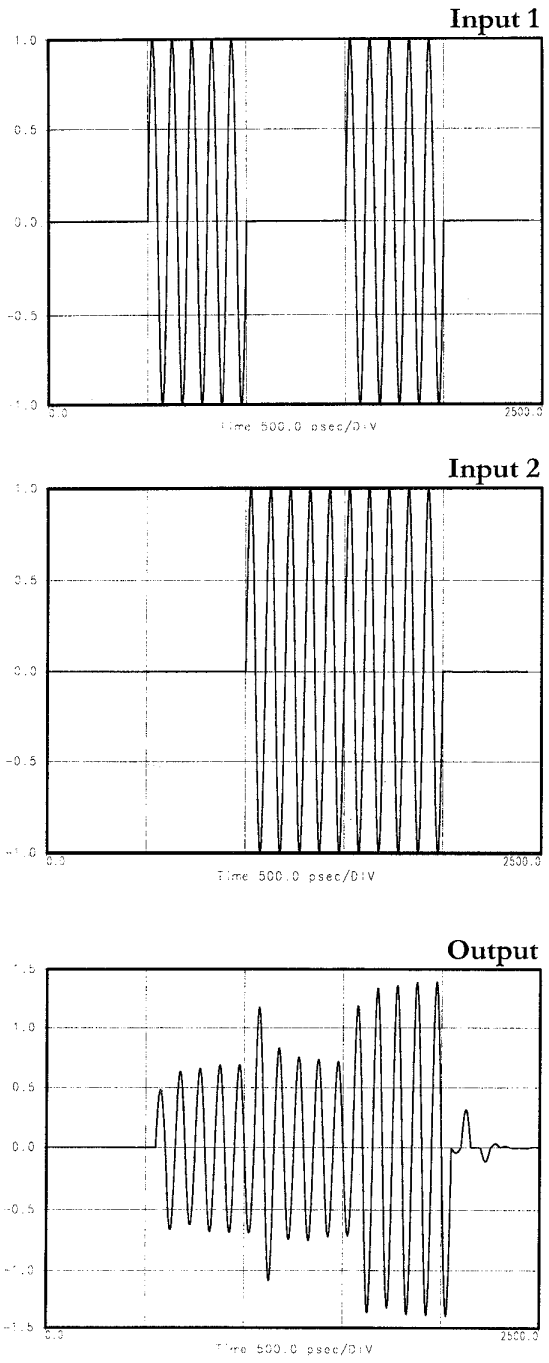

Figure 3: Simulated ASK OR Gate Results (10 GHz, 2 Gbps)

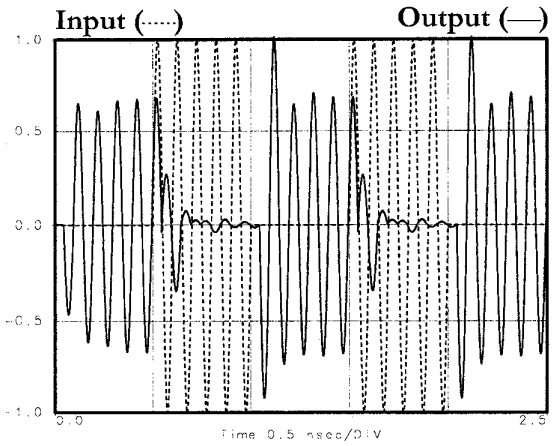

Figure 4: Simulated ASK NOT Gate Results (10 GHz, 2 Gbps)

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