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Highly Linear and Highly Efficient Dual-Carrier Power Amplifier Based on Low-Loss RF Carrier Combiner

Kenle Chen, *Student Member, IEEE*, Eric J. Naglich, *Student Member, IEEE*, Yu-Chen Wu, *Student Member, IEEE*, and Dimitrios Peroulis, *Member, IEEE*

***Abstract*—This paper presents a novel power amplifier (PA) architecture for amplifying dual-carrier signals with simultaneous high efficiency and high linearity. This dual-carrier PA is based on two high-efficiency PAs and an innovative RF carrier combiner, which is a diplexer implemented with bandstop filters (BSFs). This special BSF diplexer is capable of combining two carriers with ultra-narrow frequency spacings, e.g., down to 0.25% fractional bandwidth, while maintaining a low combining loss of <1 dB. Compared to conventional diplexers implemented with bandpass filters, this new technology leads to minimized resource usage for achieving the same combining performance. The integrated PA exhibits excellent performance when amplifying dual-carrier signals in terms of linearity and efficiency. Specifically, third-order intermodulations of <40 dBc were measured with 70.2% (60.8%) power-added efficiency for carrier spacing of 10 MHz (5 MHz).**

***Index Terms*—Bandstop filter (BSF), diplexer, dual band, dual carrier, efficiency, GaN, linearity, power amplifier (PA).**

I. Introduction

As THE wireless communication technology keeps evolving, multi-carrier schemes are being incorporated into today's communication standards, e.g., global system for mobile communications (GSM), code division multiple access (CDMA), high-speed packet access (HSPA), and long-term evolution (LTE). Compared to the conventional single-carrier technology, multi-carrier schemes significantly enhance the data transmission speed, spectrum access efficiency, and user capacity [1]–[4]. However, this multi-carrier operation is also accompanied by many practical challenges in the design and realization of high-performance, low-cost, and low-complexity hardware. For example, the simultaneous requirements of efficiency and high-linearity pose significant challenges to multi-carrier transmitters.

Existing solutions for amplifying multi-carrier signals are typically based on two different philosophies, as shown in Fig. 1: (a) using a single broadband power amplifier (PA) covering all carriers that have been combined at the IF module [5]–[9] and (b) having each of the single carriers supplied to different narrowband PAs and combined at the output [10]. For the first solution, the multi-carrier signal introduces large envelope fluctuation leading to low average PA efficiency and increased linearization complexity. On the other hand, the second approach mainly suffers from considerable combining loss because each time the signals are combined, the output power drops by at least 50% given $\geq$3-dB loss for a typical planar combiner [10] (e.g., Wilkinson Combiner or 180° hybrid combiner [11]). The multiplexer can be considered as a promising solution for combining different carriers. However, the frequency spacing between two nearby carriers is normally very small [2], typically <10 MHz due to the limited spectral access for one single network operator, thus requiring very high order filters with ultra-steep stopband responses, and high quality factor for low insertion loss (IL). This may lead to increased implementation difficulty and performance degradation.

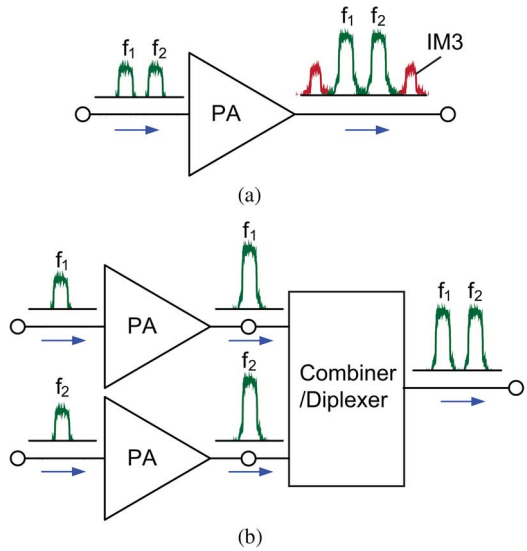

Fig. 1. Power amplification of multi-carrier signals. (a) Carriers combined at IF before feeding into PA. (b) Carriers combined at PA outputs.

In this paper, efficient and linear amplification of dual-carrier signals is investigated based on a novel carrier combiner. Specifically, high-Q (>2000) bandstop filters (BSFs) [12]–[15] are for the first time utilized to implement a diplexer capable of effectively combining two frequency components with ultra-

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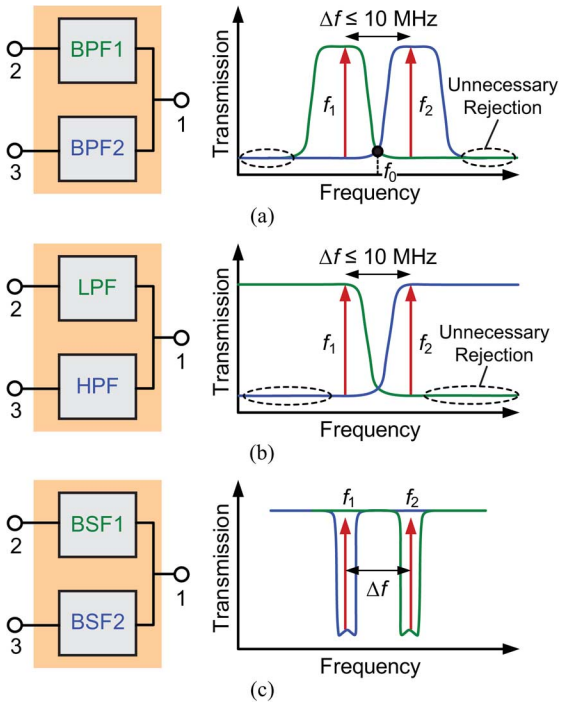

Fig. 2. Implementation of diplexer using different filter types for combining the carriers. (a) BPFs. (b) LPFs and HPFs. (c) BSFs.

small frequency separation, e.g., down to 5 MHz, which is difficult to achieve by regular bandpass diplexers. A demonstration dual-carrier PA, in which the diplexer is realized with two second-order BSFs, is described in this paper. The integrated dual-carrier PA exhibits very good linearity performance with $<$40 dBc of high-order intermodulation components and high power-added efficiency (PAE) of up to 71%. These promising results reveals that the proposed PA architecture yields an effective solution for linearly and efficiently amplifying dual-carrier signals. For applications in the real communication systems, e.g., GSM, CDMA, and HSPA, this technology significantly relieves the burdens for efficiency enhancement [e.g., envelope tracking (ET)] and external linearization [e.g., digital pre-distortion (DPD)], simplifying both the hardware and software implementations at system level. These benefits can eventually be transferred to reduced costs in research and development and manufacturing.

II. Design and Implementation of Diplexer With Ultra-Narrow Frequency Spacing

A. Comparison of Diplexer Implementation With Different Filter Types

A diplexer is a three-port device that can combine/split signals from/into different communication channels, e.g., transmitter and receiver channels. As shown in Fig. 2, it consists of two filters whose passbands fall on the stopbands of each other, while these two filters are properly designed and connected through an optimized T-junction. Regularly, bandpass filters (BPFs) are utilized to build diplexers [16]–[20], as shown in Fig. 2(a). Alternatively, in some cases, a pair of low-pass filters (LPFs) and high-pass filters (HPFs) can also be the solution [21]–[23], as illustrated in Fig. 2(b). However, when the frequency spacing is small (typically $<$1% fractional spacing for two carriers), very steep stopband responses are needed, requiring very high filter order. For example, to achieve 30-dB isolation (IS) at $\Delta f = 10$ MHz (centered at 2 GHz), at least a ninth-order BPF with 1% fractional bandwidth is needed with $>$5000 quality factor to maintain $<$0.5-dB IL. For the LPF and HPF case, $>$15th-order filters are required to achieve the same amount of IS. These results are obtained from Agilent Technologies' Advanced Design System (ADS, [24]) simulations using its symbolic filter models, as summarized in Table I.

TABLE I
Requirements of Different Filter Types for Achieving the Same IS

Filter*	f_0	Δf	Isolation	Order	Q_u
BPFs	2GHz	10MHz, 0.5%	30 dB	9	5000
LPF&HPF	2GHz	10MHz, 0.5%	30 dB	$>$15	$>$3000
BSFs	2GHz	10MHz, 0.5%	30 dB	2	2500

$*$ These values are calculated using symbolic filter models in ADS.

It is important to note that if we only consider combining two narrowband carriers, the redundant frequency selectivities [or band rejections indicated in Fig. 2(a) and (b)] and wide passband are not necessary. To lift these restrictions, the IS can be concentrated to only the unwanted carrier frequencies, respectively, leading to the case of BSFs, as shown in Fig. 2(c). In this way, the optimal solution can be achieved with the lowest circuit complexity and quality factor, as no unnecessary rejection bands are imposed on the filters. From ADS simulations, only second-order BSFs and 2500 quality factor are sufficient for yielding 30-dB IS under the identical frequency conditions, as displayed in Table I.

The above analysis are all based on regular symmetrical filter models. Actually, the filters can be modified in order to be more suitable for diplexer implementation. For example, unsymmetrical stop responses (with steeper skirt toward the passband of the other BPF) are normally formulated to further enhance the IS for very small guard band (down to 5 MHz) between two frequency bands [18], [25]. However, it still requires very high filter order (e.g., $n = 7$ in [25]) to assure sufficient stopband attenuation.

B. Diplexer Design Using High-Q_u Evanescent-Mode (EVA)-Cavity BSFs

Fig. 3 shows the topology of the proposed diplexer. In this design, the diplexer consists of two second-order BSFs whose rejection bands are placed at one of the two carrier frequencies, f_1 and f_2, respectively. The equivalent circuit model of the BSF is shown in Fig. 3, which is built using two coupled resonators connected through a $\lambda/4$ line serving as the source-to-load coupling structure. This BSF is physically realized using high-Q EVA cavities, as shown in Fig. 3.

The cross-sectional view of the EVA cavity is shown in Fig. 4. It is constructed by placing a loading post at the center of a regular cylindrical cavity. Therefore, the electrical field is concentrated between the post and the bottom wall, which is attached to the copper cavity using screws. This parallel-plate geometry creates the dominant effective capacitance of the resonator tank. The magnetic field is distributed circularly

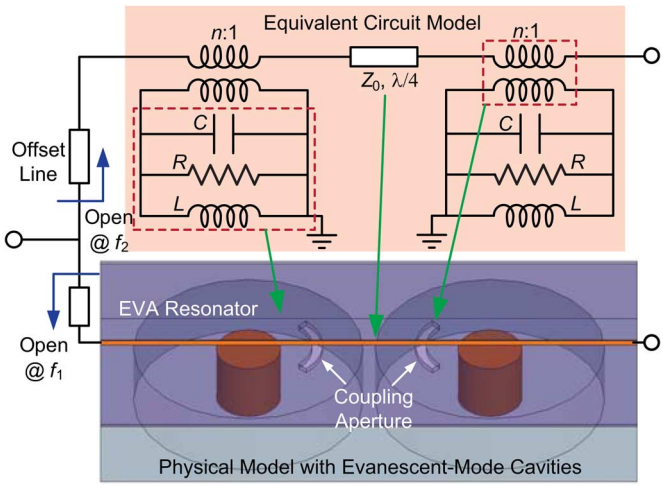

Fig. 3. Schematic of diplexer implemented using BSFs, showing the equivalent-circuit and physical models based on EVA cavities.

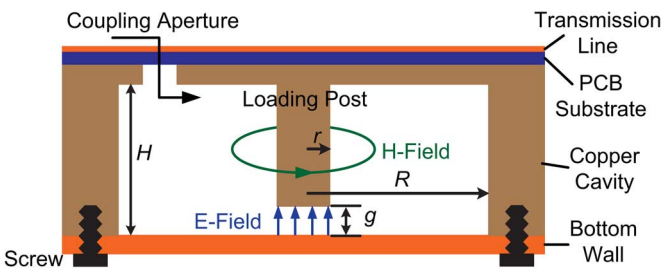

Fig. 4. Cross-sectional view of the EVA cavity.

between the center post and the side boundary. Such a coaxial structure can be treated as a short-ended transmission line, forming the dominant effective inductance. The loss tangent of this resonator is represented as a parallel resistor of the resonator circuit model in Fig. 3. This type of resonator can yield very high unloaded quality factor (Q_u) ranging from 500 to 2000 in [26]–[29] and has been extensively utilized to realize narrowband filters [26]–[29]. Fig. 5(a) shows the frequency response of one of these two BSFs with a spectral notch at $f_1 (= 2\ \text{GHz})$. The results are obtained from simulation with the equivalent circuit model using ADS. Fig. 5(a) also illustrates the definition 3-dB bandwidth of a BSF, indicating the frequency range in which S_{21} drops to $\geq$3 dB lower than the passband. In this design, the 3-dB bandwidth is around 4.3 MHz, slightly lower than Δf, as the carriers' bandwidth should be smaller than their spacing Δf by default. In most applications, the carrier frequency is on the order of several megahertz [2], [3].

When integrated into the diplexer, the notches of these two BSFs are designed to present an open circuit (O.C.) at the combining node. This is physically achieved by properly tuning the offset line length, as illustrated in Fig. 3. In this way, each of the BSFs rejects an unwanted carrier while not affecting the transmission feature of the other path. The inset of Fig. 5(a) shows the input impedance (Z_{in}) of the designed BSF versus frequency. It indicates that the notch at f_1 corresponds to the O.C. point, while the other carrier frequency of f_2 (in this case, $\approx$ 2.005 MHz) falls in the passband of the filter. In this case, the IL of one path is determined jointly by the IS of the BSF in the other

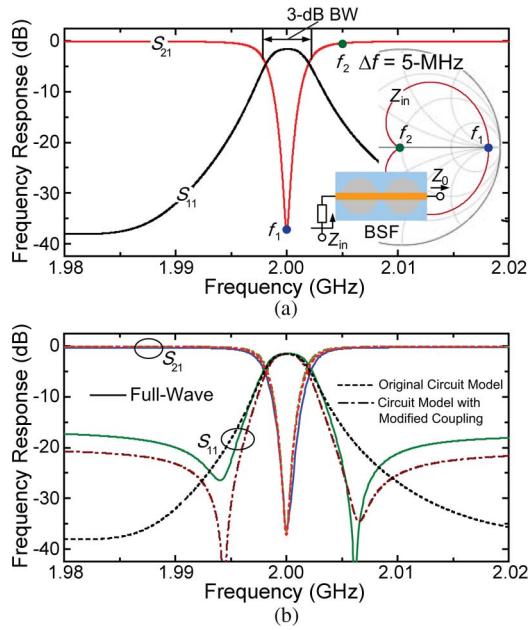

Fig. 5. Simulated frequency response of the designed two-pole BSF extracted from: (a) circuit simulation and (b) full-wave simulation.

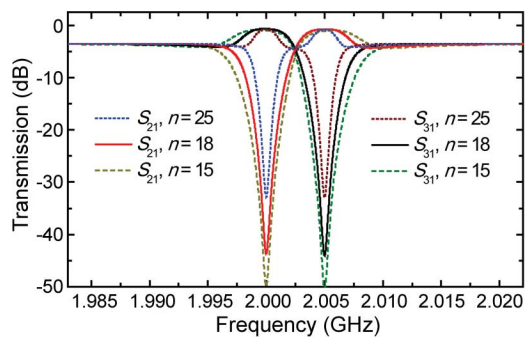

Fig. 6. Frequency response of diplexer's transmission coefficients under different transformation ratios, n.

path and the IL of the BSF in the same path, which can be expressed as

$$\text{IL}_{DPX} \approx \text{IL}_{\text{BSF1}} + \frac{1}{\text{IS}_{\text{BSF2}}} \approx \text{IL}_{\text{BSF2}} + \frac{1}{\text{IS}_{\text{BSF1}}}. \quad (1)$$

For the BSF topology shown in Fig. 3, IS and bandwidth of one BSF are both determined by the impedance transformation ratio n, given a specific frequency spacing of two carriers (Δf) and a constant quality factor of the resonators. Therefore, the transformation ratio plays a crucial role in determining the IL of each path. Fig. 6 shows the frequency response of the integrated diplexer under different transformation ratio n, which strongly impacts both the passband and stopband features of the two paths of the diplexer. These results are extracted from ADS simulation with the circuit model in Fig. 3. Fig. 6 also underlines that the coupling ratio n can be optimized according to different carrier bandwidths.

Fig. 7(a) summarizes the calculated BSF bandwidth and IS versus n. It can be seen that the 3-dB bandwidth is solely dependent on n, when Q is fixed, indicating that a stronger coupling (smaller n) leads to a wider bandwidth. The IS is determined jointly by n and Q_u. Fig. 7(b) depicts the relation between n and the IL over one path of the diplexer. It emphasizes that

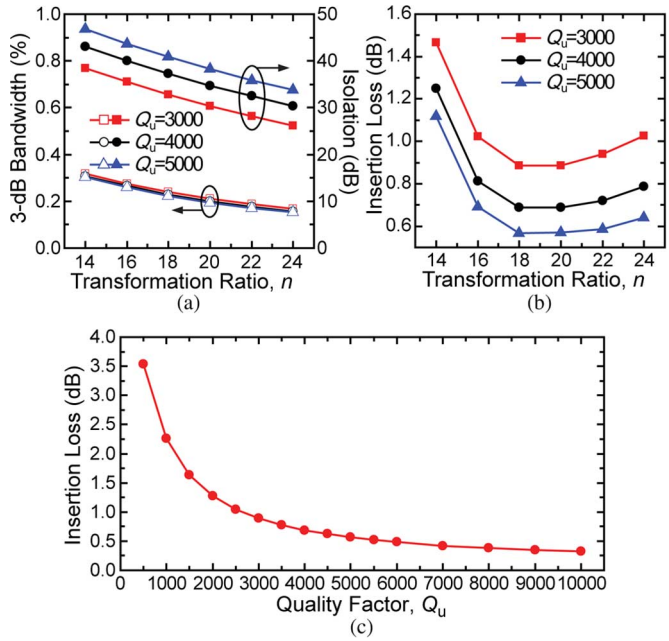

Fig. 7. Design tradeoff for the entire BSF diplexer. (a) Bandwidth and IS versus n. (b) IL versus n. (c) IL versus Q_u.

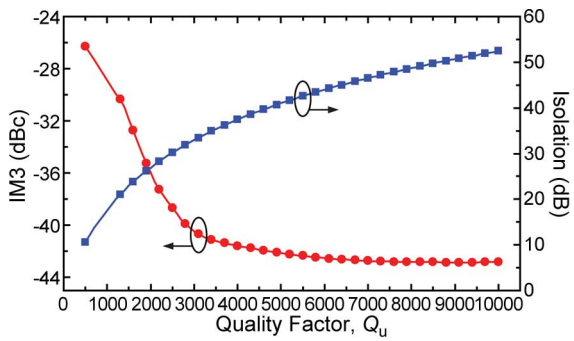

Fig. 8. Design tradeoff at system level: IM3 and IS versus Q_u.

the minimum IL is achieved around an optimal coupling value of $n = 18$. Another study is then performed on the IL of the diplexer versus resonator quality factor with an optimized value of n, as shown in Fig. 7(c). It can be seen that the IL decreases sharply as Q_u increases from 500 to 2500, above which the IL is below 1 dB and its degradation substantially. The results exhibited in Fig. 7(c) basically suggest that a tradeoff between Q_u (size) and IL can be conducted according to different target applications, while a good balance can be considered with Q_u between 3000–6000. To obtain $Q_u > 6000$, unloaded cavities are basically required, leading to significantly increased size.

Besides IL, another important consideration in diplexer design is overall system performance when it is integrated with the PAs. At system level, the concern is mainly focused on nonlinearities introduced by the combined PAs and diplexer. By diplexing two regularly designed high-efficiency PA, the third-order intermodulation (IM3) products at deeply saturated power level (high-efficiency mode, extremely nonlinear) are extracted using ADS simulation, shown in Fig. 8. The detailed design and implementation of the high-efficiency PA is described in Section III. It indicates that IM3 is mainly determined by the IS of the BSF filters, which is varied by changing the resonator's Q_u as n is now fixed to 18 to minimize the IL. As

TABLE II
DIMENSIONAL PARAMETERS OF EVA CAVITY

Parameter	Value
Cavity Radius R	21.5 mm
Cavity Depth H	12 mm
Post Radius r	$0.38R$ mm
RF Gap g	1.0 mm
Simulated Q_u	3500

the IS is increased to above 40 dB ($Q_u \geq 5000$), the IM3 approaches to a constant level of around -43 dBc. Since several standards require down to -40 dBc of adjacent channel leakage ratio (ACLR) at frequency offset beyond 10 MHz, e.g., WLAN and LTE, the target IM3 level in this design is set to -40 dBc. This means that a Q_u of >2800 is sufficient to meet the linearity requirement. If a certain communication standard require further low out-of-band emission, e.g., below 43 dBc, the PA needs to operate in a more linear mode to further degrade IM3.

C. Diplexer Implementation

Taking into account both IL, linearity, and realizability, in this design Q_u of around 3500 is eventually selected to implement the diplexer, which is realized by optimally constructing the geometry of the EVA cavity [28]. The physical model of the BSF is established and simulated using ANSYS's High Frequency Structure Simulator (HFSS). The simulated results are shown in Fig. 5(b), indicating good agreement with the circuit simulation. The discrepancy of S_{11} is mainly due to the nonideal effect of the coupling aperture. By modifying the impedance of transmission lines near the transformers, the circuit-schematic simulation results are in better agreement with the physical model, as shown in Fig. 5(b). The final dimensions of the designed EVA cavity are summarized in Table II.

Fig. 9(a) shows the simulated S_{21} and S_{31} of the integrated BSF diplexer, exhibiting the desired passbands and stopbands at f_1 and f_2, respectively. For frequencies other than the f_1 to f_2 band, this circuit acts as a regular 3-dB T-junction combiner/divider. It can also be seen from Fig. 9(a) that the simulation results of the circuit model and full-wave model match each other well, further validating the robustness of the model. The full-wave simulated IL is around 0.80 dB, which approximately corresponds to Q_u of 3500. Fig. 9(b) shows the reflection coefficient at the combining node (Port1) and the IS between Port2 and Port3. It can be seen that higher than 40 dB of IS is achieved around f_1 and f_2, respectively.

D. Fabrication and Experimental Results

The designed BSF diplexer is fabricated, as shown in Fig. 10(a) and (b). The cavities, posts, and coupling apertures are defined in a copper substrate, while a Rogers 5880 printed circuit board (PCB) with transmission line structures on it is laminated on the top of the copper substrate. The cavities are then sealed by attaching two metal plates onto the bottom of the substrate, which are fixed using screws. The entire diplexer is measured using a multi-port performance network analyzer (Agilent E8361C). Fig. 11(a) shows the measured transmission

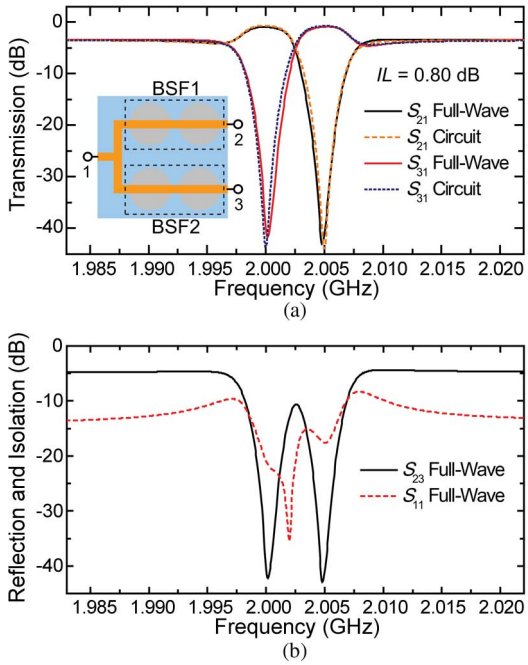

Fig. 9. Simulated frequency response of the designed BSF diplexer. (a) Transmission coefficients. (b) Reflection and IS coefficients.

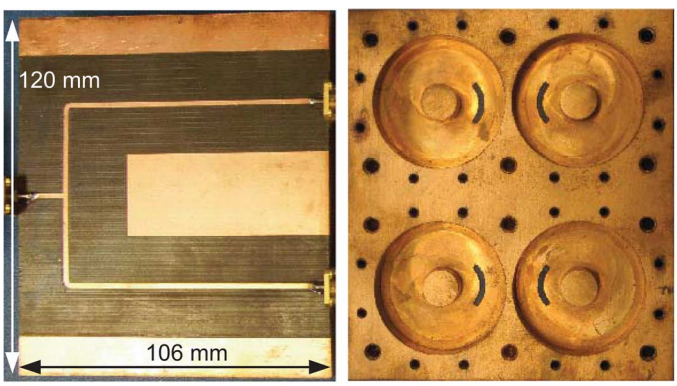

Fig. 10. Fabricated diplexer. (a) Front side. (b) Back side before sealed.

coefficients versus frequency with $\Delta f = 5$ MHz (same condition as the design presented in Fig. 9). The measured results agree well with the simulation, except the measured ISs are reduced to around 31 dB. This is mainly caused by the reduced quality factor of the fabricated EVA cavity resonator and weak coupling (electromagnetic (EM)-field leakage) between two resonators induced by fabrication imperfections, e.g., surface roughness. The measured IL is around 1.01 dB, and the corresponding Q_u of the fabricated EVA resonator is around 3000. Compared to the other regular diplexers based on high-Q BPFs (e.g., [18] and [25]), this design leads to smaller size given the similar frequency and Q factor due to the fact that the number of resonators have been significantly reduced.

In addition, this design is slightly modified by tuning f_2 to 2.01 GHz ($\Delta f = 10$ MHz), which is physically realized by changing the gap distance of the EVA resonators of the BSF1 depicted in the inset of Fig. 5(a). The measured results are plotted in Fig. 11(b). The IL improves to 0.73 dB because each of the carrier frequencies, i.e., f_1 or f_2, is located farther away

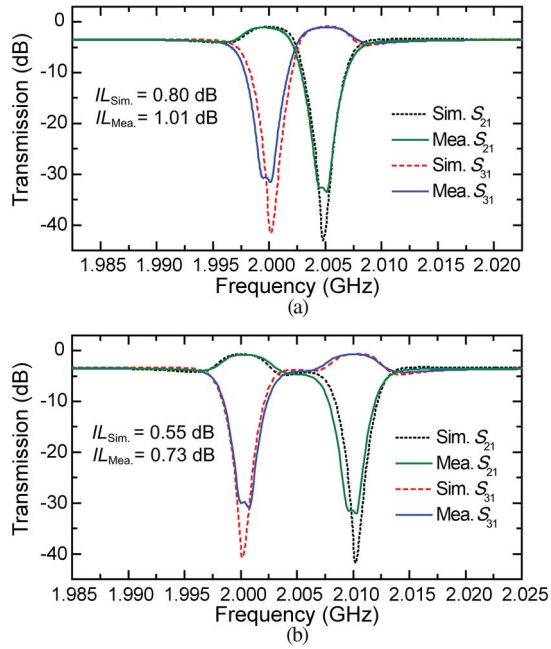

Fig. 11. Measured and simulated frequency response (transmission coefficients) of the fabricated BSF diplexer. (a) $\Delta f = 5$ MHz. (b) $\Delta f = 10$ MHz.

from the BSF's notch in its passing path, leading to enhanced transmission. The reflection coefficients of all three ports of the diplexer are plotted in Fig. 12, indicating the pole location of each of the BSFs. It is important to highlight that this BSF diplexer is capable of dynamically combining carriers from two arbitrarily different frequencies if the BSFs are made to be electrically or mechanically reconfigurable [15], [29]. Moreover, the carrier bandwidth can also be adjustable by incorporating additional tunability into the coupling structures, such as the method presented in [28].

III. Highly Efficient PA

A. Design

To demonstrate the entire concept, high-efficiency saturated-mode PAs [31], [32] are realized. GaN transistors (Cree CGH40006, 6 W) are utilized as the RF power device. In this work, we follow the typical design procedure of a saturated PA, which has been detailedly described in [32]. The design starts with transistor modeling based on the large-signal model supplied by the vendor, which also includes parasitics of the packaged GaN transistor. Load–pull simulations are carried out using ADS to obtain the optimal fundamental and harmonic loads. The desired load impedances are summarized in Table III.

The PA circuit schematic is shown in Fig. 13, indicating the input and output matching networks. Optimal second and third harmonic loadings are performed using two open-circuited stubs, which are quarter-wavelengths at $2f_0$ and $3f_0$, respectively. They present short circuit at the central node $2f_0$ and $3f_0$, respectively, and they are connected to the GaN transistor through a tuning line, which transforms the short-circuit node to the desired inductive harmonic loads. By using this method, the harmonic loading and fundamental matching are separated. The fundamental load matching is then conducted using the

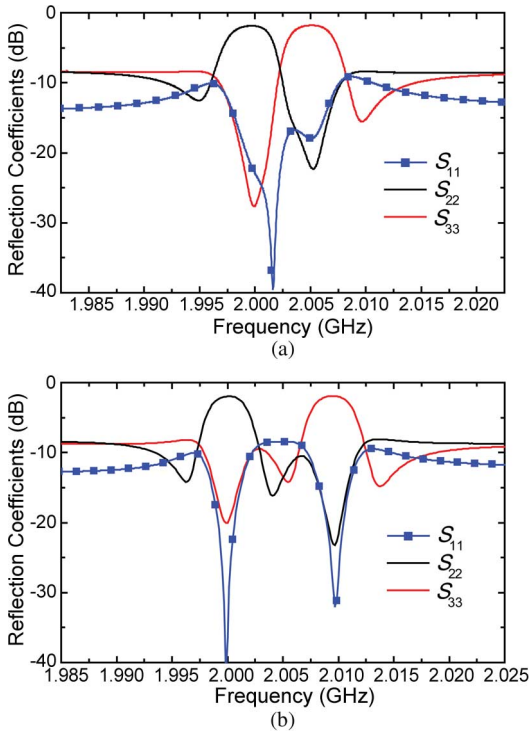

Fig. 12. Measured reflection coefficients of the fabricated BSF diplexer. (a) $\Delta f = 5$ MHz. (b) $\Delta f = 10$ MHz.

TABLE III
OPTIMAL LOAD AND SOURCE IMPEDANCES OF THE GaN TRANSISTOR IN THE HIGH-EFFICIENCY PA DESIGN

Load	Fundamental	2nd	3rd
$Z_{\mathrm{L,Opt.}}$	$15+5j$	$34.8j$	$61j$
Z_{OMN}	$15.2+4.8j$	$0.5+35.8j$	$1+66.5j$
$Z_{\mathrm{S,Opt.}}$	$5+1.2j$	N/A	N/A
Z_{IMN}	$5.4+1.5j$	N/A	N/A

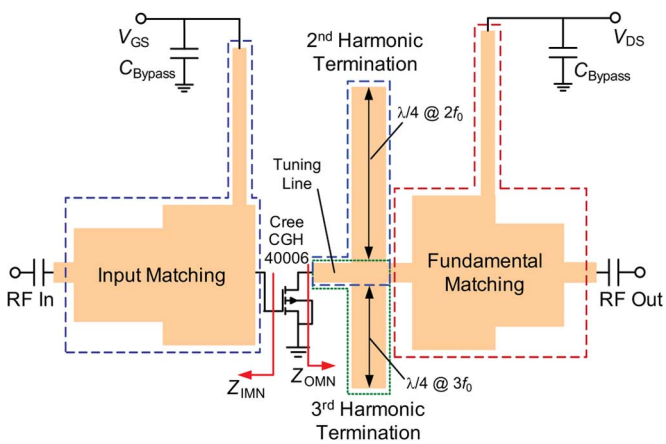

Fig. 13. Circuit schematic of the designed high-efficiency PA.

network shown in Fig. 13, in which the biasing circuit is also included. The designed PA is eventually co-optimized with the diplexer to perfect the overall performance because the diplexer input may slightly deviates from 50 Ω due to the limited IS of the other path. Since the harmonic loadings are separated to the external circuit, the co-optimization is mainly focused on the fundamental matching circuits. The finalized design parameters

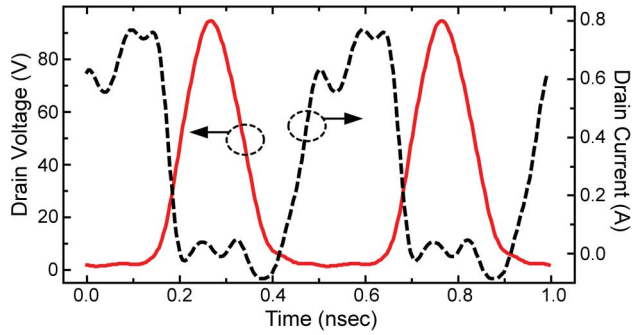

Fig. 14. Simulated voltage and current waveforms at the intrinsic drain plane of the transistor.

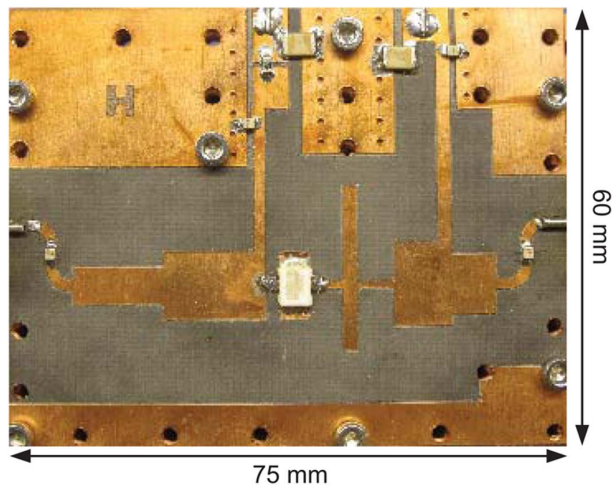

Fig. 15. Fabricated high-efficiency PA.

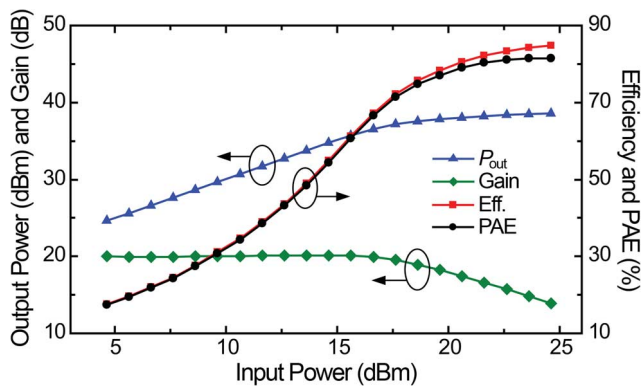

Fig. 16. Measured PA performance versus input power at 2 GHz.

of the output matching network are listed in Table III, including the load impedances at the first three frequency components.

For the source matching, the optimal source impedance is extracted from source–pull simulation. In this case, only the fundamental impedance is considered, which is provided by the input matching circuit, as shown in Fig. 13. The designed PA circuit is simulated using ADS's harmonic balance (HB) simulator. Fig. 14 shows the waveforms of voltage and current at the intrinsic drain of the transistor when the PA is operating at the saturated power level of around 6 W. It clearly illustrates a saturated behavior of this PA with a half-sinusoidal voltage waveform and a slightly bifurcated current waveform [31], [32], corresponding to a very high efficiency of 86%.

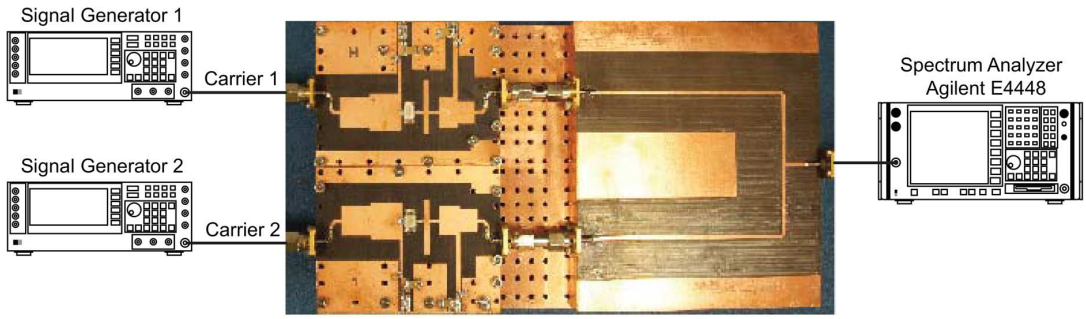

Fig. 17. Fabricated dual-carrier PA and testing setup.

B. Implementation and Experimental Results

The designed PA circuit is fabricated, which is shown in Fig. 15. The amplifier stability is enhanced using a 250-Ω resistor connected to the gate bias line. The drain node of the transistor is biased at 28 V. The gate bias is set to −2.8 V, slightly below the threshold (≈ −3.3 V) for the maximized PAE. This results in a quiescent bias current $I_{\rm DS}$ of around 100 mA. The measured PA performance versus input power is plotted in Fig. 16. It can be seen that the highest PAE of 81.6% occurs at an input power of around 23 dBm, roughly corresponding to the 3-dB gain compression point with 85% efficiency, 38.5-dBm output power, and 15-dB gain. These results are consistent with state-of-the-art PAs [32]–[34] to the authors' best knowledge.

IV. Integration and Measurement of the Entire Dual-Carrier PA

Fig. 17 shows the integrated module of the dual-carrier PA. The standalone PAs and the diplexer are connected through two adaptors, allowing independent prescription of each parts in advance of integration. The testing setup is also shown in Fig. 17. It can be seen that two carriers are generated using two signal generators (Agilent 4433B) and the output signal is measured by a spectrum analyzer.

A. Continuous-Wave Evaluation

When the PAs are integrated with the diplexer, the overall efficiency of the entire module is determined by the diplexer's IL, which is dependent, in this implementation, on the frequency spacing of carriers and also BSFs' notches, Δf. Fig. 18 plots the simulated and measured IL (IL) of the diplexer as a function of Δf. It can be seen that IL deceases sharply with Δf until it reaches a saturated value for $\Delta f > 10$ MHz, which means that the frequencies of the transmitted carriers are located completely out of the BSFs' notches since the notch introduces IL only when the passband is too close to it. Accordingly, the overall efficiency (at saturated power) has an oppositely similar behavior with respect to Δf, as shown in Fig. 18.

Unlike a conventional BPF diplexer, the BSF diplexer is not capable of rejecting out-of-band spurs, such as harmonics and clock feed-through. However, the PA itself is capable of offering sufficient attenuation to these high-frequency spurs since the contemporary high-efficiency PAs are mostly designed using output matching networks with very strong filter behaviors (either low-pass [31] or bandpass [30]). Fig. 19 shows the simulated harmonics of the integrated PA in this research, indicating −40 and −50 dBc of second and third harmonics at saturated power level, respectively. These harmonics level are already very low and may not require further attenuation from the diplexer. It is also interesting to note in Fig. 19 that these standalone PAs actually presents higher harmonic levels in the independent evaluation. This due to the fact that the harmonic loadings of these two PAs provide extra rejections to each others' harmonics.

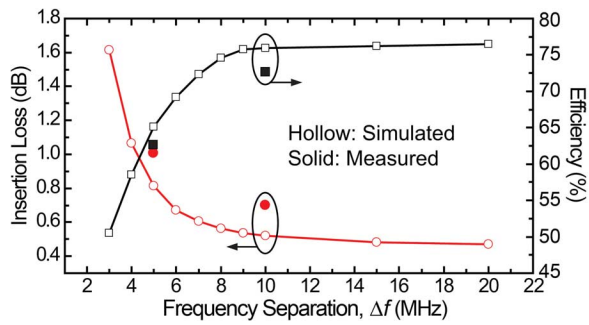

Fig. 18. Simulated and measured diplexer IL and overall efficiency versus frequency spacing, Δf.

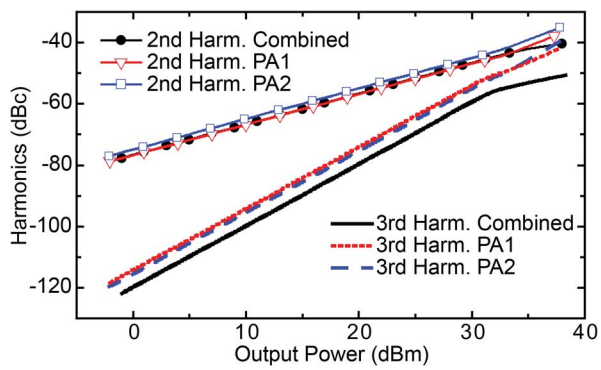

Fig. 19. Simulated harmonics of combined PA in comparison with independent PAs.

Fig. 20(a) and (b) shows the measured spectra corresponding to the two measured data points in Fig. 18 with 5- and 10-MHz Δf, respectively. The measured PAE is 60.8% (72.8% MHz) for $\Delta f = 5$ MHz (=10 MHz) with high-order intermodulation components smaller than −40 dBc for both cases. These small intermodulation products are basically due to the finite IS between the two paths. Fig. 21 shows the measured performance of the dual-carrier PA as a function of the input power of each carrier, $P_{\rm in}$, where $P_{\rm out}$ represents the average output power of two carriers. It can be seen that PA saturation starts at an input carrier power of $P_{\rm in} = 18$ dBm, which accompanied by a sudden jump of the IM3 from ≈ −53 dBc to ≈ −40 dBc. The

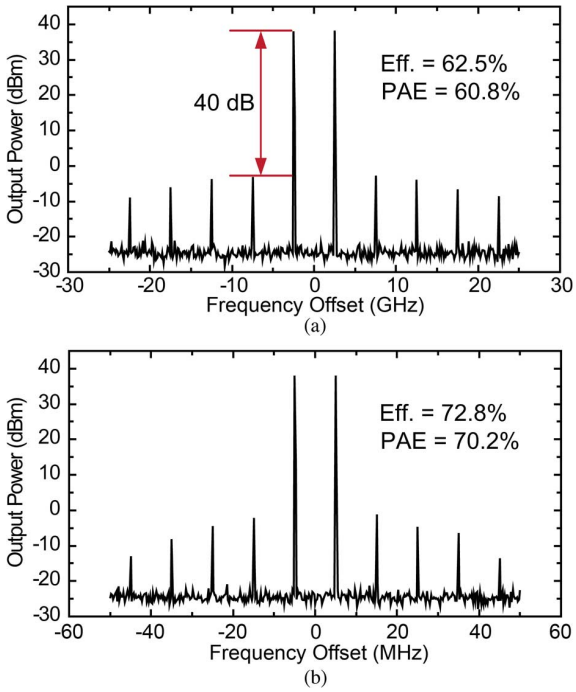

Fig. 20. Measured output spectrum of the dual-carrier PA with: (a) $\Delta f = 5$ MHz and (b) $\Delta f = 10$ MHz.

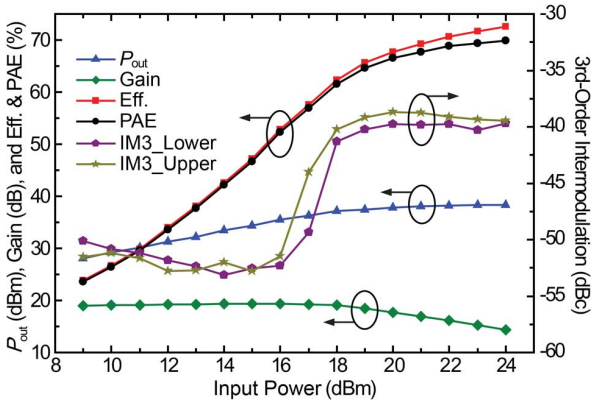

Fig. 21. Measured performance of the dual-carrier PA under the stimulus of a power-swept input signal.

highest PAE is achieved at roughly the 3-dB compression point with $P_{\text{in}} = 24$ dBm. Subsequently, we tested the dual-carrier PA under different drain bias voltages, V_{DS}. Fig. 22(a) exhibits the measured output power, efficiency, and PAE when V_{DS} varies from 18 to 28 V. Within this range of V_{DS}, a P_{out} variation from 34 to 38 dBm was measured with a constant efficiency and PAE of ≈73% and ≈70%, respectively. The measured IM3 versus V_{DS} is plotted in Fig. 22(b), indicating an average IM3 below 40 dBc throughout the measured V_{DS} range.

B. GSM-Modulated Evaluation

To evaluate the PA's performance in actual communication systems, it is tested using a dual-carrier GSM signal modulated using Gaussian minimum-shift keying (GMSK) with a modulation symbol rate of 3 Ms/s, which are generated by the two Agilent E4433B signal generators in Fig. 15. The carriers' frequency separation is 10 MHz in this case, and each carrier has a constant envelope. The bias condition in this case is identical to

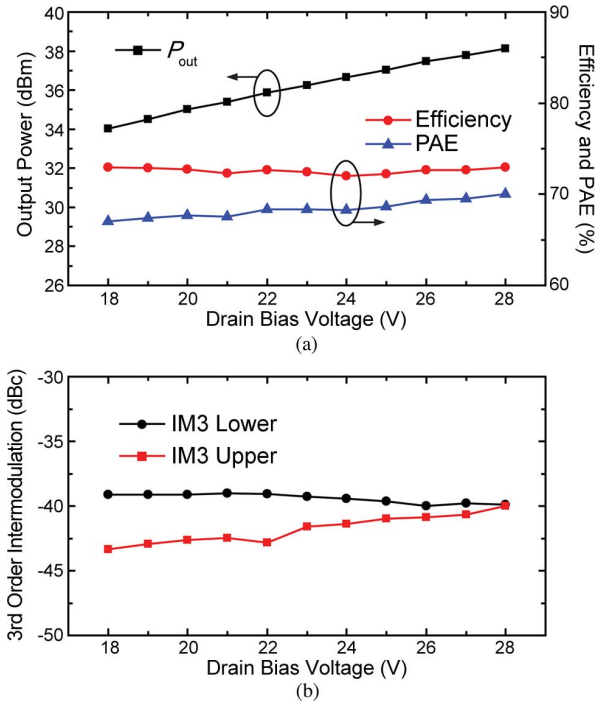

Fig. 22. Measured performance of the dual-carrier PA with different drain bias voltage. (a) PA performance. (b) Lower and upper IM3s.

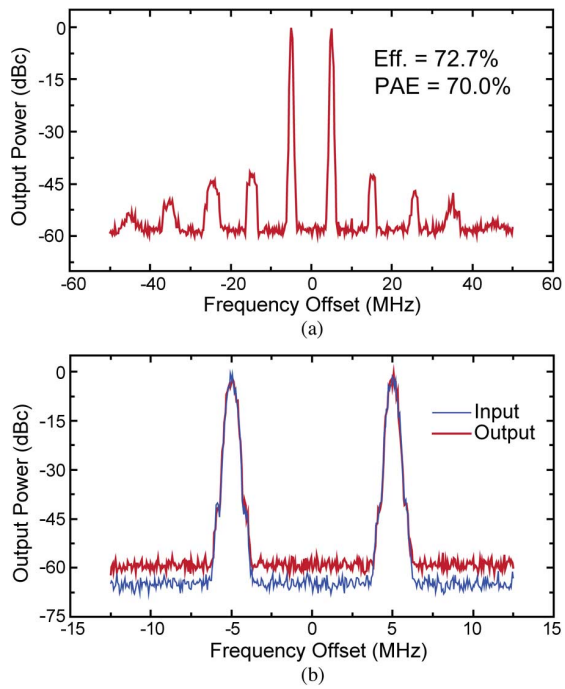

Fig. 23. Measured output spectrum with dual-carrier GSM input signal. (a) View in a wide frequency span. (b) Close-up view of two fundamental carriers.

that applied in the continuous wave (CW) testing in the above section. Fig. 23(a) shows the measured output spectrum of the PA at the saturated output power level of 38 dBm for each carrier. The measured IM3 is around −41.5 dBc with efficiency and PAE of around 73% and 70.5%, respectively. These modulated measurement results agree well with the CW results presented in Section IV-A. Fig. 23(b) shows a close-up view of the output spectrum, displaying the two fundamental frequency

TABLE IV
COMPARISON OF TWO-TONE/CARRIER PERFORMANCE WITH OTHER REPORTED MULTI-CARRIER PAS

Refs.	PA Mode	f_0(GHz)/ Δf(MHz)	P(W)	PAE(%)	IM3 (dBc)
[5]	Doherty	2.14/10	20	49	−25
[6]	Class AB +DPD	3.5/24	2	N/A	−45
[7]*	Doherty +DPD	1.8/0.6	250	42%	−55
[35]	3-Way Doherty	1.74/0.05	14	≈ 55%	−49
[36]	Doherty	2.14/10	100	< 60%†	−29
This Work	Combiner -Based	2.0/5	16	61%	−40
		2.0/10	16	70%	−41

∗ With stimulus of four-carrier GSM signal.
† Maximal CW efficiency.

components. The input signal is also plotted for comparison. It can be seen that the output carrier signals are almost distortion free compared to the input ones, indicating a good phase linearity of the designed PA.

The measured results compare favorable to other recently reported multi-carrier PAs, as summarized in Table IV. In particular, our technique exhibits the highest efficiency when amplifying a dual-carrier signal, while requiring no additional linearization for achieving a low IM3 of −40 dBc.

V. CONCLUSION

This paper has reported on an innovative PA architecture for efficiently and linearly amplifying dual-carrier signals. This dual-carrier PA consists two standalone high-efficiency PAs, which are connected to an RF carrier combiner. This combiner is implemented using a special diplexer, which enables low-loss combining (<1 dB) of two carriers with ultra-narrow frequency spacings, i.e., down to 5 MHz (0.25% fractional bandwidth at 2-GHz center frequency). Unlike conventional diplexers implemented with BPFs, this diplexer is, for the first time, realized using BSFs, which is proven to be the optimal solution for dual-carrier combining. Experimental results show that the integrated PA exhibits excellent linearity and efficiency when amplifying dual-carrier GSM signals. The measured IM3s are <40 dBc with 60.8%–70.2% PAE for 5–10-MHz carrier spacing. This technology can further extended to multi-band systems, in which the two bands can be effectively combined even though they are spectrally very close to each other.

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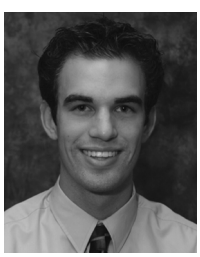

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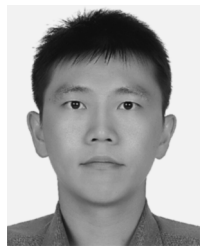

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Prof. Peroulis and his team were the recipient of Third Place in the 2011 Student PA Design Competition, IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium (IMS). In addition, a student design team for which he was the assistant team leader at Purdue University was the recipient of the First Place Awards in Phases I and II of the 2007–2008 SRC/SIA IC Design Challenge by demonstrating high-efficiency chip-to-chip wireless links with U-band transceivers. Further advances led to bondwire Yagi antenna arrays with efficiencies exceeding $>$80%.