

Michel Mardiguian  
*Contributions by*  
Donald L. Sweeney  
Roger Swanberg

# Controlling Radiated Emissions by Design

*Third Edition*



Springer

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With contributions from Donald L. Sweeney  
and Roger Swanberg



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# Foreword to the First Edition

Something over a year ago, I was fortunate enough to preview another VNR book, *Controlling Conducted Emissions by Design*, by John Fluke. My assessment at the time was that Mr. Fluke had written a very good and useful volume, its only flaw being that it focused on just half of the EMI emissions problem. This, of course, was also its strength; although radiated and conducted emissions do not exist in separate worlds, it can be useful, at least as a point of departure, to look at them as distinct phenomena. Expanding the scope of the conducted emissions book therefore would have served mostly to dilute its purpose and compromise its clarity.

After some informal discussions with the publisher on that subject, it was decided to correct the sin of omission by recruiting an author for a companion volume, to be titled *Controlling Radiated Emissions by Design*. I am gratified to have played a minor role in making that happen.

Many EMC engineers with whom I have worked over the years are capable of writing a good radiated emissions book, but few can match Michel Mardiguian's combination of practical engineering experience and proficiency with the pen. On the engineering side, he has worked on such diverse projects as the Mirage V vertical takeoff jet fighter, computer-controlled PBX systems, and, most recently, the renowned tunnel that stretches beneath the English Channel to join England with France.

In terms of academic credentials, the author has written or coauthored at least half a dozen earlier books, including a highly durable and well-respected one on electrostatic discharge. He has taught the principles of electromagnetic compatibility throughout the USA and Europe, and IEEE symposium records contain many of his short works.

Michel's books typically have several characteristics:

1. They are aimed at practical applications but provide enough theoretical material to support the suggested design and retrofit solutions.
2. They rely heavily on visual material, allowing the reader to "see" the EMI problems and solutions.
3. They omit everything that is not essential to the subject under scrutiny.

This third quality is less common than one might expect-many authors feel an irresistible urge to stuff everything they know into one volume. But Michel avoids egocentric dissertations on marginal subjects, preferring to approach each book simply as a job that needs to be done.

With this book, the author follows his usual pattern but with perhaps a greater refinement. Mathematical material is largely confined to two chapters, allowing the book to look mostly at real-world applications. More than 175 tables and illustrations provide information in a highly accessible format. This type of book is difficult for the editors and expensive for the publisher, but the reader should benefit. Some subjects (e.g., EMC testing) are covered very briefly, but the reader is referred to other sources of pertinent information.

It would be premature and presumptuous to call this book a classic in EMC literature, but it does display some of the characteristics of enduring works. *Controlling Radiated Emissions by Design* constitutes a cohesive and clear examination of the subject and is perhaps the author's best work to date.

Gainesville, VA  
1992

Jeffrey K. Eckert

# Preface

Back in 1992, I was teaching an in-house EMC seminar at a major manufacturing facility and my students were so interested to learn more; they wanted me to extend the class. My search for more material led me to Michel Mardiguian's new book, the first edition of *Controlling Radiated Emissions by Design*, and I've included it and its second edition in my seminars ever since. There are several reasons for this.

First is that the goal of my seminar is to help students think through designing an EMC compliant product from the beginning to the end, and this is exactly what Michel's book does. It starts by explaining why we need to understand the problems of radiation and how radiation happens, along with some simple mathematics for predicting the emissions and harmonic content. Michel uses graphs to further simplify the calculations. He then discusses the strategy for designing a low radiated emission product, both in the choice of circuit technology and circuit board design and all the decisions one needs to make when beginning a design. He then shows how to minimize emissions from cables and packaging. He next develops shielding, including predicting leakage from various types of apertures with real-life examples, using the emissions already predicted from our circuits in the book. He then concludes the book by showing how to troubleshoot a product when it doesn't comply with its emission requirements, including the use of a current probe to predict the reduction in emissions.

Michel is a practitioner, one who actually uses what he writes about in his consulting practice. This gives the reader a process that he/she can use to expand themselves in the field of EMC.

Secondly, instead of ending a chapter by providing problems for the student to figure out on their own, Michel gives sample problems within the text and shows step-by-step solutions to them. Our students have found the procedures and equations developed in the book so beneficial that we have developed several computer programs which allow the design engineers to repeat the calculations quickly and repeatably as they are designing their product.

Thirdly, Michel explains EMC design concepts that are easy to understand and to follow. After developing the EMC concepts, he intersperses practical examples



allowing the students to use what they just learned. These examples are rare in textbooks.

I use Michel's book during my class to supplement my own teaching materials, and I also give each of my students a copy of the book for later reference. It is also an excellent book for individual use outside the classroom.

After teaching, I give students an opportunity to sit down with an EMC expert and discuss one-on-one their own product or concerns. While doing so, one student once said, "I would not even have understood what you are talking about had I not just taken your class. Now I see what we have been doing wrong." What more needs to be said about Michel's book, seeing how it affected this student and many others like him!

Michel Mardiguian has had a distinguished career with extensive EMC experience working in the honored positions of IBM EMC Specialist, French Delegate to the CISPR Group on Computer RFI, and Director of Training for Don White Consultants. He has written many widely read books and articles and has given many lectures on EMC topics. In 2007, he received the IEEE EMC Society's prestigious Technical Achievement Award.

Wheeling, IL  
October 2013

Donald L Sweeney

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It would be unfair and incomplete if full credit was not given to those who helped with the birth of this book, and constantly attended its writing and proofing. Of all these devoted contributors, the prominent one is certainly Donald Sweeney, who relentlessly, in December 2012, inspired me to write this third edition. Don struggled eagerly through every paragraph and chapter, for the best comprehension and consistency of what I was trying to say. His colleagues at D.L.S., Roger Swanberg, Tim Lusha, and Corey Sweeney made a definite contribution to the contents of the chapters dealing with International RFI regulations and measurement procedures. Bill Stumpf and Steve Grimes did the edit review of the standards material, while Mark Rozema, Jack Prawica, and Jereme Irwin reviewed the military and RTCA part as well as Paul Vicory reviewing the automotive sections. Last but not least, I am indebted to the ladies at D.L.S.: Jessica Stephens, who did the artwork, tables, website, extensive editing, and overall support; Maxine Martin who carefully checked and rewrote some material, including those parts where Don and myself were fighting over some language controversy; Marilyn Sweeney who edited Chap. 1; and Carol Pittl who did the editing and scanning of several parts.

Michel Mardiguan



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# Abbreviations

ACMOS (or ACT)	Advanced CMOS technology
ALS	Advanced low-power Schottky logic
BGA	Ball grid array
BW	Bandwidth
CISPR	Comité International Special des Perturbations Radioélectriques
FCC	Federal Communications Commission (USA)
HF	High frequency. Although officially used for 3-30 MHz, it often designates casually the MHz frequency domain.
LCC	Leadless chip carrier
LISN	Line impedance stabilization network (synonymous: AN, artificial network)
LS (or LSTTL)	Low-power Schottky logic
QP	Quasi-peak
SE	Shielding effectiveness
SMT	Surface-mount technology
UHF	Ultra High Frequency (300-3,000 MHz)
VHF	Very high frequency (30-300 MHz)



# Symbols

- $B$  Magnetic induction, or more exactly flux density (Tesla).  
In air,  $B = \mu_0 \times H$  (A/m)
- $\beta$  Phase constant =  $2\pi/\lambda$
- $\delta$  Skin depth
- $\epsilon$  Electric permittivity constant (for air or free space =  $8.85 \times 10^{-12}$  F/m)
- $\lambda$  Wavelength =  $300/F$ (MHz)
- $\mu$  Magnetic permeability (for free space air or nonmagnetic materials  
 $\mu_0 = 4\pi \times 10^{-7}$  Henry/m)
- $\phi$  Magnetic flux. In Weber,  $\phi = B \times S =$  induction (Tesla)  $\times$  area ( $\text{m}^2$ )
- $\omega$  Angular frequency in radians/s =  $2\pi \times F$

# Chapter 1

## Generalities on Radiated Interference

### 1.1 THE PROBLEM OF RADIATED EMI

During the first part of the twentieth century, electromagnetic interference (EMI) was primarily a concern for telecommunications, both wire and radio. In these specific engineering communities, highly qualified engineers developed quite sophisticated analytical approaches to predict interference levels, taking into consideration the sources' parameters, the propagation media, and the sensitivity of the pertinent telephone or radio receivers. The typical sources of EMI until the 1960s were natural atmospheric noise, motor commutators, fluorescent lights, automobile ignition systems, and 50/60 Hz overhead lines (unintentional sources), plus jamming by other authorized (and sometimes unauthorized) radio transmitters.

The results of such interference ranged from a mere annoyance, such as poor telephone and radio audibility and disrupted TV reception, to a serious danger if the interfered transmission was critical, as in the case of an emergency service, an aircraft navigation system, etc.

But let us say that with proper handling of the frequency allocations and some rather simple constraints applied at national and international levels, the problem was acceptably under control. The "policing of the air waves" was a manageable task.

In the latter half of the twentieth century, an incredible proliferation of new RF sources has developed, including all computing and digitally operated devices (today it is very difficult to find a simple electric home appliance that does not incorporate at least an 8-bit microprocessor), medical electronics, power switchers, machine tools, remote control systems, local area networks (LANs), etc. Most of these devices produce streams of discrete frequencies that can be a stable, continuous threat for radio communication.

At the same time, the legitimate users of the radio spectrum have grown in number and types of service. From a limited, identified number of radio, TV, navigation, and safety services before 1950, the number of RF spectrum users is still increasing, comprising satellite data transmission, telemetry and radio telescopes, CB and cellular telephones, vehicle positioning systems (GPS), RFID, etc.

At the dawn of the twenty-first century, as the number and variety of potential offenders increase, so do the number and variety of potential victims, with all these growths being approximately exponential. Accordingly, the risk of interference increases astronomically, and it is little wonder that specifications and regulations have become more and more precise and stringent in an attempt to hold the problem to a manageable scale.

Equally serious is the problem of a system interfering with itself. This occurs due to lack of understanding or negligence regarding the EMI problem created by multiple sources and victims packed in close proximity.

Therefore, the subject of controlling interference, and more specifically radiated interference (the focus of this book), becomes both a matter of satisfactory performance of an equipment and its compliance with the noninterfering requirements of the military or civilian world. EMI control must be incorporated in the design stage of a product rather than postponed until the day of the prequalification or final acceptance testing. The latter invariably results in late and expensive fixes and retrofits.

This book will provide the necessary background and step-by-step procedures to design a product that neither radiates undesired signals in excess of the applicable specifications nor interferes with itself or other equipments nearby. This desirable condition is known as electromagnetic compatibility (EMC).

## 1.2 BASIC UNDERSTANDING OF RADIATED EMI

Three players are needed for the interference act:

1. A source, or emitter
2. A victim, or receiver
3. A coupling path between the two

The coupling medium can be conduction or radiation. This dichotomy is, of course, overly simplistic: no conduction exists without some radiation, and vice versa. However, it is true that certain couplings occur predominantly by conduction (through power mains, ground wires, etc.), while others occur mostly by space propagation. We will concentrate, in this book, on radiation coupling.

Depending on their internal impedance, circuits can create, in their proximity, fields that are principally electric (given in volts per meter) or magnetic (given in amperes per meter). At a greater distance from the source (farther than  $\lambda/2\pi$ ), a field is termed electromagnetic, no matter the source impedance, low or high.

In terms of radio-frequency interference, a field of 1 V/m is a rather strong field, knowing that the field sensitivity of typical radio or TV receivers could be as low as 10  $\mu\text{V/m}$ . Therefore, it is foreseeable that circuits operating at high frequency, even with low-level signals, can create interference at substantial distances.

A simple calculation can give an instant feel of the problem. Let us assume a small device where the electronic core consists mainly in a CPU and memory.

The computer circuit includes 60 IC chips, each one consuming about 400 mW of average power. Assume also that only one fourth of the circuits that reside on these chips are toggling synchronously at the internal clock frequency of 100 MHz, for instance. Then the total power switched at a given instant during a transition is

$$(1/4) \times (60 \times 0.400) = 6 \text{ W}$$

Now assume that a minuscule fraction of this power is not dissipated by Joule effect in the chips, the wiring, and various resistances or displays, but is radiated instead. For instance (and this is quite optimistic), assume that on the 100 MHz main clock frequency, only  $10^{-6}$  of the total switched power is radiated, that is,  $6 \mu\text{W}$ . A simple formula gives the field strength from any given radiator, in far-field conditions:

$$E(\text{V/m}) = (30P_r)^{0.5}/D \quad (1.1)$$

where  $D$  = distance from source, in meters  $P_r$  = radiated power (including antenna gain), in watts

At 3 m distance, our  $6 \mu\text{W}$  from the PC board will create a field:

$$E(\text{V/m}) = (30 \times 6.10^{-6})^{0.5}/3 = 4.5 \text{ mV/m}$$

Expressed in standard units of EMI specifications for field strength, this is

$$E \text{ dB}\mu\text{V/m} = 20 \log(4.5 \times 10^3 \mu\text{V/m}) = 73 \text{ dB}\mu\text{V/m}$$

The minimum field strength required by TV and FM listeners for decent reception quality in remote areas is in the range of 50-60 dB $\mu\text{V/m}$ . Therefore in the case of frequency coincidence (co-channel EMI), the CPU clock may seriously affect radio/TV reception in its vicinity since, at a 3 m distance (assuming the computer has a plastic case with no shielding), the EMI field will be 4-13 times stronger than the sound or picture carrier.

In this case, annoying interference is likely to exist 30 m away, or even farther if there is some field enhancement caused by metallic structures, poles, etc. around the short radio path between the EMI source and the victim receiver antenna.

Of course, the basis of any sound design is:

1. To understand by which mechanisms a circuit devised to store and process data, or convert power, ends up being a radio transmitter
2. To have a numerical estimate of those mechanisms, in order to reduce or counteract them
3. To test the results as early as possible on a prototype model

The two first items are really the design issues. Since no radiation can exist without voltages or currents, a large part of the quantitative approach will be spent on circuit design, waveforms analysis, and layout recommendations.

### 1.3 EMI TERMINOLOGY AND UNITS

Due to the wide dynamic range we face in the EMI/RFI/EMC disciplines, logarithmic scaling is used extensively. Therefore most ratios (dimensionless) and magnitudes are expressed in decibels (dB).

Expressing the ratio of two powers becomes

$$\text{dB} = 10 \log \frac{P_2}{P_1} \quad (1.2)$$

More often, data is measured in units of amplitude (e.g., voltage, current, field strength) instead of power. Substituting  $P = V^2/R$  into (1.2) yields

$$\begin{aligned} \text{dB} &= 10 \log \frac{(V_2)^2/R_2}{(V_1)^2/R_1} \\ &= 20 \log(V_2/V_1) + 10 \log(R_1/R_2) \end{aligned} \quad (1.2a)$$

If  $R_1 = R_2$ , this becomes

$$\text{dB} = 20 \log(V_2/V_1) = 20 \log(I_2/I_1) \quad (1.3)$$

Equations (1.2) and (1.3) are computed in Table 1.1 for all usual ratios. Corresponding negative dB equivalents are found by reciprocating any of the ratios.

The expression in dB for voltage or current is obtained by substituting 1 V or 1 A into Equ. (1.3):

$$\begin{aligned} V(\text{dBV}) &= 20 \log V, \text{ or} \\ I(\text{dBA}) &= 20 \log I \end{aligned}$$

Retrieving voltage, current, or field strength from its dB value is obtained by taking the antilog ( $\log^{-1}$ ):

$$V_{\text{volt}} = \log^{-1}(\text{dBV}/20) = 10^{\frac{\text{dBV}}{20}} \quad (1.3a)$$

If voltage has to be derived from a power in dBm (dB above 1 mW), this is obtained by

$$V(\text{dB}\mu\text{volts}) = 107 + P(\text{dBm}), \text{ for } Z = 50 \Omega \quad (1.4)$$



For narrowband (NB) EMI, where only one single spectral line (i.e., a sine wave) is present in receiver's (or victim's) bandwidth, the EMI signal can be expressed in

1. Voltage:  $V$ , dB above 1 V (dBV), or dB above 1  $\mu V$  (dB $\mu V$ )
2. Current:  $A$ , dB above 1 A (dBA), or dB above 1  $\mu A$  (dB $\mu A$ )
3. Power:  $W$ , mW, or dB above 1 mW (dBm)
4.  $E$  field:  $V/m$ ,  $\mu V/m$ , or dB $\mu V/m$
5.  $H$  field or magnetic induction:  $A/m$ ,  $\mu A/m$  or dB $\mu A/m$ , Tesla or Gauss (1 G = 80 A/m, 1 T =  $10^4$  G)
6. Radiated power density:  $W/m^2$ ,  $mW/cm^2$ , or dBm/cm<sup>2</sup>

For broadband (BB) EMI, where many spectral lines combine in the receiver's bandwidth, the received EMI is normalized to a unity bandwidth:

1. Voltages:  $\mu V/kHz$ ,  $\mu V/MHz$ , or dB $\mu V/MHz$
2. Currents:  $\mu A/kHz$ ,  $\mu A/MHz$ , or dB $\mu A/MHz$
3.  $E$  fields:  $\mu V/m/kHz$ ,  $\mu V/m/MHz$ , or dB $\mu V/m/MHz$
4.  $H$  fields:  $\mu A/m/kHz$ ,  $\mu A/m/MHz$ , or dB $\mu A/m/MHz$

There are several ways to recognize NB or BB interference conditions. A simple one is this:

Given the passband or 3 dB bandwidth (BW) of the receiver (or victim's input amplifier) and  $F_o$  the EMI source fundamental frequency, the interference will be

$$\text{BB if } BW > F_o$$

$$\text{NB if } BW < F_o$$

**Table 1.1** Ratios to dB conversion

Voltage current or field amplitude ratio	Power ratio	Decibels
$\times 1.12$	$\times 1.25$	+1
$\times 1.25$	$\times 1.6$	+2
$\times 1.4$	$\times 2$	+3
$\times 2$	$\times 4$	+6
$\times 3.16$	$\times 10$	+10
$\times 5$	$\times 25$	+14
$\times 10$	$\times 100$	+20
$\times 1,000$	$\times 10^6$	+60

Examples: 1  $\mu V = 0$  dB $\mu V$

1  $mV/m = 60$  dB $\mu V/m$

50  $\Omega = 34$  dB $\Omega$

1  $mW = 0$  dBm

1  $mW$ , in 50  $\Omega = 0.22$  V = 107 dB $\mu V$

## 1.4 THE USA AND WORLDWIDE REGULATORY APPROACH AGAINST RADIATED EMI

Long ago, maximum emission levels were set by civilian commissions to protect broadcasting as well as military organizations to insure optimum reception of vital radio communications, navigation and guidance system signals, etc. Of specific nature is the TEMPEST problem, which covers the possible eavesdropping on confidential data by unauthorized receivers. (TEMPEST is a code word for a classified program but not an acronym: its letters do not “stand for” anything.) This is both a military/government concern for national security and a business/industry issue for the protection of sensitive and confidential data.

Civilian limits to radiated emissions are fairly severe, but, generally, one could remark that military specifications are significantly more stringent due to the close proximity (sometimes less than 1 m) of sources and victims within aircraft, armored vehicles, etc. Since this book is a design tool, and not an encyclopedia of specifications, we will review only briefly the basis of civilian and military standards that pertain to radiated EMI.

### 1.4.1 Worldwide Civilian Standards

Table 1.2 gives a summary of the principal emission standards and national laws for the USA and worldwide. As indicated, many national laws are based on the CISPR documents.

In general, maximum emission levels have been set by an international commission on a device-by-device basis after establishing a need to protect radio communications from interference by a particular piece of equipment. In many instances, a country such as the USA, Germany, or the Netherlands has been the instigator and major player in the development of certain category of limits. But nevertheless, to avoid a myriad of different limits between countries, an international commission called the CISPR, part of the International Electrotechnical Commission (IEC), is tasked to publish unanimously accepted limits and establish test methods for EMI emissions.

Once CISPR limits have been voted into effect by member nations of the IEC, they sooner or later become translated into national standards within the various countries. Depending on the type of government in each country, these limits may remain as industry standards, more or less voluntarily applied, or turned into compulsory laws. The latter has been the case for many years in Germany, then since 1980 in the USA, and starting 1990 in all countries of the European Economic Community, where CISPR recommendations have been promulgated as harmonized European Norms (ENs).

**Table 1.2** Major civilian RF emission standards and regulations, worldwide

	Industrial, scientific, and medical (ISM)	Internal combustion engines	Sound and TV broadcast receivers	Household appliances and similar apparatus	Lighting devices including RF	Information technology equipment (ITE)	Automotive, boats, protection of onboard receivers	Cellular telephone systems (mob and base)	Unlicensed RF transmitters (remote ctrl, WiFi, Bluetooth, UWB)
International	CISPR 11	CISPR 12	CISPR 13 (CISPR 32 should soon replace)	CISPR 14	CISPR 15	CISPR 22 (CISPR 32 should soon replace)	CISPR 25		
Australia, New Zealand	AS/NZS CISPR 11	AS/NZS CISPR 12	AS/NZS CISPR 13	AS/NZS CISPR 14	AS/NZS CISPR 15	AS/NZS CISPR 22		AS/NZS 4268	
Canada	ICES 001	ICES 002/	BETS-7		ICES 005	ICES 003	CAN/CSA-CISPR 12-10	RSS-118 RSS-129 RSS-132 RSS-139	
China	GB 4824		GB 13837	GB 4343.1	GB 17743	GB 9254			
European Union	EN 55011	EN 55012	EN 55013 (see CISPR 32)	EN 55014	EN 55015	EN 55022 (see CISPR 32)	Auto Dir. 2004/104/EC	ETSI Standards	ETSI Standards
Japan	JIS C 1806-1					VCCI			Japan Radio Regulatory Commission Regulations
Korea	KN 11		KN 13	KN 14-1	KN 15	KN 22			
Taiwan	CNS 13803		CNS 13439	CNS 13783-1	CNS 14115	CNS 13438			
USA	FCC Part 18		FCC Part 15	(Some) FCC Part 15	FCC Part 18	FCC Part 15		FCC Part 22, 24	

Industrialized countries, including the ones not listed, generally follow CISPR recommendations for interference suppression. This chart, along with other information, will be updated and available at <http://dlsemc.com/crebd>

European Community has adopted a rather strict attitude regarding EMC: the former 89/336 Directive stated that no equipment, regardless if it is manufactured in Europe or imported, can be commercialized if it does not comply with low emission *and* immunity requirements. There was a 6-year grace period for the industry to adjust and absorb the slack of existing products in stock. After January 1, 1996, compliance has become mandatory, the conformity being attested by the CE Mark affixed on the equipment. The current update of the Directive is 2001/108/EMC.

Failure to fulfill applicable test and certification requirements (even if no interference is actually created) is illegal, and the manufacturer (not the user) can be prosecuted and penalized.

Small regulatory variations occur in some countries. However, if a product is designed to meet CISPR or EN emission levels, it is likely that it will comply with interference laws for its specific class in most industrialized countries. Each country has a specific policy to ensure that manufacturers or vendors deliver products that meet emission limits. Some require test and certification by a national laboratory (e.g., China) and some accept manufacturers' self-certification.

In general, the standards were set to cover two categories of potential interference signatures:

1. RF signals emitted by intentional high-frequency sources (mainly covered by CISPR Publications 11, 13, 22, and 25). These include HF industrial equipment, ovens, welders, oscillators, digital computing devices, and, in general, any equipment which intentionally generates high-frequency signals above 9 kHz, but is not a licensed radio transmitter. In general, the frequency spectrum of these equipments contains a set of discrete, stable spectral lines (narrowband spectrum).
2. RF signals emitted by non-intentional high-frequency sources (mainly covered by CISPR Publications 12, 14 and 15). These include motors, fluorescent lights, dimmers, car ignitions, and so forth where production of RF energy is fortuitous. The frequency spectrum of these equipments is generally a dense series of random or correlated frequencies (broadband spectrum).

Notice that many modern equipments/systems contain a mix of both types of sources. The standards generally take into account this possibility, either by imposing two sets of limits (NB and BB) or by some specific features of the measuring receiver that automatically adjust the RF detector's response.

A third type of interference sources is found in intentional radio transmitters and receivers both licensed, e.g., FCC 22, 25, and many others as well as non-licensed, e.g., some parts of FCC Part 15. These generally have discrete, stable spectral lines, NB. One exception would be that a superregenerative receiver covered in FCC Part 15 is BB.

Many specific international EMC standards keep being issued as technology evolves. They are changing quite fast and listing them all in a book like this one would be difficult and often useless since they are perishable data. A Web site which will continue to keep updated on the ever-changing list of standards can be found at <http://www.dlsemc.com/crebd> (controlling radiated emissions by design). However, besides the well-known computer category, a few of them are listed next, since they are sufficiently important and cover a large number of devices.

#### *1.4.1.1 CISPR 25 RFI Protection of Receivers on Board Vehicles*

A vehicle (car, truck, bus) is an EMI nightmare in itself. A maze of noisy components like pulse-driven motors, Electronic Control Modules with fast clocks, etc. are in close proximity and share the same cable harness with sensitive radio receivers: car radio, cellular telephones, CB or emergency receivers, navigation/positioning systems (GPS), internal telemetry, and low-power RF devices (Bluetooth, etc.). These receiver's antennas are typically within a meter or less of potential disturbers. This calls for stringent emission control, and, indeed, the CISPR 25 radiated limits are among the most severe in existence, sometimes tougher than MIL-STD levels (see Chap. 12).

It is worthwhile noting that in the USA, computers mounted exclusively in a motor vehicle are not regulated by the FCC. The reason is such emissions are deemed self-regulating: people would not buy a device if it interferes with the radio receiver in the motor vehicle! Vehicle manufacturers often have their own requirement for emission as well. Automotive presents an area of EMC where meeting the standard may not be enough. Often two devices are literally on top of each other, and the fields from a device meeting the 1 m test might not be enough in this close proximity. In these cases, special care and work will be done to make the device meet the application. Although the cost-sensitive nature of automotive electronics does not allow one to simply meet the standard by more dBs than is necessary, this could require more than 20 dB additional margin in the case of a device only a few cm from the offending device.

#### *1.4.1.2 IEC 61800-3: Variable Power Drive Systems*

The technical progress in power semiconductors has generated a whole family of secondary power sources where the output is made adjustable by electronic control: light dimmers, adjustable speed drives, etc. In the latter, an electric motor from fractional HP to thousands kW can have its speed adjusted continuously without any mechanical or electromechanical device. Operating in fast switched mode as voltage or frequency converters, they are generally powerful sources of both NB and BB interference, since the wiring to the motor can run over significant lengths in a commercial building, a public site, etc. IEC 61800-3 establishes conducted and radiated emissions limits, similar to those of CISPR 22 for computers.

#### *1.4.1.3 ETSI/FCC Standards*

Telecommunications is a complex field which is more and more intermixed with digital techniques. The tremendous growth of mobile telephony and wireless data communication has exacerbated potential EMI situations. A specific European

organization, the European Telecom. Standard Institute, has been founded in 1988 to develop ad hoc specifications among which a certain number, labeled ETSxxxx, are covering EMC aspects. Once they become a European Norm, the prefix is then changed to ETSI EN. These standards cover the EMC aspects of telecommunication equipment in the EU. Every time a system incorporates a telecommunication device, whether it is connected to a wired or radio link, the system has to comply with the relevant ETSI norms or FCC requirements.

## 1.4.2 FCC Standards for Emissions

In the USA, Congress has delegated authority to the Federal Communications Commission (FCC) to regulate civilian radio and wire communication. This includes the issuance and enforcement of EMI regulations. General classifications are as follows:

### 1. *FCC Part 15: Radio-Frequency Devices*

This is the most widely applied FCC EMI standard. It covers digital computing devices plus garage door openers, radio-controlled toys, cordless telephones, and other intentional low-power transmitters. For computers, the FCC Part 15 Subpart “B” considers two classes of potential offenders:

- A. Class A covers digital equipment that is marketed to be used only in industrial and commercial areas. For these, self-certification by manufacturer is permitted.
- B. Class B covers digital equipment that can be used in a residential environment. Because of the higher probability of proximity with a radio or TV, Class B limits are approximately 10 dB more severe than Class A, and a formal procedure is required. The manufacturer must have its equipment tested by an accredited laboratory, and then he can issue a Declaration of Conformity. The test report must be available upon FCC request. For some devices, such as intentional radiators (transmitters), the test report must be submitted directly to a TCB (Telecommunication Certification Body) for a Grant of Certification.

### 2. *FCC Part 18: Industrial Scientific and Medical Equipment (ISM)*

Like CISPR11, this part regulates spurious emissions from equipment and appliances that purposely generate RF energy for something other than radio or telecommunications. These include heating, ionization, ultrasonic process, medical treatment and diagnosis equipment, etc. Such devices have precise ISM frequency allocations where no emission limit exists, but emission restrictions apply across the rest of the spectrum.

### 1.4.3 The Mutual Recognition Agreement (MRA)

In order to eliminate trade barriers and to comply with the World Trade Organization (WTO) rules, FCC/NIST and the European CENELEC have signed in 1997 an agreement by which the EMC qualification tests conducted in the USA by an FCC-approved lab will be accepted by European countries, and vice versa. Therefore, US manufacturers and EMC laboratories can test and approve in USA an equipment bound for the European market.

The US-EU MRA allowed for the *EU labs* to be recognized by the FCC (through a formal designation process from the European Commission to the FCC) and also allowed for the EU to qualify Telecommunications Competent Bodies (also through a formal designation process from the Commission to the FCC).

For the *US labs*, the MRA's benefit was that qualified organizations in the USA could apply to become a Notified Body in the EU (this is done through a formal designation process between NIST and the Commission).

### 1.4.4 Other US Government Standards (Nonmilitary)

Many industries and professional bodies have issued emission standards in areas that are not covered by FCC regulations or where they believe that more stringent limits are needed. A few examples are described below.

#### 1.4.4.1 *FDA Standard for Medical Devices*

The Food and Drug Administration now requires compliance with the international requirements of IEC 60601-1-2, whose emission limits are those of CISPR11 (industrial, scientific, and medical devices) before submittal. This standard covers more than emissions since immunity testing (to demonstrate the robustness of the design to RF energy) is also required. This requirement has replaced the former compliance with MDS-20 1-000.

#### 1.4.4.2 *NACSIM 5100*

Better known as TEMPEST, this is a classified standard developed to ensure that confidential information cannot be captured by unauthorized receivers during electronic processing, handling, or transmitting by government agencies. Special measurement techniques and limits are required to guarantee such a low level of emission that the clear, unciphered data is undetectable. These techniques and limits are, of course, classified.

#### 1.4.4.3 SAE Standards

The Society of Automotive Engineers, among many engineering activities, has issued several EMI emission standards such as:

SAE J 551 radiated EMI from vehicles and associated devices

SAE J 181 levels and measurement methods

These are typically tailored by each vehicle manufacturer, often resulting in more stringent limits, especially regarding electronic equipments to be incorporated on board.

#### 1.4.4.4 RTCA Standards

The Radio Technical Commission for Aeronautics has issued a broad set of stringent standards for the critical domain of civilian aircrafts. Environmental effects are addressed in DO-160 (present 2013 revision is G). EMI emissions are covered in Section 21. They are parallel to, although generally less severe than, MIL-STD-461/RE101, RE102, RE103. Looking back at its evolution, since Revs. C and D, this standard has followed the same philosophy as MIL-STD-461, replacing the NB/BB dichotomy by a single limit.

### 1.4.5 Military Emission Standards

The military approach to EMI control is a remarkable example of a well-structured, rather unforgiving, test program. The most prevalent EMC military standard is the MIL-STD-461, whose current 2013 Rev. is F. The general organization tree is shown in Fig. 1.1.

Up to its Rev. D (1999), a parent document MIL-STD-462 was describing the associated test setup methods. Starting with MIL-STD-461E, the #462 STD has been suppressed, and its contents have been incorporated in the main document.

Being a tri-service document (Army, Navy, and Air Force), it is extremely versatile and can be tailored to any equipment, subassembly, or part of a system. It is not applicable to an entire complex system, such as a fire-control system, a radar warning system, a vehicle, etc. Those need to be qualified on their site or carrier, per MIL-STD-464.

MIL-STD-461, thanks to its broad scope, has been recognized by many defense organizations outside the USA, as well as some nonmilitary agencies. These entities have more or less transposed (admittedly or not) the MIL-STD-461 organization and values. This is the case for UK (Def-Stan), Germany (VGxxx), France (GAM EG 13), and many other countries. The NATO EMC Standards (STANAG) also apply the MIL-STD-461 approach.



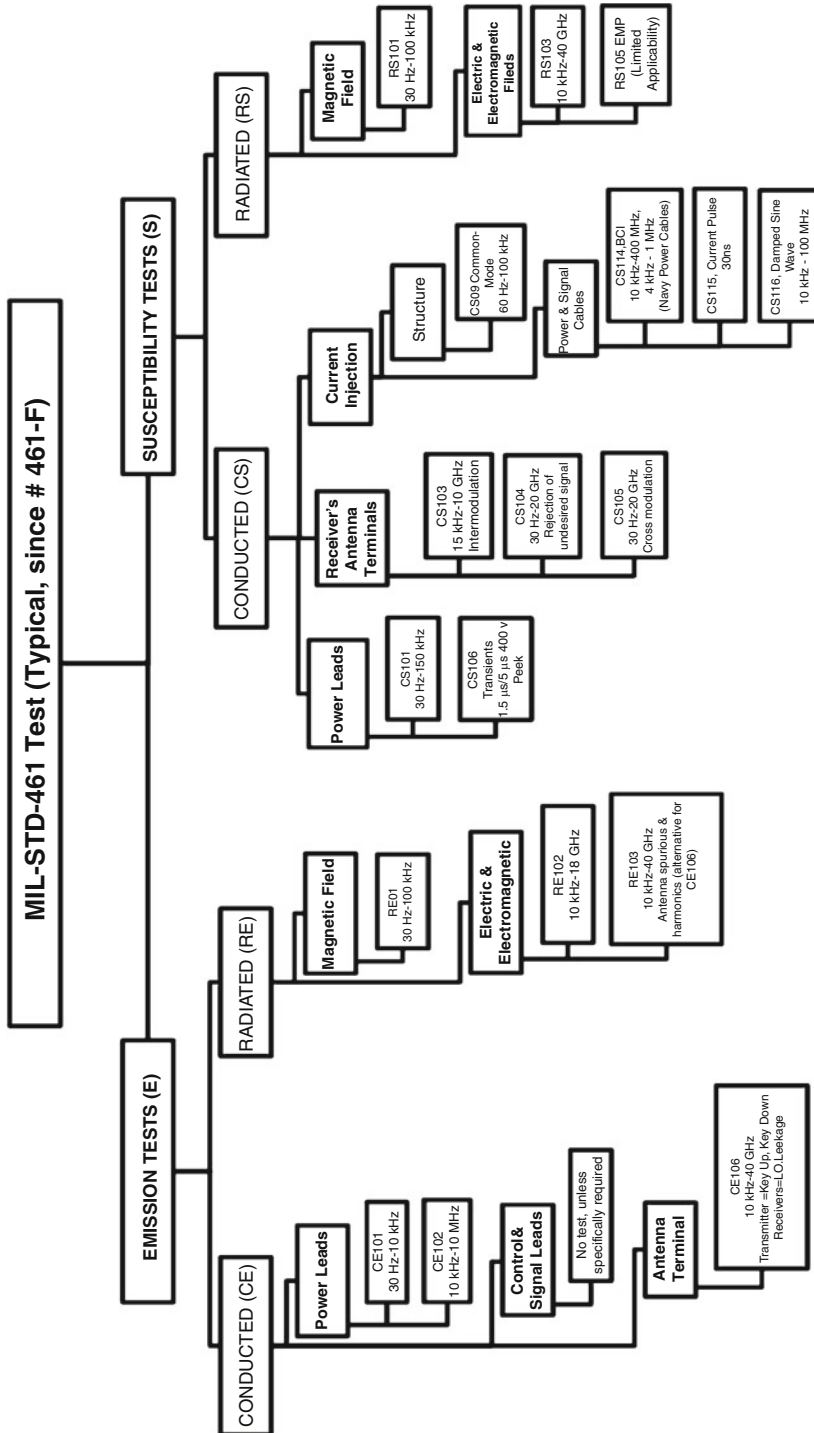


Fig. 1.1 MIL-STD-461 organization tree

Mil-STD-461 is to be regarded as a nearly complete inventory of all the EMC tests that can be performed. This does not mean that every military deliverable item has to pass all 17 tests, 8 of them being emissions! For each program, a test plan has to be written as part of the EMI control plan. Under supervision of the procuring agency, the test plan outlines which of the MIL-STD-461 tests will be performed. Depending on the nature of the equipment and its installation field, some tests are not applicable. Of the 17 tests, it is not uncommon to see only 10 or 12 being required. Therefore, it is important for the potential user of an available equipment which is claimed “compliant with MIL-STD-461” to determine exactly what tests have been actually carried out.

The emission aspect is covered by the left-hand branch of the Fig. 1.1 tree, which subdivides in two smaller branches:

1. The series of conducted emission tests (CE)
2. The series of radiated emission tests (RE)

In 1993, MIL-STD-461 incurred a major revision, becoming 461D. The changes were significant: for the emission tests, the NB vs. BB dichotomy has been suppressed ever since, replaced by a single limit in a prescribed bandwidth. The conducted tests are performed only up to 10 MHz, instead of 50 MHz as before, and the conducted limit (CE102) is given as a voltage measured at a 50  $\mu$ H LISN port, instead of a current as in the former A, B, and C versions. Although in many respects the Rev. D was an improvement in coherence, clarity, and test practices, some of the changes were resented as a stepback in the degree of EMC protection, especially for analog radio receivers. As such, certain procurement specifications and test plans still quote the 461C (dated 1986).

## 1.5 INTRASYSTEM VS. INTERSYSTEM EMI

A dichotomy appears when we attempt to define the borderline between a self-jamming system (i.e., equipment that disturbs its own operation in a sterile electromagnetic environment) and one that is a nuisance to the external environment (see Fig. 1.2). These two undesirable situations are referred to as intrasystem and intersystem EMI, respectively.

As far as radiated emissions are concerned, intrasystem compatibility requires two conditions:

1. None of the inside sources may radiate more than the field susceptibility of its neighbor components within the spectrum boundaries.
2. Condition #1 being met, the combined emissions of all sources together must remain below the field susceptibility threshold of any component within the system.

These are functional conditions. If they are not met, the system simply does not work properly, even in a noncritical environment. Therefore, satisfying intrasystem EMC is the prime, “selfish” goal of any designer who is concerned only with moving an operational product through the assembly line.

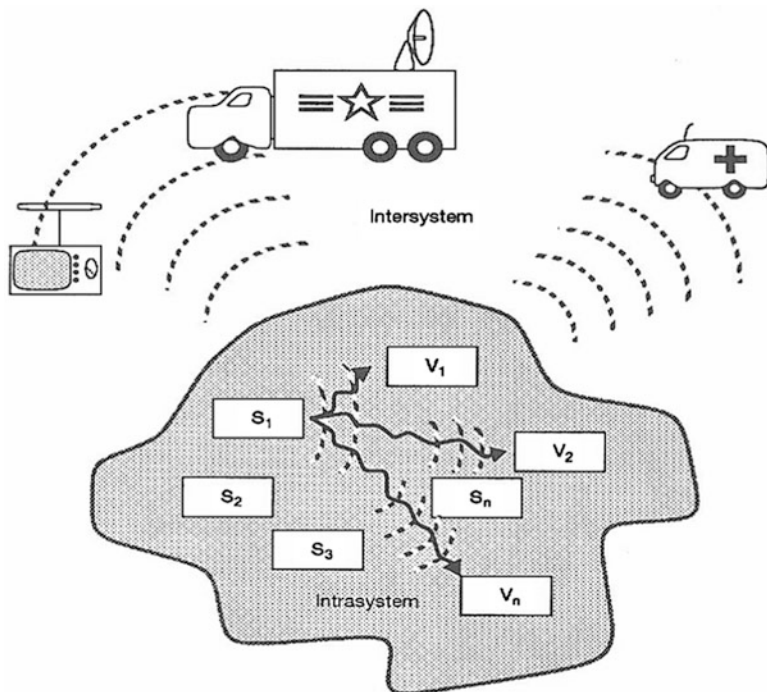


Fig. 1.2 Intrasytem vs. intersystem EMI

Quite differently, intersystem EMC requires that when the whole system operates, no other system in its vicinity may be disturbed, especially by spurious radiated signals. Intrasytem EMC concerns only the performance of a single system, while intersystem EMC deals with electromagnetic pollution of the environment.

With intrasytem EMC, the culprit and victims are known and can be controlled. It is not absolutely required (although a safe practice) that interference be suppressed at the source. After all, if all victims were very well hardened, they could tolerate strong noise sources next door.

At the contrary, with intersystem EMC the victims are unknown and out of our control. They are generally replaced by the emission limits which substitute for real victims. Thus, radiated emissions at source level should be suppressed for both intra- and intersystem EMC.

As a very broad rule, modeling and experience show that very often, if all sources in a system meet the radiated emission limits dictated by RF protection for the corresponding environment, these limits are stringent enough to guarantee that self-jamming will be avoided within the system as well.

But there are exceptions whereas a subassembly that is compliant for external compatibility may still be a nuisance for another part of the system which is extremely close (much closer than 1 m for instance).

## Chapter 2

# Electric and Magnetic Fields from Simple Circuit Shapes

If one wants to avoid empirical recipes and the “wait and see if it passes” strategy, the calculation of radiated fields from electric circuits and their associated transmission cables is of paramount importance to proper EMI control. Unfortunately, precisely calculating the fields radiated by a modern electronic equipment is a hopeless challenge. In contrast to a CW transmitter, where the radiation source characteristics (e.g., transmitter output, antenna gain and pattern, spurious harmonics, feeder and coupler losses, etc.) are well identified, a digital electronic assembly, with its millions of input/output circuits, printed traces, flat cables, and so forth, is impossible to mathematically model with accuracy, at least within a reasonable computing time by today’s state of the art. The exact calculation of the  $E$  and  $H$  fields radiated by a simple parallel pair excited by a pulse train is already a complex mathematical process.

However, if we accept some drastic simplification, it is possible to establish an order of magnitude of the field by using fairly simple formulas. Such simplification includes:

1. Retaining only the value of the field in the optimum direction
2. Having the receiving antenna aligned with the maximum polarization
3. Assuming a uniform current distribution over the wire length, which can be acceptable by using an average equivalent current instead of the maximum value
4. Ignoring dielectric and resistive losses in the wires or traces

The formulas described hereafter were derived by S. Schelkunoff [5] from more complex equations found in the many books on antenna theory. They allow us to resolve most of the practical cases, which can be reduced to one of the two basic configurations:

1. The closed loop (i.e., magnetic excitation)
2. The straight open wire (i.e., electric excitation)

## 2.1 FIELD RADIATED BY A LOOP

An electromagnetic field can be created by a circular loop carrying a current  $I$  (Fig. 2.1). Assuming that:

- $I$  is uniform along the loop.
- There is no impedance in the loop other than its own reactance.
- The loop size is  $\ll \lambda$ .
- The loop size is  $< D$ , the observation distance.
- The loop is in free space, not close to a metallic surface.

$E$  and  $H$  can be found by using the simple solutions that Schelkunoff derived from Maxwell's equations. Replacing some terms by more practical expressions:

$$H_r \text{ A/m} = \frac{IA}{\lambda} \left[ \frac{j}{D^2} + \frac{\lambda}{2\pi D^3} \right] \cos \sigma \quad (2.1)$$

$$H_\sigma \text{ A/m} = \frac{\pi IA}{\lambda^2 D} \sqrt{1 - \left( \frac{\lambda}{2\pi D} \right)^2 + \left( \frac{\lambda}{2\pi D} \right)^4} \sin \sigma \quad (2.2)$$

$$E_\phi \text{ V/m} = \frac{Z_0 \pi IA}{\lambda^2 D} \sqrt{1 + \left( \frac{\lambda}{2\pi D} \right)^2} \sin \sigma \quad (2.3)$$

where:

$I$  = loop current, in amperes

$A$  = loop area in  $\text{m}^2$

$\lambda$  = wavelength in meters =  $300/F_{(\text{MHz})}$

$D$  = distance to observation point, in meters

$Z_0$  = free space impedance =  $120\pi$  or  $377 \Omega$

Comparing this with Fig. 2.1, we see that for  $\sigma = 0$ ,  $E_\phi$  and  $H_\phi$  are null ( $\sin \sigma = 0$ ), while  $H_r$  is maximum ( $\cos \sigma = 1$ ). Except near the center of a solenoid or a transmitting loop antenna, this  $H_r$  term in the  $Z$ -axis direction is of little interest because it vanishes rapidly, by its  $1/D^2$  and  $1/D^3$  multipliers. Notice also that there is no  $E_r$  term.

To the contrary, in the equatorial plane, for  $\sigma = \pi/2$ ,  $H_r$  is null, and  $E_\phi$ ,  $H_\phi$  get their maximum value. So from now on, we will consider systematically this worst-case azimuth angle.

Looking at Equ. (2.2) and Equ. (2.3) and concentrating on boundary conditions, we see two domains, near field and far field, plus a transition region.

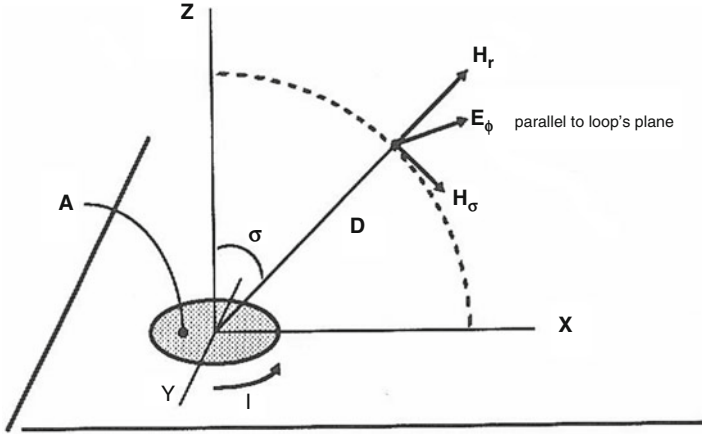


Fig. 2.1 Radiation from a small magnetic loop

**Near Field:** For  $\lambda/2\pi D > 1$ , i.e.,  $D < \lambda/2\pi$  or  $D < 48/F(\text{MHz})$

Under the square root in Equ. (2.2) and Equ. (2.3), the larger terms are the ones with the higher exponent. Thus, neglecting the other second- or third-order terms, we have:

$$H_{A/m} = \frac{IA}{4\pi D^3} \tag{2.4}$$

$$E_{V/m} = \frac{Z_0 IA}{2\lambda D^2} \tag{2.5}$$

We remark that  $H$  is independent of  $\lambda$ , i.e., independent of frequency: the formula remains valid down to DC.  $H$  falls off as  $1/D^3$ .  $E$  increases with  $F$  and falls off as  $1/D^2$ .

In this region called near-field or induction zone, fields are strongly dependent on distance. Any move toward or away from the source will cause a drastic change in the received field. Getting ten times closer, for instance, will increase the  $H$  field strength 1,000 times.

Since dividing volt/m by amp/m produces ohms, the  $E/H$  ratio, called the wave impedance for a radiating loop, is

$$Z_w(\text{near loop}) = Z_0 \frac{2\pi D}{\lambda} \tag{2.6}$$

When  $D$  is small and  $\lambda$  is large, the wave impedance is low. We may say that in the near field,  $Z_w$  relates to the impedance of the closed loop circuit which created the field, i.e., almost a short. As  $D$  or  $F$  increases,  $Z_w$  increases.

**Far Field: For  $\lambda/2\pi D < 1$ , i.e.,  $D > \lambda/2\pi$ , or  $D > 48/F(\text{MHz})$**

The expressions under the square roots in Equ. (2.2) and Equ. (2.3) are dominated by the terms with the smallest exponent. Neglecting the second- and third-order terms, only the “1” remains, so:

$$H_{A/m} = \frac{\pi I A}{\lambda^2 D} \quad (2.7)$$

$$E_{V/m} = \frac{Z_0 \pi I A}{\lambda^2 D} \quad (2.8)$$

In this region, often called the *far-field*, *radiated-field*, or *plane wave region*<sup>1</sup>, both  $E$  and  $H$  fields decrease as  $1/D$  (see Fig. 2.2). Their ratio is constant, so the wave impedance is

$$Z_w = E/H = 120\pi \text{ or } 377 \Omega$$

This term can be regarded as a real impedance since  $E$  and  $H$  vectors are in the same plane and can be multiplied to produce a radiated power density, in  $\text{W/m}^2$ .  $E$  and  $H$  increase with  $F^2$ , an important aspect that we will discuss further in our applications.

**Transition Region: For  $\lambda/2\pi D = 1$  or  $D = 48/F(\text{MHz})$**

In this region, all the real and imaginary terms in field equations are equal, so all terms in  $1/D$ ,  $1/D^2$ , and  $1/D^3$  are equal and summed with their sign. This zone is rather critical because of the following:

1. With MIL-STD-461 testing (RE102 test for instance), the test distance being 1 m, the near-far-field transition is taking place around 48 MHz, which complicates the prediction.
2. Speculations concerning the wave impedance are hazardous due to very abrupt changes caused by the combination of real and imaginary terms for  $E$  and  $H$ .

---

<sup>1</sup> However, “plane wave” does not have exactly the same meaning. Another condition is governing the near- or far-field situation that is related to the physical length of the antenna. If  $l$ , the largest dimension of the radiating element, is not small compared to distance  $D$ , another near-field condition exists due to the curvature of the wavefront. To have less than 1 dB (11%) error in the fields calculated by Equ. (2.7) and Equ. (2.8), another requirement stipulates that  $D > l^2/2\lambda$ . However, if the dimension of the radiating element is less than  $\lambda/2$ , both length and distance far-field conditions are met for  $D$  (far field)  $> \lambda/2\pi$ .

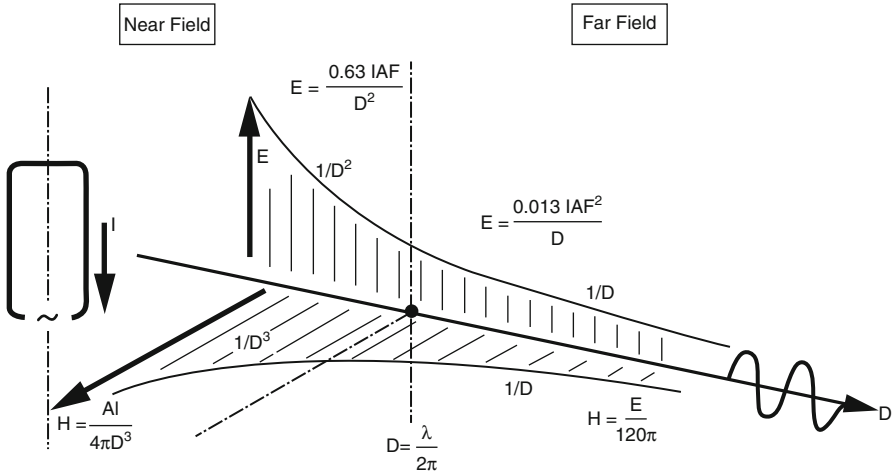


Fig. 2.2  $E$  and  $H$  fields from a perfect loop

## 2.2 FIELDS RADIATED BY A STRAIGHT WIRE

It does not take a closed loop to create an electromagnetic field. A straight wire carrying a current,  $I$ , creates an electromagnetic field (most radio communication antennas are wire antennas). The practical difficulty is that, in contrast to the closed loop, it is impossible to realize an isolated dipole with a DC current: only AC current can circulate in an open-wire self-capacitance. Fields generated from a short, straight wire are shown in Fig. 2.3.

$E$  and  $H$  can be derived from Maxwell's equations with the same assumptions as the elementary loop, i.e.:

- Current  $I$  is uniform.
- The wire length  $\ll \lambda$ .
- The wire length  $< D$ , the observation distance.
- The wire is in free space, not close from a ground plane.

Using Schelkunoff's solutions for a small electric dipole, expressed in more practical units,

$$E_r = 60I\ell \left( \frac{1}{D^2} - \frac{j\lambda}{2\pi D^3} \right) \cos \sigma \quad (2.9)$$

$$E_\sigma = \frac{Z_0 I \ell}{2\lambda D} \sqrt{1 - \left( \frac{\lambda}{2\pi D} \right)^2 + \left( \frac{\lambda}{2\pi D} \right)^4} \sin \sigma \quad (2.10)$$



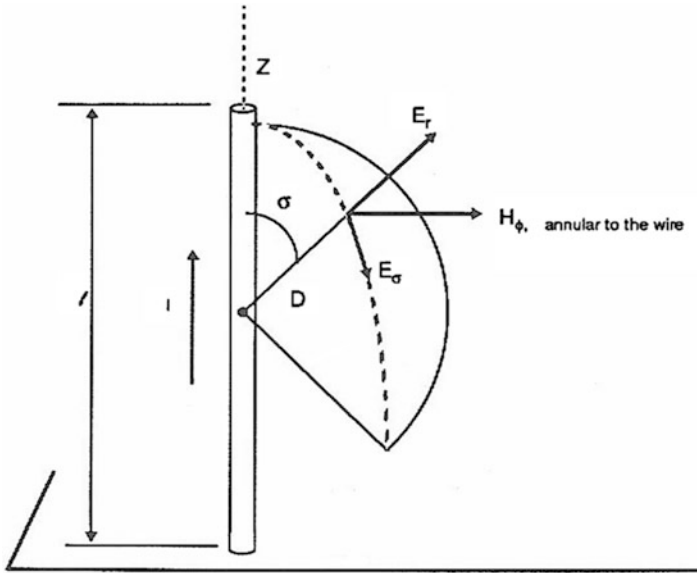


Fig. 2.3  $E$  and  $H$  fields from a small, straight wire

$$H_{\phi} = \frac{I\ell}{2\lambda D} \sqrt{1 + \left(\frac{\lambda}{2\pi D}\right)^2} \sin \sigma \quad (2.11)$$

where:

$I$  = wire current, in amperes

$\ell$  = dipole length in meters

$\lambda$  = wavelength in meter,  $300/F_{\text{MHz}}$

$D$  = distance to observation point in meters

$Z_0$  = free-space impedance,  $120\pi$  or  $377 \Omega$

As for the loop, we remark that for  $\sigma = 0$ ,  $E$  and  $H_{\phi}$  are null ( $\sin \sigma = 0$ ) while  $E_r$  is maximum ( $\cos \sigma = 1$ ).  $E_r$ , in the axis of the wire, is of little interest because it drops off rapidly, as  $1/D^2$ ,  $1/D^3$

In the equatorial plane for  $\sigma = \pi/2$ ,  $E$  and  $H$  have their maximum values. From now on we will consider this worst-case azimuth angle. In fact, for  $\sigma = 90^\circ \pm 25^\circ$ , the error would be less than 10%. As for the loop, we can see two domains plus a transition region.

**Near Field: For  $\lambda/2\pi D > 1$ , i.e.,  $D < \lambda/2\pi$  or  $D < 48/F(\text{MHz})$**

As for the loop, the terms with the higher exponent prevail, under the square root.

Neglecting the other second or third terms,

$$H_{A/m} = \frac{I\ell}{4\pi D^2} \quad (2.12)$$

$$E_{V/m} = \frac{Z_0 I \ell \lambda}{8\pi^2 D^3} \quad (2.13)$$

Here again, we remark that  $H$  annular around the dipole is independent of  $F$ . This formula holds down to DC, where it equals the well-known result of the Biot and Savart law for a small element. This time, it is to  $H$  to fall off as  $1/D^2$  while  $E$  falls as  $1/D^3$ . Both are strongly dependent on distance. Since, for a current kept constant,  $E$  decreases when  $F$  increases, the wave impedance decreases when  $D$  or  $F$  increases:

$$Z_w = \frac{E}{H} = Z_0 \frac{\lambda}{2\pi D} \quad (2.14)$$

As for the loop,  $Z_w$  near the source relates to the source impedance itself which, this time, becomes infinite when  $F$  gets down to DC.

**Far Field: For  $\lambda/2\pi D < 1$  (i.e.,  $D > \lambda/2\pi$  or  $D > 48/F(\text{MHz})$ )**

The terms with higher exponents can be neglected under the square root, so

$$H_{A/m} = \frac{I\ell}{2\lambda D} \quad (2.15)$$

$$E(V/m) = Z_0 \times I \times \ell(2\lambda D) \quad (2.16)$$

Both  $E$  and  $H$  decrease as  $1/D$ . This ratio, as for the loop in far field, remains constant:

$$E/H = Z_0 = 120\pi \text{ or } 377 \Omega$$

It is worth noticing that for a single wire in free space,  $E$  and  $H$  increase as  $F$  (instead of  $F^2$  for the loop).

**Transition Region: For  $\lambda/2\pi D < 1$  or  $D = 48 F(\text{MHz})$**

The same remarks apply as for the loop.

Figure 2.4 summarizes the evolution of  $Z_w$  for wires and loops as  $D/\lambda$  increases.

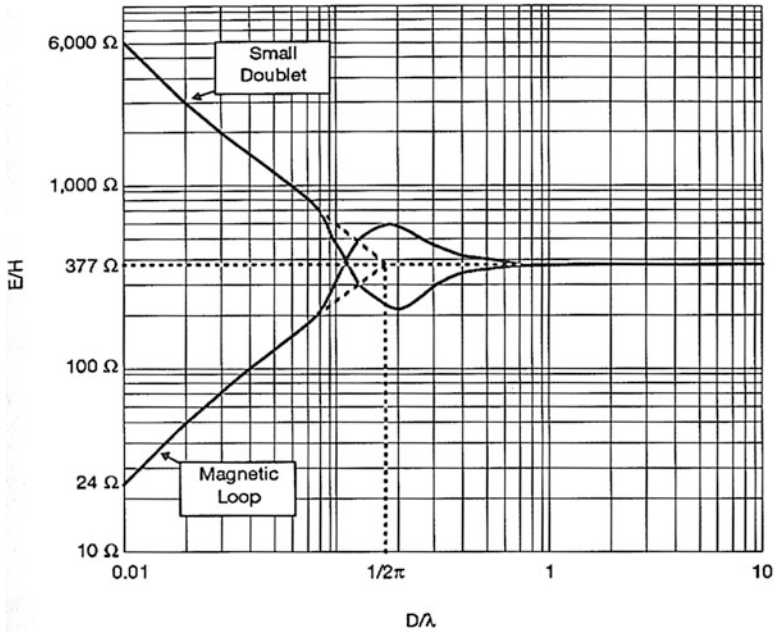


Fig. 2.4 Wave impedance vs. distance/wavelength

### 2.3 EXTENSION TO PRACTICAL, REAL-LIFE CIRCUITS

Although theoretically correct, ideal loop or doublet models have a limited practical applicability in EMC due to the restrictions associated with their formulas:

1. Distance  $D$  should be large compared to the circuit dimensions.
2. The circuit length should be less than  $\lambda/2$ , and preferably less than  $\lambda/10$ , for the assumption of uniform current to be acceptable.
3. The single-wire model corresponds ideally to a piece of wire floating in the air, in which a current is forced, a situation seldom seen in practice.
4. The single-wire model assumes that the circuit impedance is infinite in near field or at least larger than the wire reactance alone; this condition is rarely met except in dipole or whip antennas.
5. Restrictions 3 and 4 seem alleviated if one switches to the loop model. The loop, indeed, is a more workable model for practical, non-radio applications because it does not carry the premise of a wire coming from nowhere and going nowhere. But it bears a serious constraint, too: the loop must be a short circuit, such as the wave impedance, and hence the  $E$  field is only dictated by the coefficients in Maxwell's equational solutions. If this condition is not met (it is seldom met

except in the case of a coil with only one or few turns and no other impedance), the  $H$  field found by Equ. (2.6) and Equ. (2.7) will be correct, but the actual associated  $E$  field will be greater than its calculated value.

In reality, we deal with neither purely open wires nor perfect loops, but with circuit configurations which are in between. Therefore, predictions in the near field would produce:

- An  $E$  field higher than reality, if based on open-wire model (pessimistic error)
- An  $E$  field lower than reality, if based on ideal loop model (optimistic error)

Measurements have proven that the latter can cause underestimates as large as 60 dB or more. Therefore, certain adjustments need to be made. Assuming these adjustments, the modified equations and models can be usable by the designer for most of the actual circuits and cable configurations encountered, like the one in Fig. 2.5.

### 2.3.1 Fields Radiated by Actual Conductor Pairs

The core of this modeling is the “modified single-wire model” where, instead of a straight wire or circular loop, we have a more practical vehicle, where an area  $\ell \times s$  can be treated by the loop equation or regarded as two single wires with a radiation phase shift equal to  $\sin(2\pi s/\lambda)$ . Depending on the circuit impedance, we will use one or the other, as explained next. The basis for the simplification is that, in near field, the wave impedance  $Z_w = E/H$  is “driven” by the circuit impedance  $Z_c$  every time this circuit impedance is in between an ideal dipole that creates a high  $Z_w$  and an ideal loop creating a low  $Z_w$ .

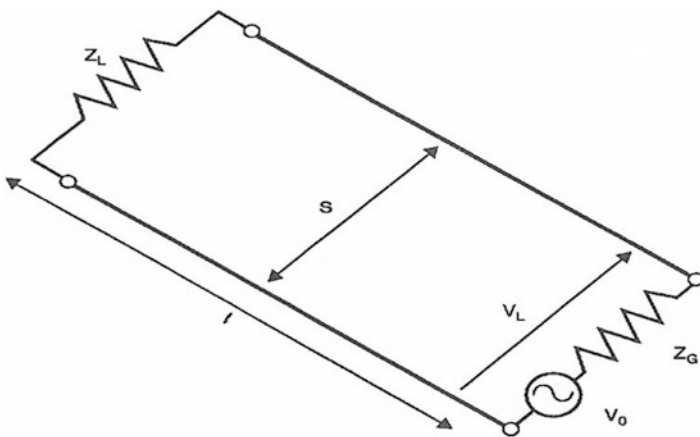


Fig. 2.5 The modified single-wire model

In the near field, given the total circuit impedance  $Z_c$  (wiring plus load),

$$Z_c = Z_g + Z_L$$

**A. If  $Z_c > 7.9 Dm \times F(\text{MHz})$ ,** we will use the modified wire model:

$$E_{V/m} = \frac{VA}{4\pi D^3} \quad (2.17)$$

where,

$V$  = driving voltage in volts (actual line voltage, not the open circuit voltage)

$A$  = circuit area  $\ell \times s$ , in  $\text{m}^2$

$D$  = observation distance, in m

Very often, more practical units are welcome:

$$E_{(\mu V/m)} = \frac{7.96 VA}{D^3} \quad (2.17a)$$

for  $V$  in volts,  $A$  in square centimeters, and  $D$  in meters.

**B. If  $Z_c < 7.9 D \times F(\text{MHz})$ ,** we will use the ideal loop formulas, since the circuit impedance is low enough for this model to hold.

$$E_{V/m} = \frac{0.63IAF_{\text{MHz}}}{D^2} \quad (2.18)$$

for current  $I$  in amperes,  $A$  in square meters, and  $D$  in meters. Or, using more convenient units:

$$E_{(\mu V/m)} = \frac{63IAF_{\text{MHz}}}{D^2} \quad (2.18a)$$

for current  $I$  in amperes,  $A$  in square centimeters, and  $D$  in meters.

Because, with such low-impedance radiating circuits, this is the  $H$  field which is of concern, we can employ a straightforward application of Equ. (2.4):

$$H(\text{A/m}) = I \times A / (4\pi D^3) \quad (2.18b)$$

for  $A$  in square meters and  $D$  in meters. Notice that this near-field expression is exactly the mirror image of the high-impedance loop  $E$  field in Equ. (2.17). The product  $I \times A$  is often referred to as the “magnetic moment.” Again, using more convenient units,

$$H_{(\mu\text{A/m})} = \frac{7.96 \times I \times A}{D^3} \quad (2.19)$$

for current ( $I$ ) in amperes,  $A$  in square centimeters, and  $D$  in meters. Therefore a *magnetic moment* is defined, in  $\text{amp} \times \text{cm}^2$ , abbreviated as  $\text{A}\cdot\text{cm}^2$ .

*In the far field*, regardless of the type of excitation (i.e., circuit impedance),  $E$  and  $H$  are given by Equ. (2.7) and Equ. (2.8), which we will reformulate in terms of frequency rather than wavelength:

$$E_{\text{V/m}} = \frac{0.013VAF_{\text{MHz}}^2}{D \times Z_c} \quad (2.20)$$

$$H_{\text{A/m}} = \frac{E}{120\pi} = \frac{35.10^{-6} \times I \times A \times F_{\text{MHz}}^2}{D} \quad (2.21)$$

with  $V$  in volts,  $I$  in amperes,  $A$  in square meters, and  $D$  in meters.

Or, once again using more practical units of measurement,

$$E_{(\mu\text{V/m})} = \frac{1.3}{D} \times \frac{V}{Z_c} \times A \times F_{\text{MHz}}^2 \quad (2.22)$$

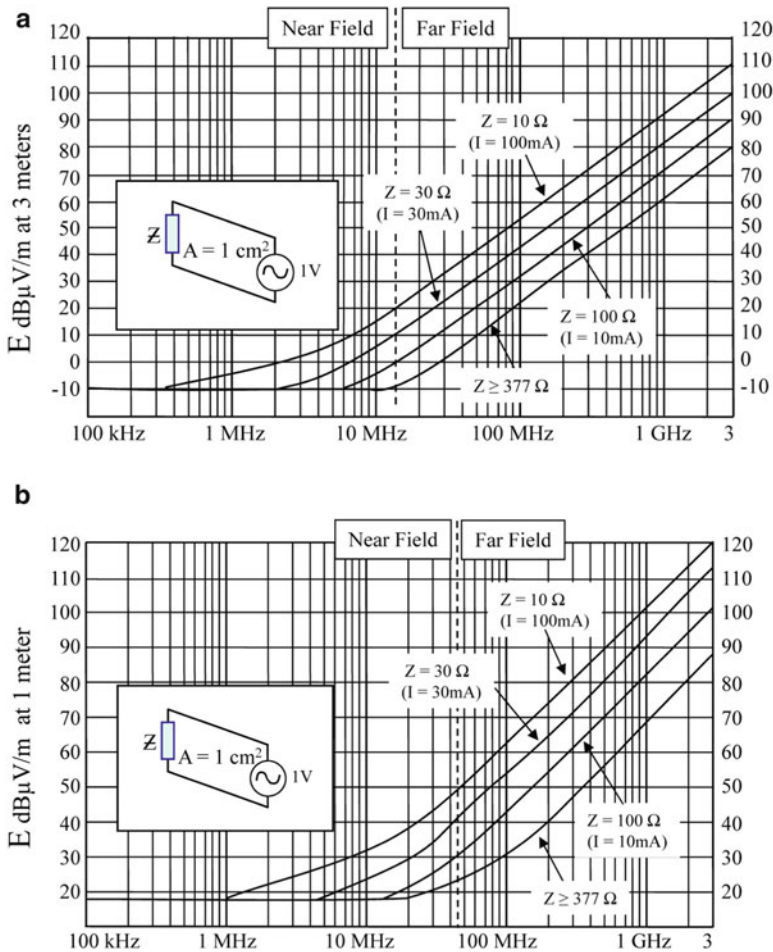
for  $V$  in volts,  $A$  in square centimeters, and  $D$  in meters.

At this point, a few remarks are in order:

1. We now have an expression for  $E$  fields that can be calculated by entering the drive voltage, which often is more readily known to the circuit designer than the current.
2. Except for very low-impedance loops (less than  $7.9 \Omega$  at 1 MHz, less than  $7.9 \text{ m}\Omega$  at 1 kHz), i.e., low-voltage circuits carrying large sinusoidal or pulsed currents, it is generally the wire pair model Equ. (2.17) and Equ. (2.19) that applies.
3. *In the near field*, for all circuits except low-impedance loops,  $E$  is independent of frequency and remains constant with  $V$ . At the extreme, if  $Z_c$  becomes extremely large, current  $I$  becomes extremely small but  $Z_w$  increases proportionally, keeping  $E$  constant when  $F$  decreases down to DC (more details in Appendix A “Modified dipole model”).
4. *In the far field*, radiation calculated for a two-wire circuit (the single-dipole formula times the weighing factor  $\sin 2\pi s/\lambda$  due to the other wire carrying an opposite current) would reach exactly the same formula as the one for a radiating circular loop. Therefore, as long as its dimensions are  $\ll \lambda$ , the actual circuit shape has virtually no effect on the radiated field in the optimum direction. Only its area counts.
5. For  $\ell \geq \lambda/4$ , the circuit begins to operate like a transmission line or a folded dipole. Current is no longer uniform, and in expressing  $A$ , the length  $\ell$  must be

clamped to  $\lambda/4$ , i.e.,  $\ell$  (m) is replaced by  $75/F_{\text{MHz}}$ . In other words, the active part of this fortuitous antenna will “shrink” as  $F$  increases. Furthermore, if the circuit does not terminate in its matched impedance, there will be standing waves, and the effective circuit impedance will vary according to transmission line theory. The radiation pattern will exhibit directional lobes.

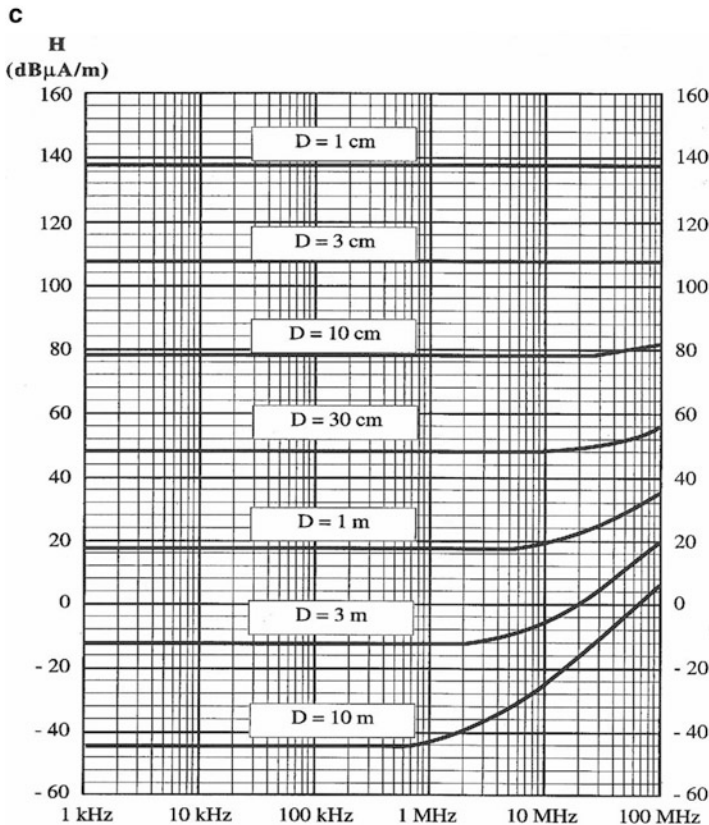
- When separation  $s$  is not  $\ll \ell$ , i.e., the loop is not a narrow rectangle but is closer to a square, the upper bound is reached [1] when  $(\ell + s) = \lambda/4$ , i.e.,  $F_{\text{max}} = 7,500/(\ell + s)$ , for  $F$  in MHz and  $\ell, s$  in centimeters. Furthermore,



**Fig. 2.6** (a)  $E$  field at 3 m from a  $1 \text{ cm}^2$  loop, driven by 1 V. For other voltages and  $(\ell \times s)$  values, apply correction:  $20 \log V + 20 \log(\ell \times s)$ . (b)  $E$  field at 1 m from a  $1 \text{ cm}^2$  loop, driven by 1 V. For other voltages and  $(\ell \times s)$  values, apply correction:  $20 \log V + 20 \log(\ell \times s)$

with conductors partly in dielectric, the velocity is reduced by a factor of  $1/\sqrt{(1 + 0.5\epsilon_r)}$ . For PVC or Mylar cables,  $F_{\max} = 5,300/\ell(\text{cm})$ . For PCB traces,  $F_{\max} = 4,400/\ell(\text{cm})$ . So an average value  $F_{\max} = 5,000/\ell(\text{cm})$  could be retained, above which the physical length should be replaced by  $5,000/F(\text{MHz})$ .

7. In the far field, if  $Z_c > 377 \Omega$ , the value of  $377 \Omega$  must be entered in Equ. (2.20). This acknowledges the fact that an open-ended circuit will still radiate due to the displacement current.
8. In the far field,  $E$  increases as  $F^2$  for a loop or a pair. This is a very important effect that we will address in the application part of this book. Equations (2.17a) to (2.22) are plotted in Fig. 2.6a–c for a “unity” electric pair of  $1 \text{ V}\cdot\text{cm}^2$  and a unity magnetic moment of  $1 \text{ A}\cdot\text{cm}^2$ . They show  $E$  or  $H$  at typical test  $d$  distances.



**Fig. 2.6** (continued) (c) Magnetic field from a 1 amp,  $1 \text{ cm}^2$  loop. For other currents and areas, apply correction:  $20 \log [I \times A(\text{cm}^2)]$



## 2.3.2 Fields Radiated by a Wire or Trace Above a Ground Plane

A frequent configuration is that of a single wire or PCB trace above a conductive plane acting as return or reference conductor. From image theory, a wire at a height  $h$  above a ground plane will radiate the same  $E$  field as a wire pair with separation  $2h$ , driven by the same voltage [1, 4]. Therefore, one can conclude that given a same voltage/current combination, the field radiated by any conductor at a distance  $h$  above a plane could be calculated from Equ. (2.17a), Equ. (2.18a), or Equ. (2.22) simply by using  $2h$  for the loop dimension. Yet, one must not forget that image theory is only valid for an infinite plane, which is seldom the case with a PCB, as will be explained next.

### 2.3.2.1 Finite Plane

As shown on Fig. 2.7, the finite plane allows the return current to radiate a magnetic field that surrounds the PCB, hence it radiates in all directions, that is a  $360^\circ$  solid angle (or  $4\pi$  steradians) and not just in the half space. Close to the wire and plane, the field contour is approximately the same as if the plane was infinite. But for an observation point  $P$ , at a distance  $D$  much larger than the PCB dimensions, the trace above ground merely radiates like a 2-conductor pair with height  $h$ , the return conductor being the plane itself.

### 2.3.2.2 Quasi-Infinite Plane

However, there are cases where image-plane conditions actually exist:

- Typical radiated emission (RE) tests of an equipment with its external cables are performed at 1, 3, or 10 m, with a conductive ground surface (semi-anechoic room or open-area test site) extending far beyond the test setup. In this case the doubling of the field by the image mechanism is real at certain frequencies (see Sect. 2.5.2).
- When calculating  $E$  or  $H$  field in close proximity of a chip or trace, if the distance  $D$  is  $\ll$  than PCB dimensions, we can accept the finite plane conditions and use  $2h$  for the loop size.

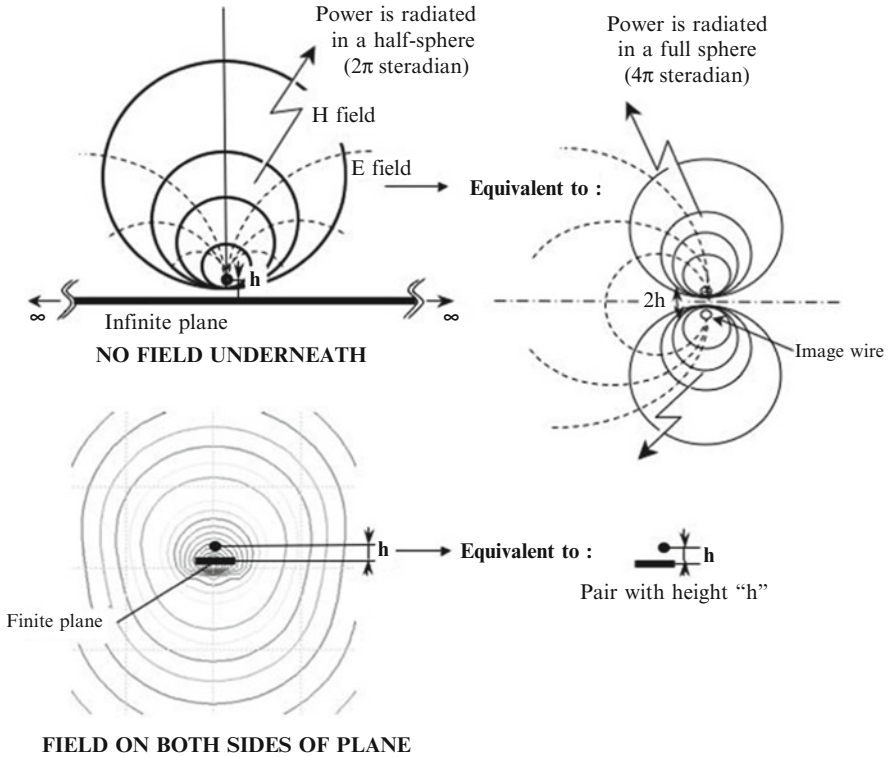


Fig. 2.7 Image mechanism with infinite and finite ground planes

## 2.4 DIFFERENTIAL-MODE RADIATION FROM SIMPLE CIRCUITS

The simplest radiating configuration we will encounter in practice is the small differential-mode radiator, whose largest dimension,  $\ell$ , is smaller than both the observation distance,  $D$ , and the height above ground. Such circuits (see Fig. 2.8) are found with:

- PCB traces, truly differential or microstrip (one trace above ground plane)
- Wire wrapping or any hard-wired board or backplane
- Ribbon cables
- Discrete wire pairs (for  $\ell \ll D$ )

The culprit source exciting such circuits can be a digital or analog signal, a switching transistor, a relay, a motor creating transient spikes, etc. There is also a possibility that the differential pair is simply a carrier of an EMI signal that has been generated in the vicinity and coupled to it through power supply conduction or nearby crosstalk.

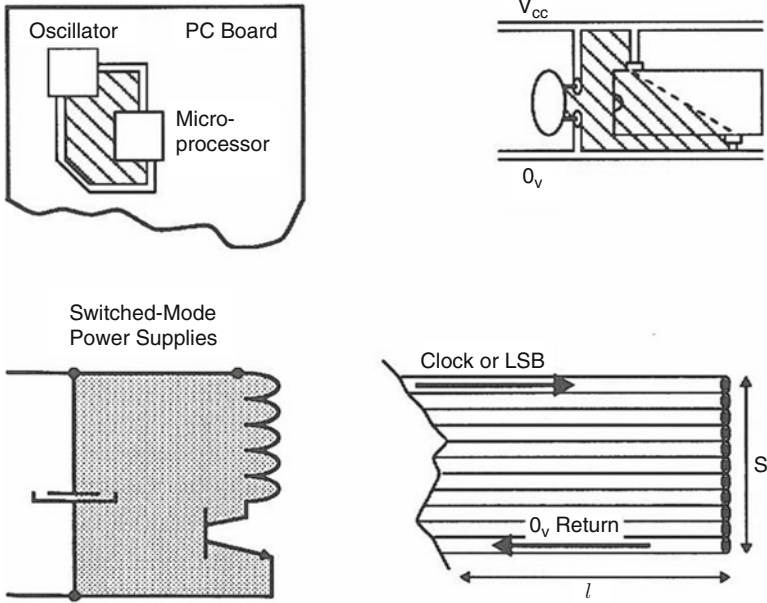


Fig. 2.8 A few typical differential-mode radiators

The procedure is then as follows:

1. Determine  $V_{\text{diff}}$ ,  $I_{\text{diff}}$  at the frequencies of interest and the circuit impedance.
2. Check for test distance  $D \geq 48/F_{\text{MHz}}$  (far-field conditions).
3. If far field, use the curves in Fig. 2.6 or Equ. (2.20).
4. If near field, determine if the circuit belongs to the low- $Z_c$ , loop model (for  $Z_c < 7.9 \times F \times D$ ) or to the wire model ( $Z_c > 7.9 \times F \times D$ ).
5. Check if  $\ell$  (cm)  $> \lambda/4$  or  $5,000/F$ . If  $\ell$  is larger, replace  $\ell$  by  $5,000/F$  for area correction.
6. Repeat Step 5 for wire or trace separation,  $s$ .
7. Calculate  $A \text{ cm}^2 = \ell \times s$  and determine area correction,  $20 \log A$ , using adjustments (5) and (6), if needed. For a trace above a ground plane, do not apply image theory, since the plane is not infinite. Simply use  $A = \ell \times h$ .
8. Find the  $E$  field by:  $E$  (dB $\mu\text{V}/\text{m}$ ) =  $E_0$  (from curves) +  $20 \log A$  +  $20 \log V$ .
9. If  $H$  field calculation is desired instead, use the  $H$ -field curves and add corrections.

**Example 2.1** A video signal crossing a PC board is to be switched to different displays. The carrier is 100 MHz with a line voltage of 10 Vrms. The PCB has the following characteristics:

- Single-sided, one layer (no ground plane)
- Average video trace length,  $\ell = 6$  cm
- Average distance to ground trace,  $s = 0.5$  cm

Calculate the  $E$  field at 1 m vs. the RE102 limit of MIL-STD-461 when:

1. The circuit is loaded with  $75 \Omega$ .
2. The circuit is “on” but standby, open-ended.

We will assume, as a starting condition, that there is no box shielding.

- $V_{\text{diff}} = 20 \text{ dBV}$  (loaded) or  $26 \text{ dBV}$  when open-ended (the voltage will double).
- At  $100 \text{ MHz}$ , the near-field/far-field transition distance is

$$D_{N-F} = 48/100 = 0.48 \text{ m}$$

Therefore, at 1 m we are in far-field conditions. We can use Fig. 2.6 or Equ. (2.22).

- Area correction:  $20 \log(6 \times 0.5) = 10 \text{ dB}$ . The 6 cm length is  $< \lambda/4$  at  $100 \text{ MHz}$ .
- For the  $75 \Omega$  load, we can interpolate between the  $30$  and  $100 \Omega$  curves. For the open circuit ( $Z = \infty$ ), we will use the curve for  $Z \geq 377 \Omega$ .

The calculations steps are detailed below:

Frequency	100 MHz (with $Z = 75 \Omega$ )	100 MHz (open circuit)
$E_0$ (for $1 \text{ V} \times 1 \text{ cm}^2$ )	44 dB $\mu\text{V}/\text{m}$	30 dB $\mu\text{V}/\text{m}$
Amplitude correction	20 dBV	26 dBV
Area correct. ( $\text{cm}^2$ )	10 dB	10 dB
$E$ (final)	74 dB $\mu\text{V}/\text{m}$	66 dB $\mu\text{V}/\text{m}$
$E$ specification limit	29 dB $\mu\text{V}/\text{m}$	29 dB $\mu\text{V}/\text{m}$
$\Delta \text{ dB}$	45	37

The specification limit is exceeded by 37-45 dB. Such an attenuation can only be obtained, in practical terms, by using a multilayer board or a single-layer board with a ground plane. This would reduce the radiating loop width by a ten-times factor, i.e., 20 dB, and a correctly designed metal housing to provide at least 25 dB of shielding at 100 MHz. Both solutions will be discussed further in this book.

**Example 2.2** A 5 V/20 A switching power supply operates at the basic frequency of 50 kHz. In the secondary loop (formed by the transformer output, the rectifier, and the electrolytic capacitor), the full-wave rectified current spikes have a repetition frequency of 100 kHz and an amplitude of 60 A (peak) on the fundamental. Loop dimensions are  $3 \times 10 \text{ cm}$ . The loop impedance at this frequency is  $0.2 \Omega$ . Calculate  $E$  and  $H$  at 100 kHz for a 1 m distance.

1. The 60 A amplitude corresponds to 36 dBA.
2. At 100 kHz, the near-far transition distance is  $D_{N-F} = 48/0.1 = 480 \text{ m}$ . So, at 1 m, we are in very near field.
3. With  $Z_c = 0.2 \Omega$ , we meet the criteria for  $Z_c < 7.9 \times F \times 1 \text{ m}$ .
4. The area correction is  $20 \log(30 \text{ cm}^2) = 30 \text{ dB}$ .

We will use the ideal loop model, i.e., Fig. 2.7 or Equ. (2.19) for  $H$  field and Equ. (2.18a) for  $E$  field. The field is computed as follows:

Frequency	0.1 MHz	0.1 MHz
$H_0$ (1 A - 1 cm <sup>2</sup> )	17 dBμA/m	
$E_0$ (1 A - 1 cm <sup>2</sup> )		16 dBμV/m
Amplitude correction (amp)	36 dB	36 dB
Area correction (cm <sup>2</sup> )	30 dB	30 dB
$H$ (final)	83 dBμA/m	
$E$ (final)		82 dBμV/m

Notice that the wave impedance for this predominantly magnetic field at 1 m has a value of

$$Z_w = E/H = 82 \text{ dB}\mu\text{V/m} - 83 \text{ dB}\mu\text{A/m} = -1 \text{ dB } \Omega \text{ or } 0.9\Omega$$

## 2.5 COMMON-MODE RADIATION FROM EXTERNAL CABLES

External cables exiting an equipment are practically always longer than the size of the equipment box, so it is predictable that they will be major contributors to radiated emissions (just as they would be for radiated susceptibility). Cables radiate by the differential-mode signals that they carry, as discussed in the previous section, but also by the currents circulating in the undesired path, that is, the ground loop.

Ground loop CM (common mode) currents are due to the unbalanced nature of ordinary transmitting and receiving circuits, the imperfect symmetry of the differential links, and, more generally, the quasi-impossibility of avoiding some CM return path, whether the loop is visible (circuit references grounded at both ends to chassis and/or earth) or invisible (floated equipments or plastic boxes). This phenomenon of common-mode excitation of external cables causing radiated emissions is one of the most overlooked one in computers and high-frequency devices interference [2].

The very simple example of Fig. 2.9 shows the unavoidable generation of a CM current. Assume that over a cable length  $\ell$ , the wire pair (untwisted) separation is  $s = 3$  mm, and the cable height above ground is  $h = 1$  m. When a signal is sent from equipment #1 to equipment #2, although the designer believes in good faith that current is coming back via the return wire, we see no reason why some of the current ( $i_3$ ) could not return by the unintended path, i.e., the ground loop.

Currents  $i_2$  and  $i_3$  will split in proportion to the respective impedances. If the wires in the pair are in close proximity, the return impedance by the pair is significantly less than the return impedance via the ground. But less does not mean null. Let us assume that only 10% of the current is returning by the ground loop. The differential-mode (DM) radiation is related to  $0.9i \times \ell \times s$ . The CM radiation is related to  $0.1i \times \ell \times h$ . The ratio of the two magnetic moments is

$$\text{CM/DM} = (0.1i \times \ell \times 1 \text{ m}) / (0.9i \times \ell \times 0.003 \text{ m}) = 37$$

$$20 \log 37 = 31 \text{ dB}$$

This CM loop, although the corresponding current is regarded as a side effect, radiates 31 dB above the DM loop (notwithstanding that this latter can be further reduced by twisting).

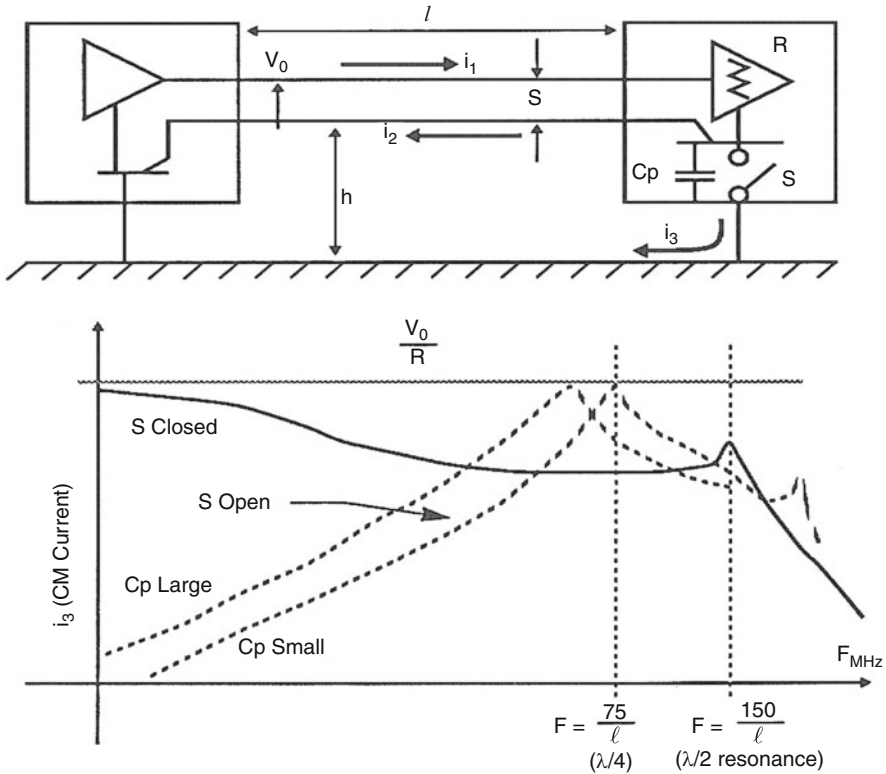


Fig. 2.9 Conceptual view of CM current generation by a differential signal

Opening the switch  $S$ , i.e., floating the PCB 0 V reference, would reduce  $I_{cm}$  at low frequencies (below a few megahertz for a 10 m cable). In this range, radiated EMI is generally not a concern; but the problem would aggravate at first cable resonance because we now have an oscillatory inductance-resistance-capacitance (LRC) circuit with a high  $Q$  (low  $R$ ). The hump in CM current (Fig. 2.9) depends on the value of  $C_p$ , the PCB stray capacitance to chassis. At this occasion, we see that the traditional recipe of grounding the PCB only at one box (star grounding) is useless in the frequency range of most radiation problems. It can even be slightly worse at some specific frequencies.

The undesired CM currents that are found on external cables can be some percentage of the signal currents that would normally be expected on this interface, but, more often, cables are found to carry high-frequency harmonics *that are not at*

all part of the intentional signal (see Fig. 2.10). Rather, they have been picked up inside the equipment by crosstalk, ground pollution, or power supply DC bus pollution. Since the designer did not expect these harmonics, it is only during FCC, CISPR, MIL-STD-461, or other compliance testing that they are discovered.

Figure 2.10 shows the contrast between (a) what is normally expected: power line carries only 50/60 Hz or 400 Hz currents, *I/O* cable carries a slow serial bus, and the 10 MHz clock is used only internally and (b) what real life provides: *I/O* pairs or ribbon cable carries 10 MHz residues from the clock, picked up internally; their spectrum extends easily to 200 or 300 MHz. Because of the primary-to-secondary capacitance in the power supply transformer, power wires (phase, neutral, and ground) are also polluted by 10 MHz harmonics. The radiating loops can be ABCD, ABEF, or combinations of all.

Predicting such radiated emissions from external cables will consist of the following:

- Measuring or estimating the CM currents driving the external cables
- Estimating the geometry for the CM-driven antenna
- Applying simple, appropriate antenna formulas (loop or open wire)

These three steps of prediction are examined next.

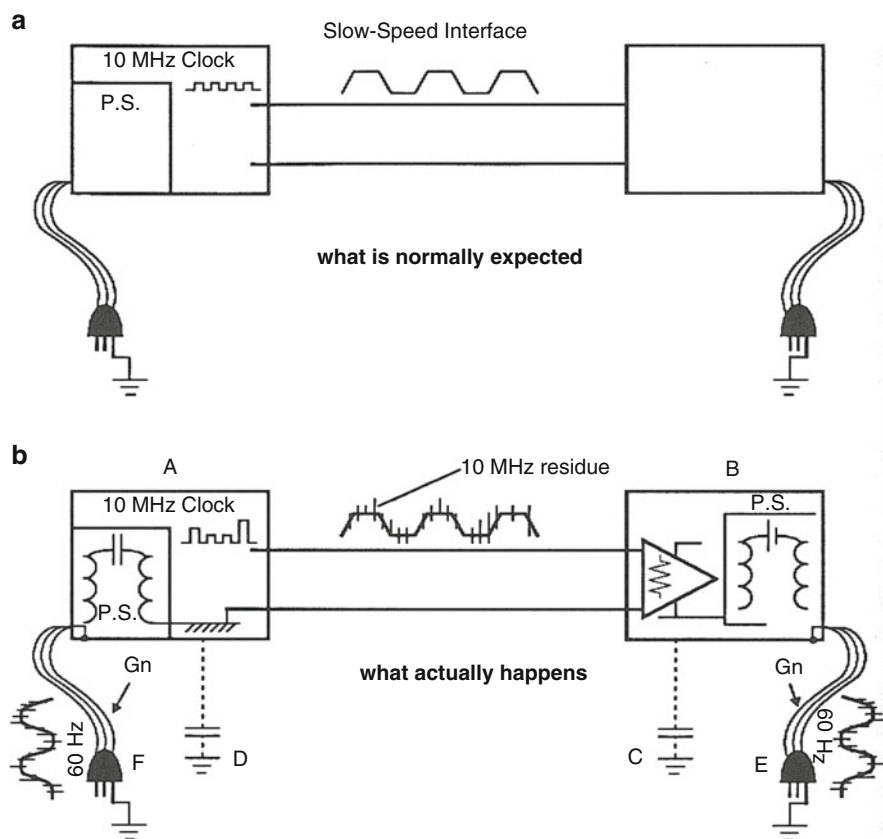


Fig. 2.10 Contamination of external cables by internal HF circuits

## 2.5.1 How to Estimate CM Currents on Cables

As stated before, the CM currents found on external cables can have essentially two origins. The mechanisms that are causing such currents are analyzed hereafter.

### 2.5.1.1 CM Current from Intentional Signals

By this, we mean the portion  $i_3$  (generally undesired) of signal current that is returning by the external ground loop. Let us review the three principal cases.

#### – *Single-Wire Transmission*

The useful signal is carried on a single wire, the chassis, or other structural system ground forming the return path. This type of link is, of course, highly detrimental for EMC and almost never used anymore. Few exceptions are found in automobile, aircraft, or helicopter applications where certain signals are still carried between a hot wire and the vehicle body, to save on copper weight. In this case, the full signal spectrum is driving the single-wire antenna.

#### – *Unbalanced, Two-Wire Transmission* (RS232, RS423, etc.)

This time, the CM current is the % of the signal current which “elect” to return by the external path instead of using the return wire. Above a few kHz, the mutual inductance between the two wires is strong enough to attract most of the current into the intended path  $i_2$  (Fig. 2.9), leaving only 20–30% of the current returned by the ground loop ( $i_3$ ). Unless one knows the exact value of the mutual inductance, which itself varies with the cable height and wire separation, a conservative value is to expect  $i_3 = i_1 - 10$  dB. This is of course assuming an unshielded cable (see Chap. 11 for the additional suppression by a shield).

#### – *Unbalanced Coaxial Transmission* (RF, Video, Ethernet, etc.)

This type of link is inherently low radiating, due to the high % of current—typically more than 99%—returning by the shield. This, too, is covered in Chap. 11.

#### – *Differential Transmission* (RS422/485, MIL-STD-1553, Diff. SCSI, CAN, USB, LVDS, IEEE 1394, Ethernet, HDMI, etc.)

With such links, the transmitter and receiver circuits have been designed to force balanced currents into the wire pair. In addition to excellent immunity and low crosstalk, this maintains also a low CM current generation, hence less EMI radiation. Along with the symmetry of the driver and receiver, a good symmetry of the wire pair is also required, such as the overall balance of the transmission is within the 1-10% range. Unless it is exactly known, we can conservatively assume 5%, i.e., the CM current  $i_3$  will be at least 26 dB below  $i_1$ .



### 2.5.1.2 Non-intentional Signals

As shown on Fig. 2.10, these are residue of clock frequencies, switch-mode power regulators, etc., coupled onto PCB *I/O* traces from:

- Ground traces/plane noise
- $V_{cc}$  pollution (this in turn is partially transferred to *I/O* lines by some “transparency” in the driver or receiver ICs)
- Crosstalk

They can also be coupled by near-field radiation from the PCB hot spots onto the exiting cables, because of box shield leakages around the connector area. These leaks are causing the two (or more) wires to be CM-driven like a single conductor. The first difficulty is to evaluate the amplitude of these undesired signals. A pragmatic approach is to measure their voltage or current spectrum directly on the cable itself. This is easy to do at a diagnose and fix level, but it requires at least a representative prototype at the design stage. How can one do this when the hardware does not yet exist? A deterministic approach would consist in calculating every possible internal coupling between the inner circuitry and the leads corresponding to *I/O* ports. This is feasible but takes a considerable amount of time. A crude but effective solution is to make the following assumption by default: *Unless one knows better, it is logical to assume that the noise picked-up by internal couplings is just below the immunity level of the circuits interfacing the external link in question.*

The rationale for the above is that designers will at least make their product functionally sound; if worst-case values were exceeded (e.g., 0.4 V for a digital input noise margin), the system simply would not operate properly.

**Example 2.3** A serial link between a computer and its peripheral operates at a 20 kb/s rate. The internal circuitry uses a 50 MHz clock with associated Schottky logic circuits, with the following characteristics:

- Amplitude = 3 V
- Rise time (STTL) = 3 ns
- Noise margin (worst case) = 0.3 V

Not knowing the exact layout of the inner circuit, estimate the worst possible noise picked-up by the 20 kb serial link.

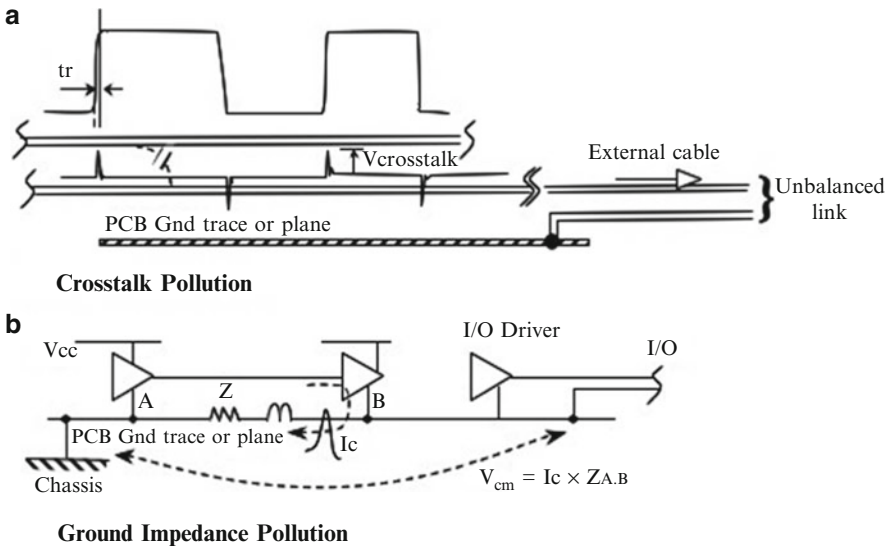
Lacking of any other data, we can make the following worst-case assumptions (Fig. 2.11):

- The amplitude of any parasitic coupling from a clock-triggered pulse to a nearby trace or wire will not exceed the 0.3 V noise margin.
- Because crosstalk and ground-impedance sharing are all derivative mechanisms, the pulse width of the coupled spike on the victim trace will be in the range of 3 ns. STTL transition time. This is a worst-case guess since pulse stretching and ringing will occur due to distributed parameters of the victim line.
- If crosstalk exists, it will appear as a differential (signal-to-Gnd) noise at the *I/O* port.

Therefore a DM-to-CM reduction factor must be applied to the driven cable, like -10 dB for an ordinary unbalanced link (see previous Sect. 2.5.1.1, Unbalanced 2-Wire Transmission)

*In Summary*

- The crosstalk pollution of the low-speed *I/O* link by the internal 50 MHz spurious will appear as 0.3 V, 3 ns-wide spikes, with alternating positive and negative sign, riding over the 20 kb signal pulses train. Approximately 2/3 of the corresponding current will flow differentially in the pair, causing only minor radiation. The remaining 1/3 will return via the large cable-to-earth loop, causing a CM loop radiation with a spectrum populated by 50 MHz harmonics.
- The PCB ground pollution by the same 50 MHz spurious will appear as unipolar pulses (Fig. 2.11b) because they correspond to the transient overcurrent demand (“thru-current”) of digital gates at each 0-to-1 or 1-to-0 transition. The resulting PCB ground noise can be shared by several circuits in this board area, forcing CM currents into the whole *I/O* pair, returning by the local chassis or facility ground. This coupling is likely to be the greatest threat because it excites entirely the cable-to-ground loop, without DM-to-CM conversion loss.



**Fig. 2.11** Coupling of internal clock transitions by crosstalk to *I/O* traces

### 2.5.2 Approximating the Proper Radiating Geometry

Having determined the CM current driving mechanism, we now have to figure out what is the driven antenna: closed loop or open wire? Although they are gathering many configurations in two rather crude configurations, resorting to these two simple models gives remarkably good results when compared to actual validation test data.

#### 2.5.2.1 Loop with Defined Contour

By this term, we do not imply necessarily that the loop is physically closed; the signal grounds (0 V Ref.) may or may not be connected to chassis or earth reference at both ends. If the I/O cables are connecting to metallic equipment cases (and hence are most likely grounded), the CM radiating loop is geometrically identified by its size  $\ell \times h$  (Fig. 2.9). If the ground references are floated inside the box, this will increase the low-frequency impedance of the loop, yet its size remains. Therefore, depending on the loop impedance and the near-field or far-field conditions, we will apply either the loop equations or the two-wire equations of Sect. 2.3.

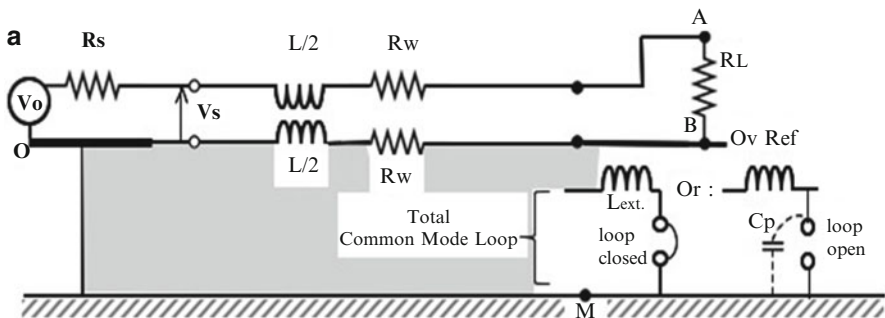


Fig. 2.12 (a) Loop Impedance of External Cables Radiation

**For all-grounded ends** (PCB to chassis and chassis to local earth network), the current  $i_1$  delivered by the signal source to the line termination  $R_L$  is splitting in two possible return paths (Fig. 2.12b):

- Current  $i_3$  returning to the source reference by the large cable-to-ground CM loop. The loop impedance seen by this  $i_3$  current is

$$Z_{CM} = R_w + R_L + j\omega L_{CM} \tag{2.23}$$

where  $L_{CM}$  is the wire self-inductance above ground plane.  $R_w$  (typ.  $0.1 \Omega/m$ ) can be neglected, and typical value for  $L_{CM}$ , with heights in the 0.1 to 1 m range, is 1-1.5  $\mu H/m$ , and so Equ. (2.23) is rewritten in a more convenient way:

$$Z_{CM} = R_L + j7.5 \Omega \times \ell_m \times F_{MHz} \tag{2.23a}$$

The amplitude of  $i_3$  is approximately the value that the return current would take if the second wire of the pair did not exist. This current is the major contributor to cable radiation, via the CM loop.

- Current  $i_2$  is returning back to its source via the return wire of the pair. The total loop impedance seen by this current  $i_2$  is

$$Z_{diff} = 2R_w + R_L + j\omega L_{diff} \tag{2.23b}$$

where  $L_{diff}$  is the differential loop self-inductance of the pair. This inductance is substantially lower than that of the large CM loop, thanks to the mutual inductance between the closely spaced wires. For typical, small-gauge signal wire, this 2-wire inductance is in the order of 0.5-0.6  $\mu H/m$ .

The total output current  $i_1$  is the combination of  $i_2 + i_3$ .

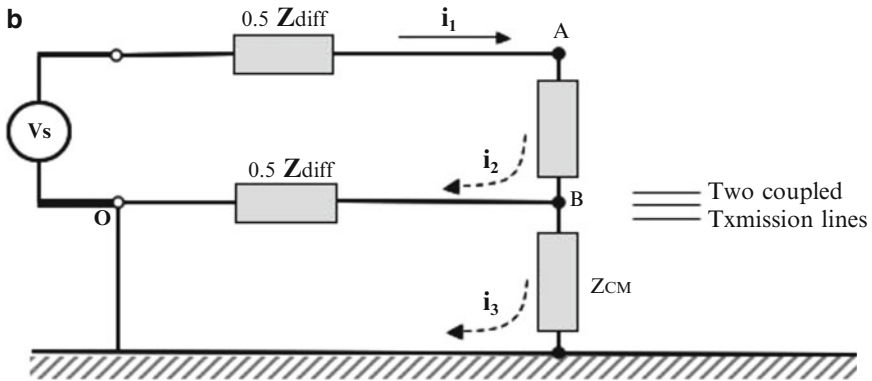


Fig. 2.12 (b) Split of return currents in the Loop Impedances of External Cables Radiation

For a floated end, the loop impedance seen by the CM current is

$$Z_{CM} = R_w + R_L + (j\omega L_{CM} - j/C_p\omega) \tag{2.24}$$

$$\approx 1/C_p\omega \text{ for low frequencies.}$$

where  $C_p$  is the PCB-to-chassis stray capacitance ( $\approx 30$  pF for small boxes, 100-200 pF for large cabinets). When cable length exceeds  $\lambda/2$  (for both ends

grounded) or  $\lambda/4$  (for one end floated),  $Z_{CM}$  can be approximated by the characteristic impedance of the cable above ground:

$$\text{in the air, } Z_0 = 60 \text{Ln}(4h/d) \quad (2.25)$$

where,

$\text{Ln}$  = natural logarithm

$d$  = cable diameter (average contour of whole wire bundle)

Practical  $h/d$  range of 3-100 gives a span of  $Z_0$  from 150 to 360  $\Omega$ . The low value would correspond to a typical MIL-STD-461 test setup, the high value being the extreme for a tabletop equipment in an FCC or CISPR test. A typical real-life value would be 250  $\Omega$ .

**Example 2.4** A 5 MHz clock is used on a short-haul parallel bus. For a 5 V pulse, the ninth harmonic, at 45 MHz, has an amplitude of 0.3 V. The characteristics of the I/O cable between the two metallic equipments are:

1. Cable length,  $\ell = 1.20$  m
2. Height,  $h = 0.30$  m
3. Inductance of cable above ground  $L = 1.2$   $\mu\text{H/m}$
4. Terminating resistor = 120  $\Omega$

Calculate the 45 MHz  $E$  field at 3 m vs. the FCC Class B limit for (a) both PCBs grounded to chassis and (b) one PCB 0 V ground floated, with a total stray capacitance of 30 pF.

### Solution

- $D = 3$  m  $>$  48/45 MHz, so we are in far-field conditions.
- $\ell(\text{m})$  and  $h(\text{m})$  are  $<$ 75/45 MHz, so we are below cable “antenna” resonance.

We can use directly Equ. (2.20) or Fig. 2.6 curves for 3 m distance:

$$\text{Area} = 120\text{cm} \times 30\text{cm} = 3,600\text{cm}^2 = 72\text{dB cm}^2$$

- (a) *For grounded condition*, the cable is essentially an inductance; impedance is calculated from Equ. (2.23a):

$$Z_{\text{cm}} = 120 \Omega + j(7.5 \times 45 \text{MHz} \times 1.2 \text{m}) = 420 \Omega$$

- (b) *For floated condition*, the cable inductance resonates with the floating PCB capacitance at

$$F_{\text{res}} = 1/2\pi\sqrt{LC} = 1/2\pi\sqrt{(1.2\text{m} \times 1.2 \cdot 10^{-6}\text{H} \times 30 \cdot 10^{-12})} = 24 \text{MHz}$$

Therefore, due to resonance downshifting caused by the stray capacitance, the cable is now beyond resonant condition. We will use a typical characteristic impedance of 250 Ω, dictating the average value of the current along the cable.

*Calculation spread sheet for 45 MHz frequency*

1) $E_0$ in Fig. 2.6 (for 1 V - 1 cm <sup>2</sup> )		
– For Z: 420 Ω:	<b>8 dBμV/m</b>	
– For Z: 250 Ω (floated):		<b>11 dBμV/m</b>
2) Area correction	+72	+72
3) Amplitude corr. (0.3 V)	-10	-10
4) $E = 1 +2 +3$	70 dBμV/m	(73 for floated)
FCC limit, Class B	40 dBμV/m	
Off specification	30 dB	(32 for floated)

For the all-grounded case, a quick analysis of the circuit in Fig. 2.12b, with the variables of the example, gives the following current split:

- $i_1$  (upper wire) = 2 mA
- $i_2 = 1.3$  mA
- $i_3 = 0.7$  mA, which is 10 dB below  $i_1$

This is due to the DM loop inductance of the wire pair being approximately a third of the large CM loop inductance. Notice that we have passed the point where a floated PCB could be of any use. The exact calculation of  $I_{average}$  could be made using transmission line theory and would give slightly different results for each resonant condition. To reduce this excessive emission will require one of the several solutions (e.g., CM ferrites, cable shield, balanced link) that we will examine later.

### 2.5.2.2 Open Wire, Monopole or Dipole

We now examine the case where no geometric loop can be identified (Fig. 2.13). The external cable terminates on a small, isolated device (sensor, keypad, etc.) or into a plastic, ungrounded equipment. It may even not be terminated, waiting for a possible extension to be installed. No finite distance can be measured to a ground plane. In this case, we use the single-wire radiation model described in Sect. 2.2.

In a sense, we can say that the floating, open wire is the maximum radiating antenna that can be achieved when the height of a ground loop increases to infinity. To calculate the radiated field using Equ. (2.13) or Equ. (2.16) requires that the CM current in the wire be measured or calculated. Measurement with a high-frequency current probe is easy, but only if a prototype is available. Otherwise, one can simply use the cable self-capacitance of  $\approx 10$  pF/m for low-frequency modeling and the cable characteristic impedance Equ. (2.25) with high values of  $h$ , above the first resonance.

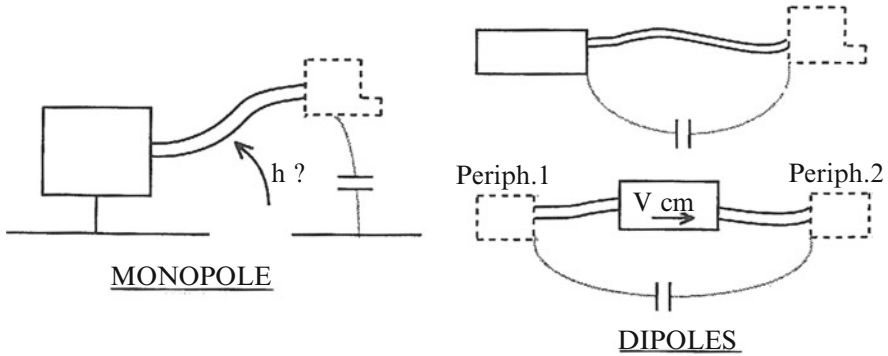


Fig. 2.13 Common-driven monopole or dipole

Using more practical units, single-wire radiation is expressed as

$$\text{In the near field, } E_{(\mu\text{V/m})} = \frac{1,430 \times I_{\mu\text{A}} \times \ell_m}{D^3 F_{\text{MHz}}} \quad (2.26)$$

$$\text{In the far field, } E_{(\mu\text{V/m})} = \frac{0.63 I_{\mu\text{A}} \times \ell_m \times F_{\text{MHz}}}{D_m} \quad (2.27)$$

If the cable interconnects two units that are completely floated and not close to any ground, the length,  $\ell$ , is regarded as a radiating dipole length. If one of the two units is grounded or is in a metallic case close to ground, the cable has to be regarded as a radiating monopole whose length,  $\ell$ , radiates like a dipole twice as long. In this case,  $2\ell$  should be entered in the formula.

Of course, wire lengths may exceed  $\lambda/2$  ( $\lambda/4$  for a monopole). In this case, the current can no longer be regarded as uniform over the wire length. But the “active” segment of the radiator cannot exceed a length of  $\lambda/2$ . The other  $\lambda/2$  segments create fields that mutually cancel due to phase reversal (except for the field propagation delays, which are unequal). Everything behaves as if the antenna were electrically “shrinking” as  $F$  increases. In this case,  $\ell$  must be replaced by  $\lambda/2$  in the formula.

Applying a correction factor averaging  $I_{\text{max}}$  over the length, we have, for free space,

$$E_{(\mu\text{V/m})} = \frac{60 I_{\mu\text{A}}}{D} \quad (2.28)$$

Interestingly, we observe that  $E$  becomes independent of  $F$  and  $\ell$ . This formula is extremely useful, and we will employ it frequently.

**Example 2.5** For the same 5 Mb/s signal as in Example 2.4, assume that the 1.20 m cable now terminates into a plastic equipment on one end. The cable is far from

any ground plane. What is the maximum CM current tolerable on this cable to meet the FCC (B) 3 m limit of 100  $\mu\text{V}/\text{m}$  at 45 MHz (harm #9) and 85 MHz (harm #17)?

- At 45 MHz,  $\ell < 75/F$ . From Equ. (2.27), remembering that we have a monopole, a length  $2\ell$  is entered as radiating length:

$$E = 0.63I \times (1.20 \times 2) \times 45 \text{ MHz}/3 \text{ m}$$

Solving for the current  $I$ ,

$$I < E/22.5 \text{ so, } I < 4.4 \mu\text{A}$$

- At 85 MHz,  $\ell > \lambda/4$ . We will use Equ. (2.28):

$$E = 60I/D$$

$$I \leq ED/60, \text{ so } I < 5 \mu\text{A}$$

Therefore, before running an exhaustive radiated EMI test, a simple measurement on the cable with a high-frequency current probe will indicate whether the equipment has a good chance of meeting the specification.

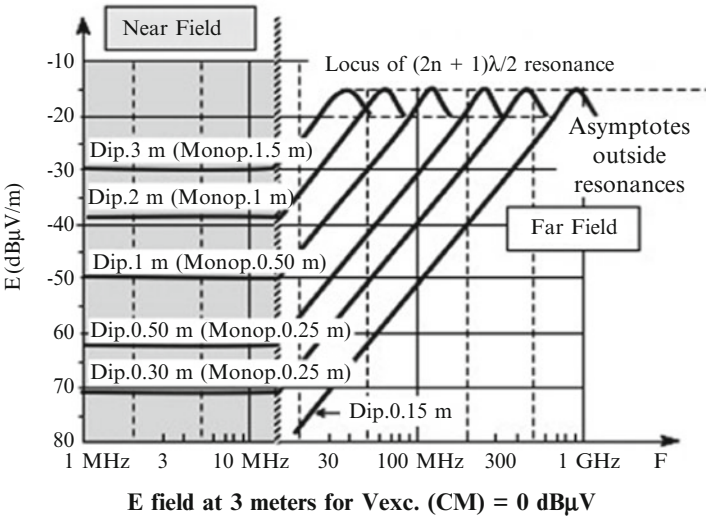
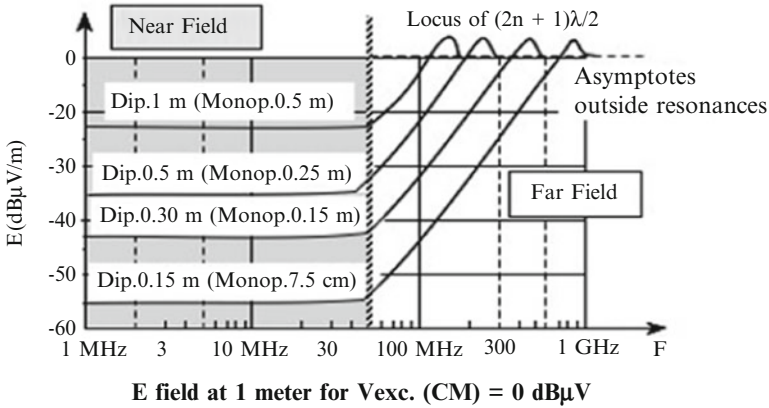
### 2.5.2.3 Simple Voltage-Driven Nomograms for Open Wire

If the CM current cannot be measured on a prototype, instead of computing the open-wire impedance at each frequency, the nomogram of Fig. 2.14 for isolated wires can be used for a quicker estimate. All that is needed is the value of the voltage(s) driving the monopole or dipole. The curves are based on cable capacitance, for electrically short lines, and a conservative 150  $\Omega$  CM impedance otherwise. Notice that, at each exact resonance, a 6 dB hump has been accounted for the 75  $\Omega$  impedance of a tuned dipole. Results are given in  $\text{dB}\mu\text{V}/\text{m}$  for one  $\mu\text{V}$  (0  $\text{dB}\mu\text{V}$ ) of CM excitation.

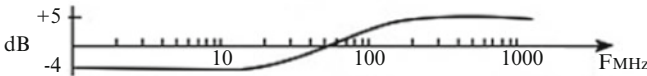
Notice that for the 1 m test distance, the length of the longest effective dipole has been limited to 1 m. This is to prevent an overprediction of the field amplitude, since the farthest segments of the radiating wire would be at a distance greater than 1 m from the receiving antenna.

**Example 2.6** Taking the same equipment as Example 2.5, assume that the 5 MHz CM current is not known, but the harmonic #9 CM driving voltage is 100 mV. This voltage may have been measured vs. chassis by a voltage probe directly at the I/O connector. We will extrapolate from the curve for a 2 m dipole (equivalent to 1 m monopole) at 45 MHz.





**Average correction for reflecting ground D = 3 m,  
cable height ≈ 0.80 m**



**Fig. 2.14** E-field radiation at 1 and 3 m distance from voltage-driven, open wires. Field given for 0 dBμV of CM drive. Peak fields horizontal locus correspond to odd multiples of λ/2

**Solution**

Test distance 3 m, frequency:	45 MHz
1. $E_0$ for 2 m dipole and 0 dBμV (Fig. 2.14)	-23 dBμV/m
2. Length correction* $20 \log (1.20/1)^2$	+3
3. Amplitude correction ( $10^5 \mu V$ )	+100
$E = 1) +2) +3)$ :	80 dBμV/m (40 dB above Class B)
*For a voltage-driven wire and below resonance, radiation efficiency increases like the square of length (relates to equivalent radiating area).	

We see that with approximately the same CM current, the field is approximately twice as large than with a closed loop, 0.30 m above ground. This can be considered as the upper bound for a CM-driven cable infinitely far from ground. Notice how little voltage it takes to excite an open wire above the radiated limit.

#### 2.5.2.4 Influence of a Nearby Ground Plane

If there is a conductive plane near the cable, this proximity causes a reflected wave with a phase shift (see Fig. 2.15). If the plane is sufficiently close, this shift is always at phase reversal with the directly radiated wave, and the total field equals  $E_0 - E_r$ . It is not necessary that the source or load be referenced to this plane, but the plane must be quasi-infinite. In practice, it must extend far enough around the cable projection and farther than the cable-to-antenna distance.

The radiation reduction, for  $h < 0.1\lambda$  (i.e.,  $h(m) < 30/F_{\text{MHz}}$ ), is

$$\frac{E_{\text{total}}}{E_0} = \frac{h}{0.1\lambda} \text{ or } \frac{10h}{\lambda} \quad (2.29)$$

Entering this factor into Equ. (2.27), for far field:

$$E_{\mu(\text{V/m})} = \frac{0.021 \times I_{\mu\text{A}} \times \ell_m \times h_m \times F_{\text{MHz}}^2}{D_m} \quad (2.30)$$

If  $h(m)$  is  $> 30/F(\text{MHz})$ , the reflected field is alternatively additive or subtractive, and the field is not reduced but doubled at certain frequencies. Incidentally, Equ. (2.30) shows a similarity with loop radiation from a since  $E$  now also depends on the area  $\ell \times h$ , and  $F^2$ .

**Example 2.7** For the equipment of Example 2.5, recalculate the maximum acceptable value for CM current with the cable now located 5 cm from a ground plane. The criterion to meet is MIL-STD-461-RE102, at 1 m distance. At 45 MHz, the limit is 24 dB $\mu\text{V/m}$ . At 150 MHz, the limit is 30 dB $\mu\text{V/m}$ . We can accept the far-field assumption for both frequencies.

#### Solution

- At 45 MHz,  $\lambda = 6.6$  m, so the 1.20 m cable length is  $< \lambda/4$ . Since  $h$  is 0.05 m, it is  $< 30/F$ . Per (2.30) and remembering that we have a monopole,

$$E = 0.021 \times I(1.20\text{ m} \times 2) \times 0.05 \times 45^2 = 5 \times I = I \text{ dB}\mu\text{A} + 14 \text{ dB}$$

Therefore, for limit compliance, we must satisfy  $I = E_{\text{limit}} - 14 \text{ dB}$

$$I \leq 24 \text{ dB}\mu\text{V/m} - 14 \quad I \leq 11 \text{ dB}\mu\text{A}$$

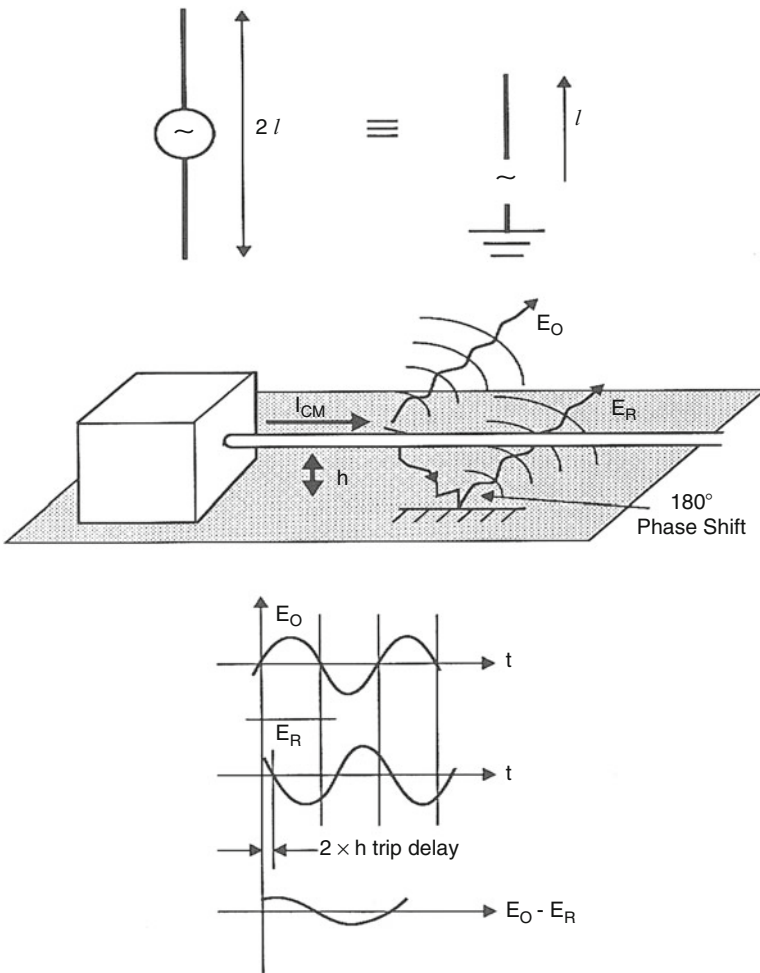
- At 150 MHz,  $\ell > \lambda/4$ , and  $h$  is still  $< 30/F$ . Equation (2.28) will be corrected by ground reflection factor  $h/0.1\lambda$  that we replace by  $h/(0.1 \times 300/F)$  or  $h F/30$

$$E = (60I/D) \times 0.05 \times 150/30$$

$$= 15I \text{ or } : I + 23.5 \text{ dB}$$

Therefore, the  $E$ -field limit translated into a CM current limit is  $I \leq E_{\text{limit}} - 23.5 \text{ dB}$

$$I \leq 30 \text{ dB}\mu\text{V/m} - 23.5 \text{ dB} \quad I \leq 6.5 \text{ dB}\mu\text{A}$$



**Fig. 2.15** Equivalent antenna for wire floated at both ends (dipole) or grounded at one end (monopole). Effect of a nearby ground plane for  $h < \lambda/10$

2.5.2.5 Ground Reflection with FCC/CISPR Tests

The reflected field addition on an *infinite ground plane*, practically doubling the value of  $E$ , is typical of FCC 15B or CISPR 22 emission testing. The equipment under test (EUT) and its cables are located above a ground plane, while the receiving antenna is cranked up and down to find the maximum level. A typical test configuration is the following:

- EUT + cables: 0.5–1 m above ground
- Test distance: 3 m
- Antenna set for vertical and horizontal polarization, with height scan 1–4 m

The corresponding correction for ( $E_{dirr.}, E_{refn}$ ) max. vs. free-space field is given below [3]

EUT height above ground	Horiz. polar.		Vert. polar.	
	0.5 m	1 m	0.5 m	1 m
$F_{MHz}$	Corr. $\Delta$ dB		Correction $\Delta$ dB	
30	+5	+4	-8	-4
50	+5	+4	-5	-1
70	+5	+3	-2	+2
100	+4	+2	0	+4
150	+3.5	0	+3	+5
200	+3		+4	+5

Below 100 MHz, the strongest reflection is detected with horizontally polarized sources (seldom the case with CM-excited cables), typical of DM sources inside the EUT. Above 100 MHz, the additive reflections are caused by vertically polarized sources, adding a maximum of 5 dB to the theoretical free-space value. We therefore can retain, as a reasonable worst case for all FCC- or CISPR-like measurements, a +5 dB ground reflection addition in our emission calculations.

As a concluding remark, Fig. 2.16 is showing the respective field contributions of PCB vs. external cables in two situations. The first plot, at top, corresponds to a PCB with 30 MHz clock circuit, attached to a 1.5 m external cable carrying typical spurious contents. As explained in this section, the cable CM radiation dominates the PCB DM contribution by 25–30 dB and is the sole violator of FCC/CISPR limit. In the bottom plot, the same geometry with a 150 MHz PCB shows a different split. Above 100 MHz, the spurious spectrum carried by the cable starts decreasing because:

- The maximum possible crosstalk coefficient in the PCB has been reached.
- Cable starts exhibiting HF losses.
- Around these frequencies, the cable radiating efficiency for 1.2-1.5 m lengths has reached its maximum.

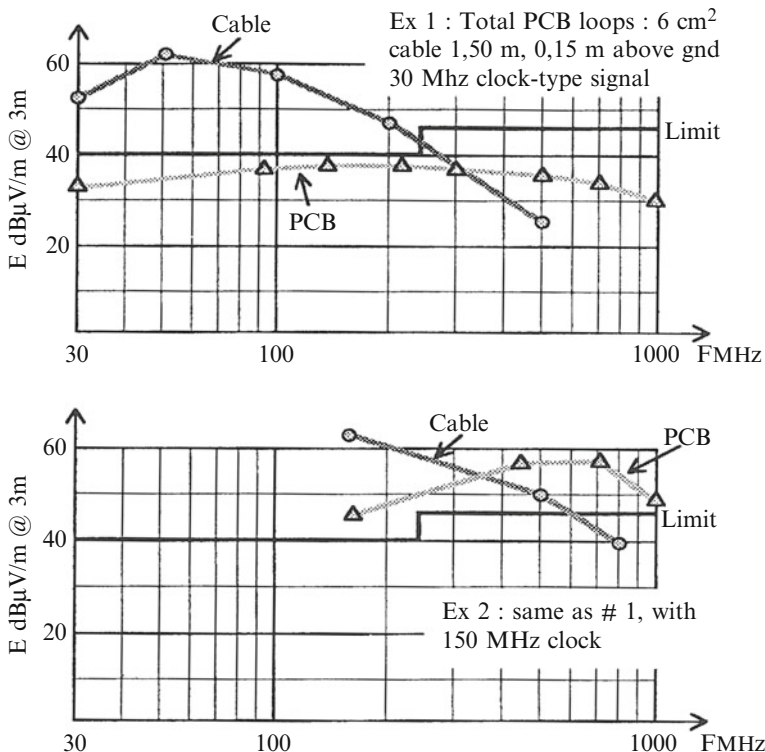


Fig. 2.16 Comparison of PCB vs. cable contribution to radiated spectrum

### 2.5.3 Radiation from a Long Wire

The distance restriction imposed for using the loop model or the wire models (i.e.,  $l < D$ ) rapidly becomes an obstacle to calculations in many configurations where cable lengths exceed a few meters. In this case, the physical length of the wire is such that it cannot be considered as a small element with respect to the observation distance. We can use a practical expression, taking into account the wide viewing angle from the observation point to the cable (infinite wire model):

$$H(A/m) = I(A)/2\pi D \tag{2.31}$$

Only the  $H$  field can be correctly determined by this Ampere’s law. An “equivalent”  $E$  field could be derived using a  $120 \pi\Omega$  wave impedance, but it would be inaccurate in this very near-field zone from such long antenna. Equation (2.31) assumes the wire is far from a ground plane, with respect to observation distance (i.e., in practice,  $h \gg D$ ). If the wire is close to a ground plane and the observation point is at the same height,  $h \ll D$ :

$$H \approx \frac{I}{2\pi D} \left( 1 - \cos \frac{2h}{D} \right) \quad (2.32)$$

This formula is valid for low frequency, a condition being that the phase shift due to the offset  $h$  be totally negligible. Notice that for small values of  $2h/d$ , cosine is approaching 1 and the  $H$  field tends to zero.

The criterion for deciding when a wire has to be considered to be “long” in comparison to  $D$  is simple: the maximum field is reached when  $\ell \geq \pi D$ . If one takes  $\ell > D$  as criteria, the error would be only 16% (1.3 dB). This is because a length increase from  $\ell = D$  to  $\ell = \pi D$  corresponds only to an argument viewing angle variation from  $\cos \alpha = 0.84$  to  $\cos \alpha = 1$ .

#### *Case of the Long-Wire Pair (DM Radiation)*

The infinite wire equation, when transposed to a long-wire pair carrying equal and opposite currents, becomes

$$\begin{aligned} H(\text{A/m}) &= 0.16I [s/(D^2) - s^2/4] \\ &\approx 0.16I (s/D^2) \text{ for } D \gg s \end{aligned} \quad (2.33)$$

with:

$D$  = pair to receiver distance, measured from pair axis

$s$  = wires separation

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# Chapter 3

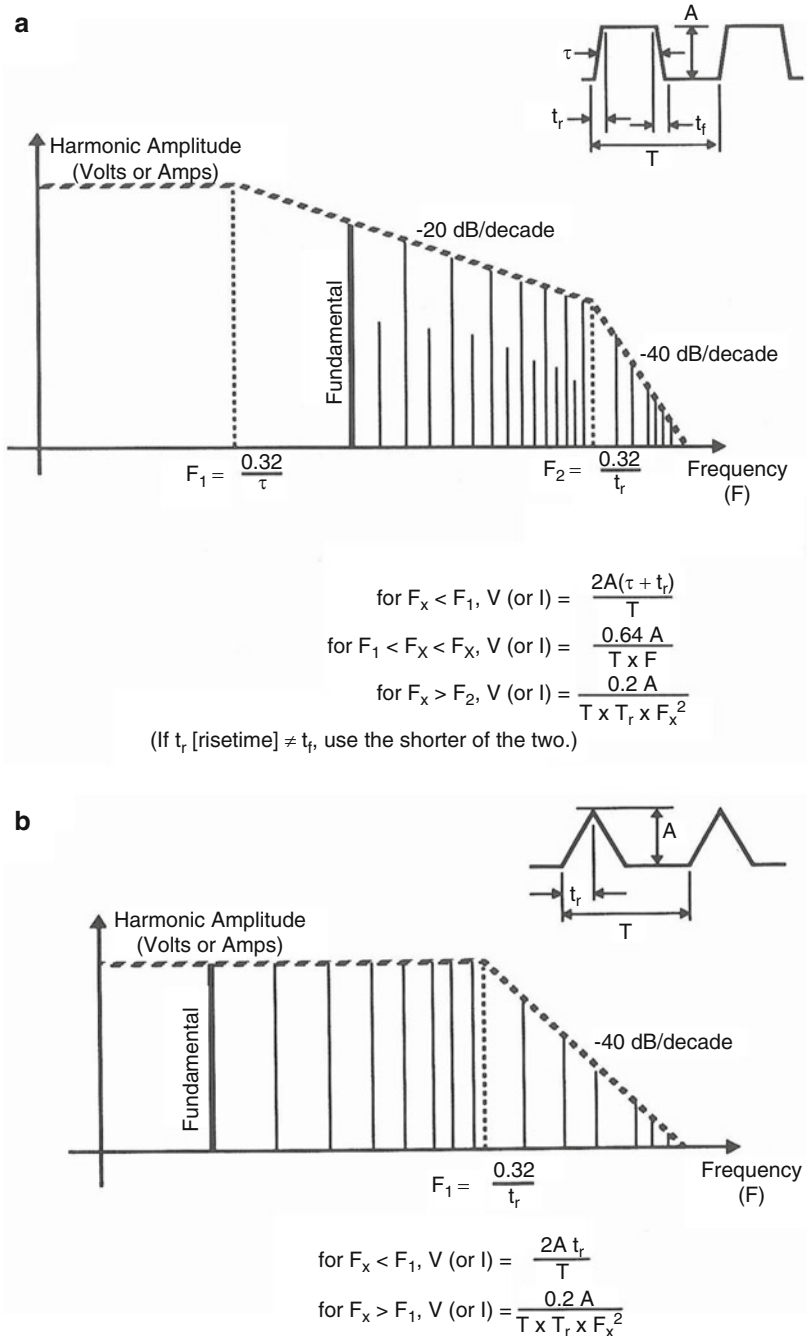
## Fields Radiated by Nonsinusoidal Sources

This chapter describes the two most common cases of nonsinusoidal sources: periodic signals with narrowband (NB) spectrum and periodic signals with broadband (BB) spectrum. The simplified equations briefly described in Chap. 2 can be extrapolated to the majority of practical cases where the excitation signal is not a pure sine wave but a repetitive signal with a known period and waveform. In both cases, the prediction process consists of first performing a Fourier analysis of the source signal, then treating each harmonic (or group of harmonics in a given bandwidth) as a sine wave for calculating radiation.

### 3.1 FREQUENCY SPECTRUM AND RADIATION FROM PERIODIC PULSES

Fourier theory states that a periodic signal can be expressed as a series of sine and cosine signals, at frequencies that are multiple integers of the pulse period. On the other hand, the standard emission limits typically range from 10 kHz to 10 or 40 GHz for military applications and 30 MHz to 1 or 10 GHz for most civilian ones. Thus, if one were to take a periodic signal and perform a rigorous Fourier computation, thousands or more discrete terms would have to be sorted out.

Instead, we will use the Fourier envelope method for voltages or currents. Figure 3.1a, b shows the Fourier envelope shapes and equations, corresponding to a few typical waveforms, as they would appear on an oscilloscope with a sufficient bandwidth. To make sure that the oscilloscope does not significantly distort the rise times, use an oscilloscope bandwidth (BW) (MHz) greater than  $350/t_r(\text{ns})$ , with  $t_r$  representing the fastest rise time of the observed pulse, measured in nanoseconds. The Fourier envelope is the locus of the maximum harmonics, without considering their phase. To draw this envelope, we must know:



**Fig. 3.1** (a) Fourier envelopes for narrowband spectrum, trapezoidal pulse train (any duty cycle). (b) Fourier envelopes for narrowband spectral amplitudes, symmetrical (isosceles) triangular pulses



- The peak amplitude,  $A$  (volts, amperes, etc.).
- The pulse width,  $\tau$ .
- The period,  $T$ , where the signal reproduces itself.
- The rise time,  $t_r$ , at 10-90% crossings. If fall and rise times are different, select the shorter of the two for  $t_r$ .

For a periodic signal, the frequency spectrum is composed of a series of discrete sine wave harmonics, consisting of the fundamental ( $F_0 = 1/T$ ) and integer multiples of  $F_0$ .

Besides the fundamental,  $F_0$ , two key frequencies are needed in constructing the spectrum envelope:

$$F_1 = 1/\pi\tau$$

Above  $F_1$ , the locus of the maximum amplitudes rolls off with a  $1/F$  slope (-20 dB/decade), up to the second-corner frequency:

$$F_2 = 1/\pi t_r$$

Above  $F_2$ , the spectrum decreases abruptly, with a  $1/F^2$  slope (-40 dB/decade). Notice how critical this frequency is: the shorter the rise time, the higher the spectral occupancy. A nomogram has been constructed (Fig. 3.2) to provide easy and quick approximation of the spectral envelope. Once the envelope is drawn, the worst-case amplitude of any harmonic can be found.

**Example 3.1** Find the Fourier envelope of the signal in Fig. 3.3.

The first step consists in identifying the three frequency marks:

$$F_0 = 1/0.020\mu\text{s} = 50\text{MHz}$$

$$F_1 = 1/\pi\tau = 32\text{MHz}$$

$$F_2 = 1/\pi t_r = 160\text{MHz}$$

Notice that, at frequency  $F_1$ , such a pulse train, with a 50% cycle, has no frequency component, yet. However, we need  $F_1$  to construct the envelope. The starting amplitude for the reference line is

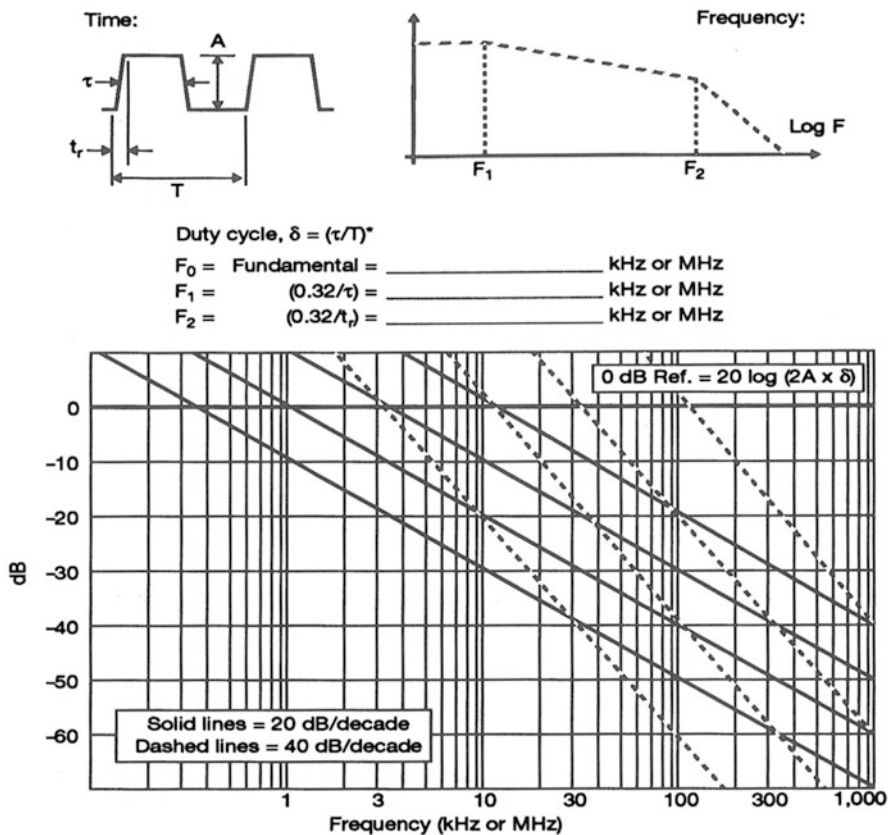
$$20 \log (2A\tau/T) = 20 \log (2 \times 3.2\text{V} \times 0.5) = 10\text{dBV}$$

The frequency  $F_1$  (32 MHz) is marked on top of the 0 dB reference line. Then, a -20 dB/decade slope is drawn, using the parallel grids, until  $F_2$  (160 MHz) is encountered. From this point, a -40 dB/decade slope is drawn. The amplitude of any harmonic, in dBV or dBamp, can be found by simply subtracting the slope decrease in dB, from the reference amplitude.

There is a small ringing of the waveform at the pulse edges due to a reflection mismatch (assuming it was not caused by the oscilloscope probe capture). This ringing of about 3% of amplitude is almost unnoticeable on an oscilloscope trace

but causes a 6 dB hump around 400 MHz on the frequency spectrum. The +6 dB corresponds to the normal harmonic amplitude of -20 dBV, adding to the ringing amplitude of 0.1 V peak (above the second-corner frequency, even harmonics tend to reach the same amplitude as odd ones, as explained further in Sect. 3.4.4). This is shown below in Table 3.1 for few typical harmonics.

To calculate the radiation from a circuit carrying such spectrum, we simply need to apply the equations or graphs for loop surface or wire length.



\*if  $\delta = 0.5$ , amplitude at  $F_0 = A - 4$  dB

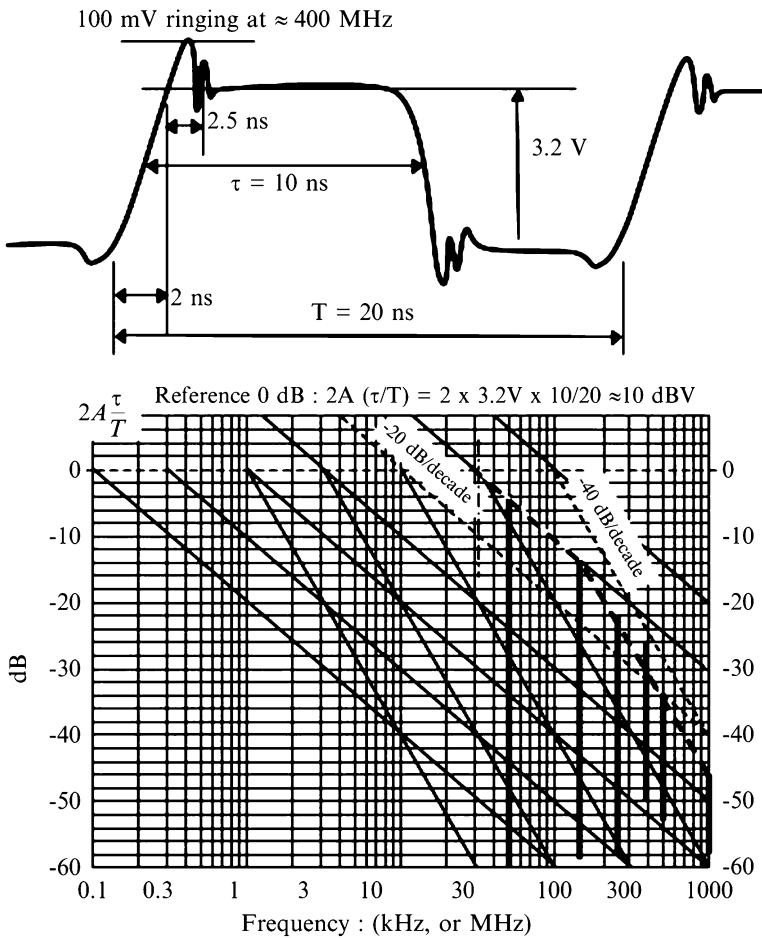
Harmonic #	Frequency	Ref. Amplitude (dB V or dB A)	Slope Decrease dB	Amplitude of Harmonic #

Fig. 3.2 Template for quick frequency spectrum plot

**Table 3.1** Amplitude calculation for Example 3.1

Harmonic #	Fundamental	# 3	# 5	# 7	# 8	# 10	# 20
Frequency (MHz)	50	150	250	350	400	500	1,000
Ref. amplitude (dBV)	10	10	10	10	10	10	10
Slope decrease (dB)	-4	-14	-22	-28	-30	-34	-46
Actual amplitude (dBV)	6	-4	-12	-18	-20	-24	-36
					+6*		

\*Parasitic edge resonance



**Fig. 3.3** Signal from Example 3.1 in time and frequency domains, showing envelope and a few spot frequencies

**Example 3.2** The clock pulse train of Example 3.1 is distributed to several daughter cards via the motherboard of Fig. 3.4. The equipment is a mass-produced, large consumer appliance with severe cost constraints. The board is a double-sided single layer, with ground plane on one side.

The critical radiating circuit has the following characteristics:

- Eight clock runs with ground plane return
- Clock trace height above Gnd plane = 0.16 cm
- Trace length,  $\ell = 12.5$  cm
- Terminal resistance at line end = 200  $\Omega$
- Approximate line characteristic impedance,  $Z_0 = 100 \Omega$  (to use above  $\lambda/4$ )

Calculate the field strength at 3 m against FCC Class B limits. The measuring bandwidth for this test is 120 kHz, so each harmonic is seen one at a time (narrowband situation).

**Solution** Using the curves of Fig. 2.6, we will apply the following corrections:

Voltage correction: from Table 3.1

Area correction:  $20 \log (12.5 \times 0.16 \text{ cm}) = +6$  dB

Number of synchronous loops:  $20 \log N = 18$  dB

(Viewed from 3 m, the eight loops radiate approximately as a single one with eight times more current or eight times the area.)

The quarter wavelength limitation (see Sect. 2.4) for current distribution on PCB traces is reached when  $\ell = 5,000 \text{ cm}/F(\text{MHz})$  (i.e., here, 400 MHz for  $\ell = 12.5$  cm). Above this frequency,  $\ell$  is replaced by  $5,000/F$  in the area correction. Beyond this point, each harmonic will drive a gradually diminishing effective area: the efficiency of the “antenna” decreases, as does the voltage spectrum. As a result, the total radiation profile collapses. At the same time, the load resistance of 200  $\Omega$  will be replaced by the 100  $\Omega$  characteristic impedance of the line.

Calculations are detailed in Table 3.2. Line #1 in the table is simply reusing the results of Table 3.1, last line.

**Table 3.2** Calculation steps for Example 3.2

$F$ (MHz)	50	150	250	350	400	500	1,000
1. Actual amplitude (dBV)	6	-4	-12	-18	-20	-24	-36
2. $E_0$ ( $1 \text{ V} \times 1 \text{ cm}^2$ ) (dB $\mu$ V/m) for $Z = 200 \Omega$ , $Z = 100 \Omega$	14	34	42	46	56	60	72
3. Area correction (dBcm $^2$ )	+6	+6	+6	+6	+6	+4	-2
4. Number of synchronous loops ( $20 \log N$ )	+18	+18	+18	+18	+18	+18	+18
Total field (dB $\mu$ V/m): 1 + 2 + 3 + 4	44	54	54	58	66	58	52
Limit: FCC Class B (dB $\mu$ V/m)	40	43	46	46	46	46	46
Off-spec. (dB)	<b>4</b>	<b>11</b>	<b>+8</b>	<b>+12</b>	<b>+20</b>	<b>+12</b>	<b>+6</b>

\*Parasitic edge resonance

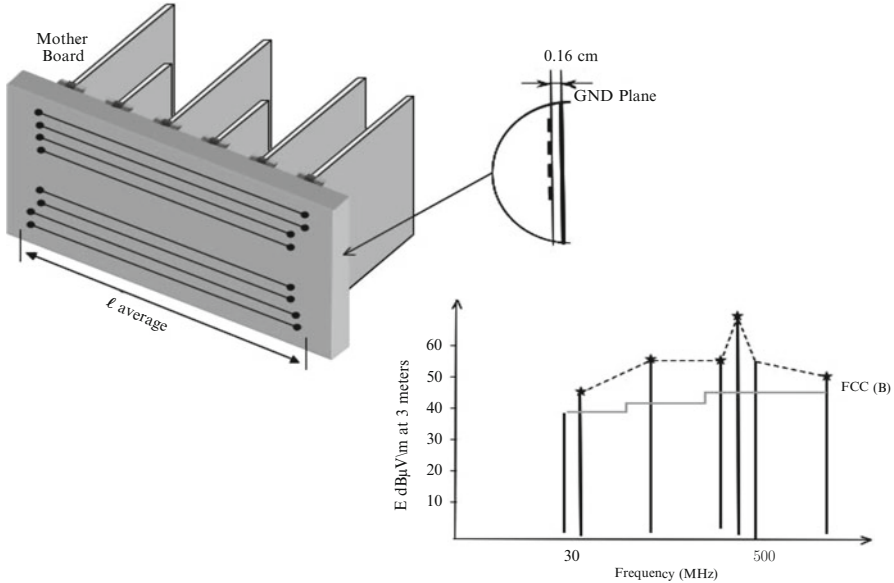


Fig. 3.4 Motherboard of application Example 3.2

The FCC limit, accounting for no shielding at all from the box and covers, is violated by 11-20 dB up to 500 MHz. Some action has to be taken, e.g., reducing the loop size (adding ground traces closer to the clock traces) or shielding the box. For the sake of precision, it should be remarked that:

1. The Fourier series gives peak values for each harmonic, while EMI receivers are scaled in rms terms, so we can expect a +3 dB prediction error (pessimistic).
2. The FCC and CISPR procedures call for scanning the height with the antenna to search for maximum readings, which typically causes up to 5 dB increase at frequencies where the ground-reflected wave come in phase addition (see Sect. 2.5.2.5).
3. The model assumes lossless propagation in cables and circuit traces. In reality, line losses start becoming significant above 200-300 MHz in meter-long circuits. This causes an increase in rise times, making the signal spectrum roll off at 40 dB/decade sooner than calculated. On the other hand, the model takes into account that  $\lambda/4$  resonance is reached about 0.7 times earlier.

The opposite effects of items (1) and (2) can be handled as follows: the -3 dB correction for peak-to-rms adjustment is almost offset by the +3 to 5 dB ground reflection of the test setup (see Chap. 2), such as in all our subsequent calculation examples, *we will simply disregard these two corrections, as being a wash-out*. If one wants to perform more exact predictions (knowing that actual measurement uncertainty will cause a greater error), he/she can still use the actual corrections.

### 3.2 SPECTRUM AND RADIATION FROM BROADBAND SOURCES

The previous narrowband (NB) analysis that examines one harmonic at a time is inapplicable when the radiating circuit is carrying signals with a BB spectrum (i.e., signals whose frequency harmonics are closely staggered in the Fourier spectrum). This is especially true when the repetition frequency is lower than the receiving instrument (or victim) bandwidth. The same periodic waveform as in Fig. 3.1 can be displayed by its spectral density (see Fig. 3.5). The starting voltage amplitude is

$$V(\text{dBV}/\text{MHz}) = 20 \log 2A\tau \quad (3.1)$$

All the same, the current spectral density is derived from the circuit impedance  $Z_c(f)$  at the frequency of interest:

$$I(\text{dBA}/\text{MHz}) = \text{dB}(V/\text{MHz}) - 20 \log Z_c(\Omega) \quad (3.2)$$

For a trapezoidal pulse (Fig. 3.5, caption “a”), at any frequency  $F_x$  across the spectrum, the BB voltage in a unity bandwidth of 1 MHz will be equal to:

**For  $F_x < 1/\pi\tau$ :**

$$V(V/\text{MHz}) = 2A \times \tau \text{ or } V(\text{dBV}/\text{MHz}) = 20 \log (A\tau) + 6$$

**For  $1/\pi\tau < F_x < 1/\pi t_r$ :**

$$V(\text{dBV}/\text{MHz}) = 20 \log A - 4 - 20 \log F_x(\text{MHz})$$

**For  $F_x > 1/\pi t_r$ :**

$$V(\text{dBV}/\text{MHz}) = 20 \log A.t_r - 14 - 40 \log F_x(\text{MHz})$$

with

$V$  = voltage amplitude in time domain

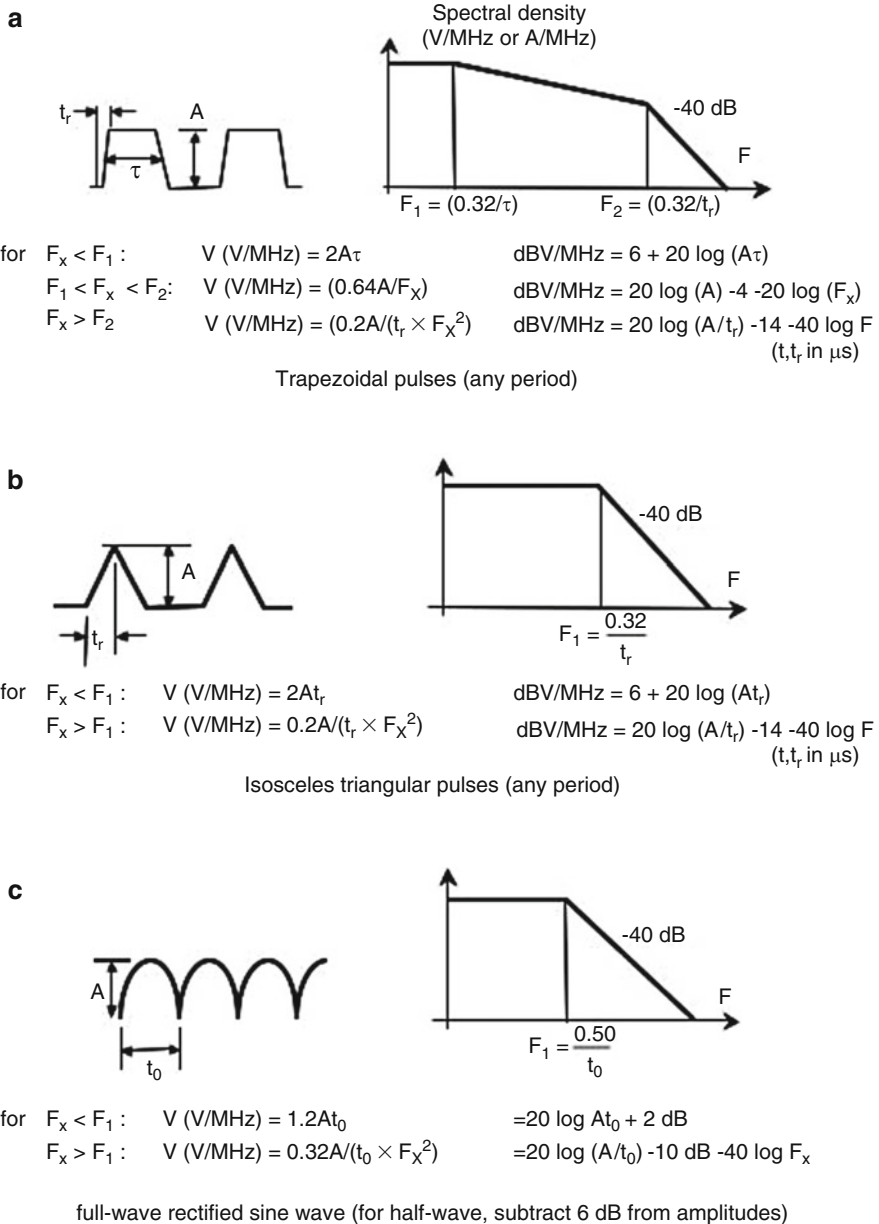
$\tau$  = 50% pulse width in microseconds

$t_r$  = rise/fall time in microseconds

If the results are desired in a bandwidth  $B_x$  different from 1 MHz, use  $20 \log B_x$  (MHz) for correction. Then, the calculation steps are similar to a narrowband excitation, except that the resulting field will be expressed in  $\text{dB}\mu\text{V}/\text{m}/\text{MHz}$ .

Since the majority of EMI emissions specifications have abandoned the principle of double BB and NB limits (see Chap. 1, Sect. 1.4), calculating the amplitude of a BB type of interference seems an antiquated, useless chore. However, although the double limit is often obsolete, it is still applied in specific standards, like CISPR 25 for vehicle applications. But furthermore, although not clearly stated, BB

interference is implicitly addressed in most civilian/military EMI standards via the required measurement bandwidths. For instance, typical emission tests stipulate a 9 or 10 kHz receiver BW for the 0.15-30 MHz frequency band and 100 or 120 kHz BW for the 30–1,000 MHz range.



**Fig. 3.5** Fourier envelopes for broadband spectral amplitudes. Notice that spectral density is independent of pulse repetition rate and remains true for a single pulse (Fourier integral)

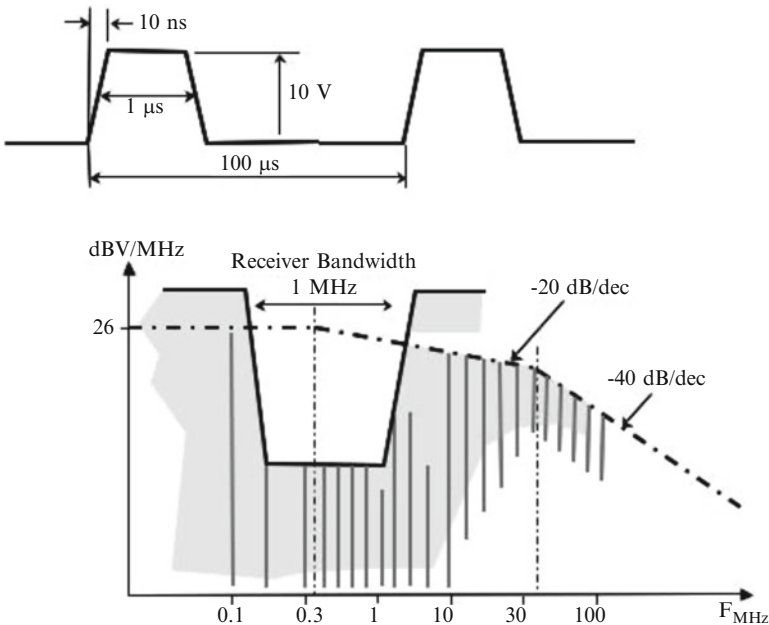
Accordingly, a switch-mode power supply with 30 kHz switch rate will appear as a NB source in a 10 kHz BW (below 30 MHz), but a BB source in a 120 kHz BW, with three or four harmonics adding up in the receiver window. In fact, most specifications give several limits for a same measurement, depending upon the type of detection used: peak, average, or quasi-peak. This is nothing else than addressing, without saying, the possibility of a mixed NB/BB content in the measured spectrum.

Before applying a BB analysis, one should always check that measurement conditions are actually broadband, that is, pulse repetition frequency < receiver bandwidth.

**Example 3.3** Consider the train of triggering pulses in Fig. 3.6. This pulse train is carried over two parallel wires on a flat ribbon cable, with

$$\ell = 1 \text{ m} \quad s = 0.5 \text{ cm}$$

Circuit load impedance is matched to  $100 \Omega$ . The cable is installed at 5 cm over a ground plane and terminates onto a small plastic keypad, isolated from ground, with a stray capacitance of 10 pF.



**Fig. 3.6** Time and frequency view of pulse train with low-duty cycle, from Example 3.3



**Part a)** Calculate the radiated BB field due to the DM and CM radiation, against RE02 BB limit of MIL-STD 461C (Air Force and Navy) at 1 m and few specific frequencies. Although the 461C is an old version, it is interesting to run a numerical application for a fully BB situation.

Calculation of key elements:

$$F_0 = 10 \text{ kHz}$$

$$F_1 = 1/\pi\tau = 320 \text{ kHz}$$

$$F_2 = 1/\pi t_r = 32 \text{ MHz}$$

Spectral density at spectrum start:  $2A \times \tau = 2 \times 30 \text{ V} \times 1 \mu\text{s} = 60 \text{ V/MHz}$   
 $= 36 \text{ dBV/MHz}$

Area corrections:

$$\text{DM loop} = 100 \text{ cm} \times 0.5 \text{ cm} = 50 \text{ cm}^2 = 34 \text{ dBcm}^2$$

$$\text{CM loop} = 100 \text{ cm} \times 5 \text{ cm} = 500 \text{ cm}^2 = 54 \text{ dBcm}^2$$

For DM radiation, the line is a symmetrical pair, behaving as a folded dipole. Resonance occurs when each 1 m arm of the dipole reaches  $\lambda/4$ , that is 75 MHz. Beyond this frequency, the effective radiating length will decrease as frequency increases as follows:

$$F = 150 \text{ MHz}, \quad \lambda/4 = 50 \text{ cm}$$

$$F = 300 \text{ MHz}, \quad \lambda/4 = 25 \text{ cm}$$

For CM radiation, the line consists of two wires above ground, i.e., most of the propagation media is air, not a dielectric. The propagation velocity can be taken as that of free space. So, for a monopole with  $\ell = 1 \text{ m}$ , the  $\lambda/4$  length clamp occurs when

$$\ell \text{ m} = 0.25(300/F) = 75/F, \quad \text{hence } F = 75 \text{ MHz}$$

At some selected frequencies, the CM loop impedance (open wire) will be:

$$\text{For } 10 \text{ MHz}, \quad Z_{\text{cm}} = 1/C\omega = 1/(10 \cdot 10^{-12} \times 2\pi \times 10^7) = 1.5 \text{ k}\Omega$$

$$\text{For } 30 \text{ MHz}, \quad Z_{\text{cm}} = 500 \Omega$$

Above 75 MHz,  $Z_{\text{cm}}$  will be replaced by the characteristic impedance of this cable above ground, i.e.,  $\approx 200 \Omega$ .

Table 3.3 shows the calculation steps for DM radiation. BB limit is satisfied with at least a 10 dB margin at 10 MHz and beyond. Table 3.4 shows similar calculations, but for CM radiation. We apply the loop equation, using the capacitive impedance (yet, entering in the far-field region, the loop load impedance is clamped

to a maximum value of 377  $\Omega$ ). Notice that the drive voltage for the CM loop is derived from the DM/CM conversion ratio, with -10 dB being the default value for a non-balanced, wire pair link (see Chap. 2 Sect. 2.5). It translates the differential drive voltage into an equivalent longitudinal source driving the CM loop.

Finally, profiles of the DM and CM radiated levels are shown in Fig. 3.7. Because of the CM contribution, the BB limit is exceeded up to 10 MHz, and the margin is small up to 150 MHz. In near-field conditions (for  $F = 1\text{-}10$  MHz), the ref. field  $E_0$  in the table can be read from Fig. 2.6 or calculated by Equ. (2.17a), since  $Z_c > 7.9 \times D \times F(\text{MHz})$ .

**Table 3.3** Calculation steps for DM radiation

$F$ (MHz)	1	10	30	150	300
Reference amplitude (dBV/MHz)	36	36	36	36	36
Slope decrease (dB)	-10	-30	-40	-68	-80
1. Actual amplitude (dBV/MHz)	26	6	-6	-32	-44
2. $E_0$ ( $1 \text{ V} \times 1 \text{ cm}^2$ ) (dB $\mu$ V/m) at 1 m for $Z = 100 \Omega$	18	18	26	50	62
3. Area correction (dBcm $^2$ )	+34	+34	+34	+28*	+22*
Field (DM) (dB $\mu$ V/m): 1 + 2 + 3	78	58	54	46	40
Spec. RE-102 (dB $\mu$ V/MHz)	80	68	64	55	58

\*These frequencies are beyond quarter wave length resonance: effective area ( $\ell \times s$ ) is replaced by  $[(\lambda/4) \times s]$

**Table 3.4** Calculation steps for CM radiation (the BB limit is exceeded up to 10 MHz)

$F$ (MHz)	1	10	30	150	300
1. Actual DM amplitude (dBV/MHz)	26	6	-6	-32	-44
2. DM-to-CM conversion (dB)	-10	-10	-10	-10	-10
Z loop (CM)	15 k $\Omega$	1.5 k $\Omega$	500 $\Omega$	200 $\Omega$	200 $\Omega$
3. $E_0$ ( $1 \text{ V} \times 1 \text{ cm}^2$ ) (dB $\mu$ V/m) at 1 m for Z loop (CM)	18	18	18	44	56
4. Area correction (dBcm $^2$ )	+54	+54	+54	+48*	42*
Field (CM) (dB $\mu$ V/m): 1 + 2 + 3 + 4	88	68	56	50	44
Spec. RE-102 (dB $\mu$ V/MHz)	80	68	64	55	80

\*These frequencies are beyond quarter wave length resonance: effective area ( $\ell \times s$ ) is replaced by  $[(\lambda/4) \times s]$

**Part b)** Repeat example for compliance to MIL-STD-461D or  $E$  and limit RE102.

Starting Rev. D, the MIL-STD-461 has abandoned the NB/BB discrimination, requiring emission tests with preassigned BW as follows:

$$\begin{aligned} 0.150 - 30 \text{ MHz} &: \text{BW} = 10 \text{ kHz} \\ 30 - 1,000 \text{ MHz} &: \text{BW} = 100 \text{ kHz} \end{aligned}$$

We must first perform a check for the pulse repetition frequency vs. receiver BW. The pulse train of Fig. 3.6 has a 100 μs period, hence a 10 kHz rep. rate. Therefore,

- For frequencies <30 MHz: only one harmonic at a time will be seen in the receiver BW. Interference will appear as NB.
- For frequencies >30 MHz: up to ten harmonics at a time will add up in the receiver BW. Interference will appear as BB.

This is reflected in Tables 3.5 and 3.6 and Fig. 3.7 where the new RE102 bandwidths and spec. limit are used, with the associated limit violations. The CM contribution is still the highest, but the ΔdB off-spec. is totally different from the ones in Tables 3.3 and 3.4 with the old RE02. We notice that if the 10 kHz BW had been used for the 30 MHz measurement, the emission would have been below limit. The changeover to 100 kHz BW has caused a +20 dB aggravation. The lower plot in Fig. 3.7 has been computed as the coherent addition of DM and CM contributions, since they both exist.

**Table 3.5** Calculation steps (DM) for Example 3.3 part b

<i>F</i> (MHz)	1	10	30	150	300
Reference amplitude NB: $2A\tau T$ (dBV)	-14	-14			
BB: $2A\tau$ (dBV/MHz)	x x x x x	x x x x x x	26	26	26
Slope decrease (dB)	-10	-30	-40	-68	-80
BW factor correct. (dB) $20 \log 0.1/1$ MHz	x x x x x	x x x x x	-20	-20	-20
1. Actual DM amplitude: NB(dBV)	-24	-44			
BB (dBV in 100 kHz BW)			-34	-62	-74
2. $E_0$ ( $1 \text{ V} \times 1 \text{ cm}^2$ ) (dBμV/m) at 1 m for $Z = 100 \Omega$	18	18	26	50	62
3. Area correction (dBcm <sup>2</sup> )	+34	+34	+34	+28*	+22*
Field (DM) (dBμV/m): 1 + 2 + 3	<b>28</b>	<b>8</b>	<b>26</b>	<b>16</b>	<b>10</b>
MIL-STD-461-RE102 (dBμV/m) (most severe class)	30	24	24	28	34
Off-spec. (dB)	OK	OK	+2	OK	OK

\*These frequencies are beyond  $\lambda/4$  resonance. ( $\ell \times s$ ) is replaced by  $[(\lambda/4) \times s]$

**Table 3.6** Calculation steps for CM radiation

<i>F</i> (MHz)	1	10	30	150	300
1. Actual DM amplitude: NB (dBV)	-24	-44			
BB (dBV in 100 kHz BW)			-34	-62	-74
2. DM-to-CM conversion (dB)	-10	-10	-10	-10	-10
Z loop (CM)	15 kΩ	1.5 kΩ	500 Ω	200 Ω	200 Ω
3. $E_0$ ( $1 \text{ V} \times 1 \text{ cm}^2$ ) (dBμV/m) at 1 m for Z loop (CM)	18	18	18	44	56
4. Area correction (dBcm <sup>2</sup> )	+54	+54	+54	+48*	42*
Field (DM) (dBμV/m): 1 + 2 + 3 + 4	<b>38</b>	<b>18</b>	<b>28</b>	<b>20</b>	<b>14</b>
MIL-STD-461-RE102 (dBμV/m) (most severe class)	30	24	24	28	34
Off-spec. (dB)	+8	OK	+4	OK	OK

\*These frequencies are beyond quarter wave length resonance: effective area ( $\ell \times s$ ) is replaced by  $[(\lambda/4) \times s]$

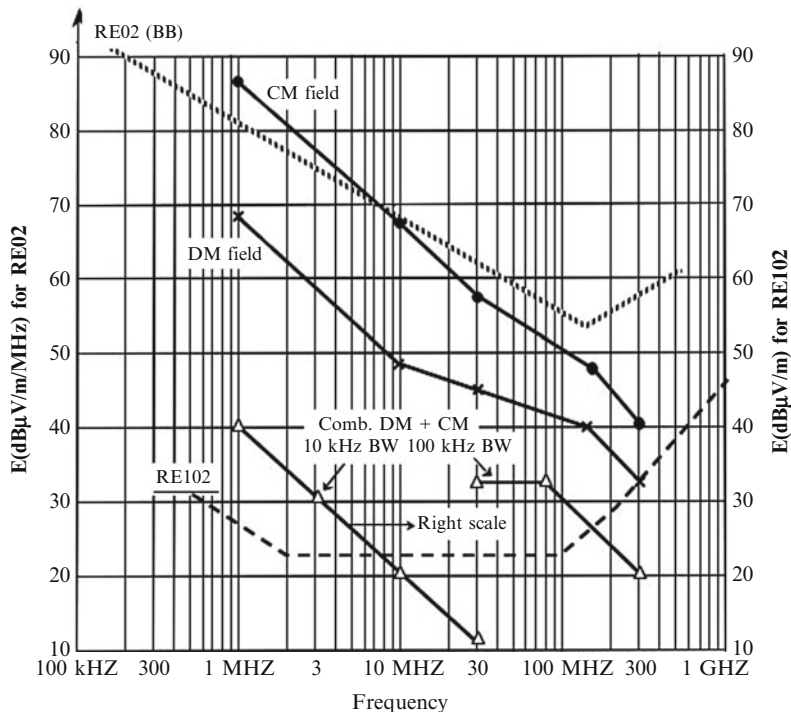


Fig. 3.7 Profiles of DM and CM radiation, from Example 3.3

### 3.3 RANDOM VS. PERIODIC SPECTRA

Whenever there are stable frequency devices in an equipment, test results invariably show that the NB and coherent BB components (those with a stable repetition frequency) are the dominant signatures in the measured spectrum. Although other noise components are found in a radiated spectrum, the BB field from diode noise, motor brushes, fluorescent tubes, ignition, and so forth is generally inferior, when measured in a bandwidth-limited receiver.

As a result, when a radiated limit is exceeded by a device containing digital circuits (today, it is hard to find a device which does not), the major violators are the clock harmonics. For instance, in the actual test results of a digital circuit (see Fig. 3.8), the clock signal being a perfectly stable, frequency-locked pulse train generates a coherent spectrum. In contrast, the digital signals have durations which constantly vary depending on the transmitted message, producing only a non-coherent spectrum with no stable harmonics. Therefore, it is the clock harmonics, switching power supply harmonics, and the like that will dominate the radiated profile. Because of this, clock circuits on PCBs, motherboards, and cables should be treated very carefully, as will be described further on.

However, with the growing EMC awareness in PCB design teams, clock circuits and their PCB traces are given more and more attention, while at the same time, high-speed parallel busses with frequencies of 50 or 100 MHz are commonly used, as well as serial busses with 500 MHz or even a few GHz. The result is that fast digital equipments may show limit violations not only by their clock harmonics, but also by the BB contents (generally random), of their address/data busses, as described hereafter in Sect. 3.4.1.

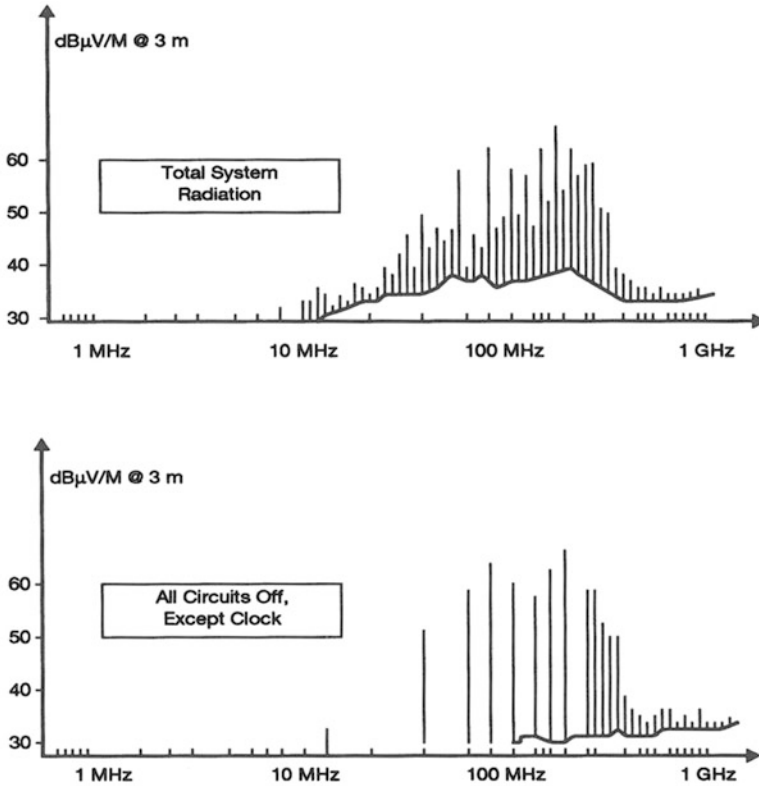


Fig. 3.8 Periodic vs. random radiated signatures

### 3.4 PECULIAR ASPECTS OF SOME FREQUENCY SPECTRA

Certain pulse trains produce Fourier spectra which are not as simple as the immaculate 50% duty cycle clock of our former examples. However, provided a few adjustments are made, they can be treated by the same straightforward envelope method.

### 3.4.1 Random Signals with Narrowband Contents

NRZ (non-return to zero) digital signals, although they are synchronized with a fixed clock rate, exhibit constantly varying duty cycle depending on each byte content. In theory, they can only create a random type of BB spectrum, whose average spectral density is proportional to the square root of receiver bandwidth (10 log BW), instead of 20 log BW as in coherent BB (see Sect. 3.2). However, even random pulse trains often contain repetitive patterns which are causing some NB contents. Examples of possible NB contents buried in a BB random spectrum are [2]:

- The least significant bit (LSB) lines on a parallel bus, whose state is almost constantly toggled at the clock rate or submultiples of it.
- The logic circuits using RZ (return to zero) Manchester or similar codings.
- Certain signaling codes (for instance, in ISDN) with an alternating mark-space pattern.
- Clock recovery in data transmission.
- Certain cyclic software sequences.
- “Transparency” of ASIC and  $\mu$ P cells to clock activity inside the chip.

This BB + NB combination appears as a random pulse modulation of discrete harmonics in the emitted spectrum. With typical  $\mu$ Processor address or data bus, this can be estimated on a probabilistic basis, by some worst-case assumption of the data stream. Based on the probable spectral density, Fig. 3.9 shows the amplitude of a BB spectrum of random NRZ pulse train with 10 and 100 Mb rates, when received in a 120 kHz bandwidth. Compared to the original spectrum of a clock with the same rate, we see that clock residue (NB) will emerge from an otherwise BB spectrum if their amplitude is  $\Delta$ dB or less below the original clock spectrum.

This can be restated as follows: if PCB traces, ribbon cables, etc. are polluted by clock residue, these can be examined as prime candidates to specification violation if their amplitude is greater than [original clock spectrum - $\Delta$ dB].

The  $\Delta$  term depends on the ratio of the clock pulse width compared to the elementary data bit width, and the measuring receiver bandwidth. For instance, in Fig. 3.9,  $\Delta$  is 30 dB for the 10 MHz/10 Mb case, and 50 dB for the 100 MHz/100 Mb case. If the clock has been extremely well segregated and filtered from the rest of the circuits, with a decoupling greater than  $\Delta$ , the BB spectrum sources can be examined as the next potential candidates. The two are not mutually exclusive.

**Example 3.4** Calculate the BB voltage spectrum and the peak amplitude, in a 100 kHz bandwidth, for the following random NRZ pulse trains:

- (a) 10 Mb, 1 V; one-bit mean width,  $\tau = 50$  ns,  $t_r, t_f = 5$  ns
- (b) 100 Mb, 1 V; one-bit mean width,  $\tau = 5$  ns,  $t_r, t_f = 0.5$  ns

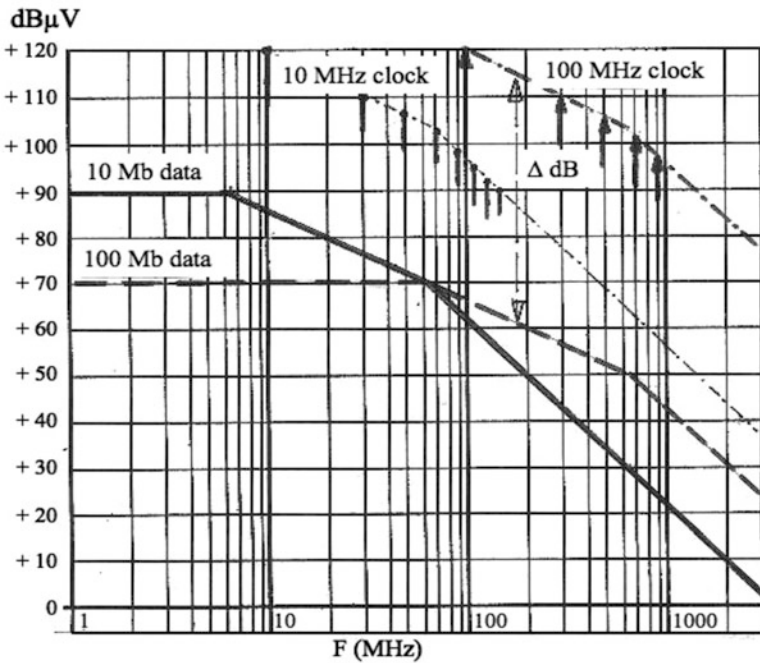
**Solutions**

Rep. rate	10 Mb	100 Mb
Mean spectral density		
$2A\tau(V/MHz)$	0.1 V	0.01 V
$dB\mu V/MHz$	100	80
First-corner frequency	6 MHz	60 MHz
Second-corner frequency	60 MHz	600 MHz

Peak amplitude, 100 kHz BW:

BW correction for random BB		
$10 \log (0.1/1 \text{ MHz})$	-10	-10
Amplitude up to 6 MHz	90 $dB\mu V$	70 $dB\mu V$
Amplitude at 60 MHz	70 $dB\mu V$	70 $dB\mu V$
Amplitude at 600 MHz	30 $dB\mu V$	50 $dB\mu V$

Therefore, with a 10 Mb transmission, clock residues carried by the message content will emerge from the emission spectrum if their measured voltage at I/O port exceed 72  $dB\mu V$  at 50 MHz (5th clock harmonic) or 54  $dB\mu V$  at 150 MHz (15th clock harmonic). For a 100 Mb transmission, the critical amplitude for the 100 MHz clock residues would be 52  $dB\mu V$  at 500 MHz and 34  $dB\mu V$  at 1,500 MHz.



**Fig. 3.9** Magnitude of the BB spectrum of 1 V random NRZ data with 10 and 100 Mb when measured in a 100 kHz BW. The discrete spectrum of V clocks with same frequencies is shown of comparison. Rise times are assumed 10% of elementary bit width

### 3.4.2 Repetitive Symbols Enhancing EMI Radiations

High-definition displays use pixel clock oscillators at 100 MHz or more, with video signal rise times  $< 2$  ns. This pixel frequency corresponds to the smallest picture segment, i.e., the elementary pixel duration:

$$\text{Pixel clock frequency} = \text{Number horiz.pixels} \times \text{Number vertical pixels} \\ \times \text{Refresh rate}$$

In some EMI analysis or testing, it is sometimes useful to force the highest symbol rate, i.e.,  $0.5 F_{\text{clock}}$ , corresponding to mark-space-mark-space, etc. In that respect, one of the busiest test patterns for displays is a full screen of “H” characters, generating a high level of discrete harmonics [3, 4].

### 3.4.3 Spread Spectrum Clocks (SSC) for Reduced EMI

An interesting concept was developed by Bush [1], whereas the digital processor clock, instead of a stable frequency, is using a frequency modulated clock, such as the actual spectrum occupancy for each one of the clock harmonics is over wider bandwidth. If the modulation is  $\Delta f$  on the fundamental, each consecutive  $n$ th spread harmonic is spread over a bandwidth  $\pm n \Delta f$  around the theoretical narrowband frequency. If  $\Delta f$  is chosen to be greater than the typical receiver bandwidth, the resulting net amplitude will be less than with an ordinary NB spectrum. The decrease in measured amplitude is approximately equal to  $\sqrt{n/2}$ , i.e.,  $10 \log n/2$ , or  $10 (\log n) - 3$  dB.

For example, with a FM deviation of 125 kHz and a 100 kHz EMI receiver bandwidth of the reduction brought by the spread spectrum for a 20 MHz clock (odd harmonics) is as follows:

Harmonic #	$\Delta$
3	-2 dB
5	-4 dB
9	-6.5 dB
etc.	

One key factor for the improvement is that the modulating signal is not a sine wave itself but a smoothed sawtooth whose time derivative at zero crossing is minimal. This technique has been applied on some processors of the Pentium and Celeron families.



### 3.4.4 Even vs. Odd harmonics when Duty Cycle is Not Exactly 0.5

The general expression for each spectral term of a trapezoidal pulse train is

$$A_N = A_0 [(\sin(n\pi\delta))/n\pi\delta] \times [(\sin(n\pi t_r/T))/(n\pi t_r/T)] \quad (3.3)$$

where  $A_0$  is the time-domain pulse amplitude.

(a) When  $\delta = \tau/T$ , the duty cycle, is exactly 0.5 as we often assume in the simplified spectrum envelope of a clock signal, a quick look at the  $A_N$  function shows that:

- For each even value of  $n$ ,  $\sin(n\pi\delta)$  equals zero: only odd harmonics are present.
- For small values of  $n$  (1, 3, 5, etc.), the first term equals  $(1/0.5n\pi)$ , while the second term is approximately equal to 1, resulting in the  $1/n$  decrease (-20 dB/dec) that we show beyond first-corner frequency  $F_1$ .
- For higher values of  $n$ , the [sine] term takes any value between 0 and 1, while  $n\pi t_r/T$  can become very large. So, the product of the two bracketed terms falls off like  $1/n^2$ .

(b) If  $\delta$  is not exactly equal to 0.5 (as is often the case, due to pulse pedestal distortions), even harmonics will take place. Related to the fundamental amplitude ( $A_0$ ), the even harmonics value is

$$A_{\text{even}}/A_0 = (\sin n\pi p)/n \quad (3.4)$$

where  $p = (\delta - 0.5)$ , i.e., the deviation from an ideal 50% duty cycle.

As long as  $n\pi p < \pi/6$  (i.e., where  $\sin x \approx x$ ), the even harmonic amplitude is given by

$$A_{\text{even}}/A_0 \approx \pi p \quad (3.5)$$

Thus, although their level is much lower at the beginning than the odd ones, even harmonics are keeping a constant amplitude when  $F$  increases, as long as condition of Equ. (3.5) will hold, reaching eventually the maximum spectral envelope. Then, even harmonics will progressively fall off at -40 dB/decade, like the odd terms. This does not change our maximum field prediction based on the envelope (in fact it justifies it), but the designer must be prepared to find, among the radiated emissions, even harmonics with an amplitude as large as the odd ones (Fig. 3.10).

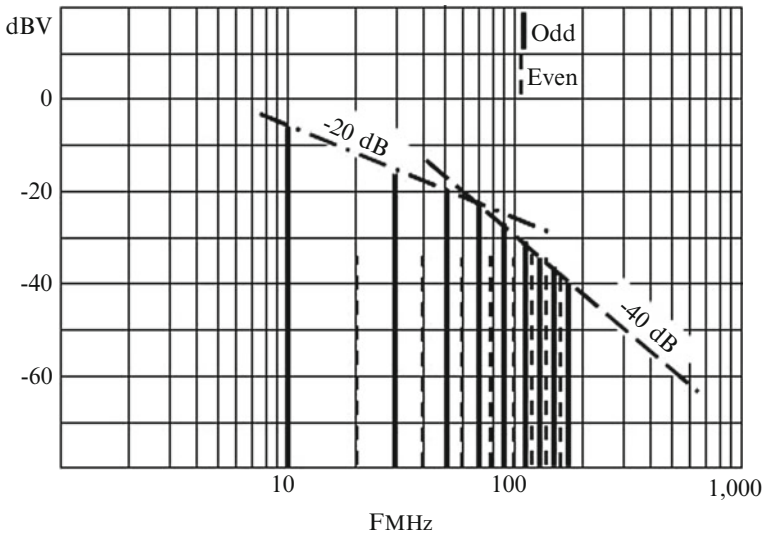
**Example 3.5** Let us take a 10 MHz digital pulse train whose duty cycle is slightly asymmetrical:

$$\delta = 0.5 - 1\%, \text{ i.e., } \tau = 49 \text{ ns for } T = 100 \text{ ns and } p = 0.01.$$

Assume  $t_r = 5 \text{ ns}$ , so  $F_2 = 64 \text{ MHz}$ . The pulse amplitude is normalized as 1 V. A precise calculation of each term is shown below:

$n$	$A_{\text{odd}}$ , volts	(dBV)	$A_{\text{even}}$ , volts	(dBV)
1	0.64	(-4)		
2			0.02	(-34)
3	0.21	(-14)		
4			0.02	(-34)
5	0.13	(-18)		
6			0.02	(-34)
7	0.08	(-22)		
8			0.02	(-34)
9	0.05	(-26)		
10			0.02	(-34)
11	0.03	(-30)		
12			0.011	(-39)
13	0.024	(-33)		
14			0.01	(-40)
15	0.016	(-36)		
16			0.08	(-42)
17	0.01	(-40)		

Beyond this point, even terms are falling off like  $1/F^2$ , leveling at  $\approx$  same amplitude as odd terms.



**Fig. 3.10** Presence of even harmonics in a 10 MHz pulse train with 49 % duty cycle

**Recapitulation Example 3.6** As a recapitulation exercise, we will run the following example of cable radiation with a combined NB + BB spectrum.

An external cable with unknown balance is carrying differential data with *random pattern* at 25 Mb rate. The equipment I/O port is also polluted by small 50 MHz clock residue riding over the digital pulses. These residues are caused by unipolar current spikes; therefore, they repeat with a 10 ns period. Characteristics for the wanted and unwanted signals are as follows:

- 1) 25 Mb differential signal: Amplitude = 5 V, rise time = 3 ns
- 2) 50 MHz clock spurious, Period,  $T = 10$  ns (every clock transition), Amplitude = 50 mV  
Pulse width  $\tau = t_r = t_f = 2$  ns

Cable length  $\geq 1.50$  m, cable outer diam. = 1 cm, and height above ground  $\approx 0.80$  m.

Calculate the worst-case radiation from this long cable, high above ground, compared to FCC Class B limit, measured in 120 kHz bandwidth.

**Solution**

1) Calculate first the CM characteristic impedance for this cable:

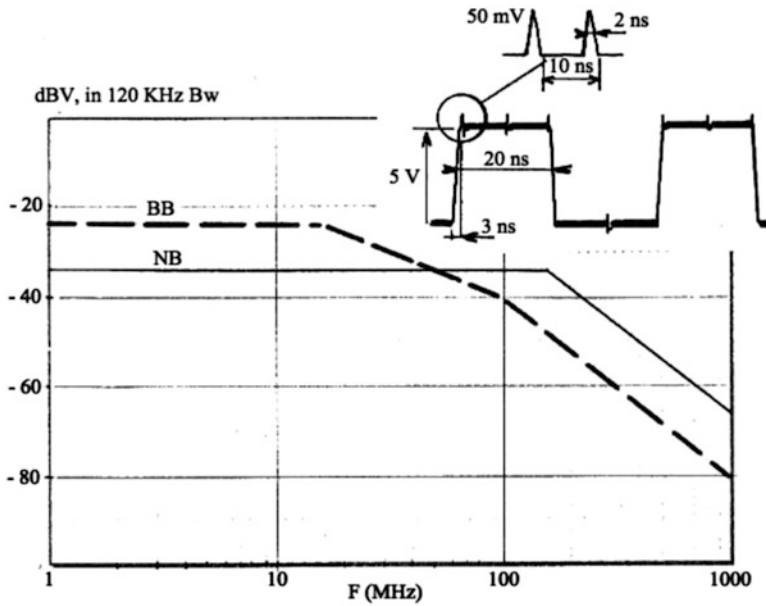
$$Z_{cm} = 60 \ln(4h/d) \approx 300 \Omega = 50 \text{ dB}\Omega$$

2) Voltage spectrum envelope	Random BB (25 Mb)	NB (clock spurious)
Mean bit width	$\tau = 20$ ns	$\tau = 2$ ns
First-corner frequency	16 MHz	160 MHz
Second-corner frequency	106 MHz	160 MHz
Pedestal amplitude	$2A\tau = 0.2$ V/MHz =-14 dBV	$2A\tau/T = 0.02$ V -34 dBV
Correction for random		
Pulse train: 10 log BW(MHz)	-9 dB	NA
Spectrum pedestal, 120 kHz BW	-23 dBV	-34 dBV

Since we are calculating the worst possible radiation, we will estimate the CM current that can drive such long wire configuration. By default, we assume a 10% cable unbalance.

$F$ , MHz	30	60	100	150	300
BB differential voltage, dBV in 120 kHz (Reference-slope decrease)	-28	-34	-38	-45	-57
NB differential voltage, dBV	-34	-34	-34	-34	-46
Larger of the two, or rms combined	<b>-28</b>	<b>-31</b>	<b>-33</b>	<b>-34</b>	<b>-46</b>
CM/DM derating for 10% unbalanced	-20	-20	-20	-20	-20
Corresponding CM voltage drive, dBV	-48	-51	-53	-54	-66
Conversion into dB $\mu$ V: +120	+72	+69	+67	+66	+54
CM current, dB $\mu$ A = dB $\mu$ V -50 dB $\Omega$ :	<b>+22</b>	<b>+19</b>	<b>+17</b>	<b>+16</b>	<b>+4</b>
Maximum $I_{cm}$ criteria (see Chap. 2. Sect. 2.5) for meeting Class B, incl. 4 dB margin	+10	+10	+10	+10	+10

The composite BB/NB voltage spectrum envelope is shown on Fig. 3.11.



**Fig. 3.11** Composite voltage spectrum of Example 3.6. Notice that there is no fixed rep. rate for the 20 ns random pulses

The CM current criteria are exceeded from 30 to  $\approx 200$  MHz. The larger CM current is due to the wanted BB signal up to 50 MHz. In the mid-interval 50–100 MHz, the BB spectrum is overriding the NB one that progressively takes over, and this is their rms addition which is seen. Above 100 MHz, the NB spectrum is the dominant mode.

The problem requires a rather moderate  $>12$  dB improvement, which can be obtained by a better balancing (changing from 10 to 2.5%) or ferrite loading. Notice that filtering only the clock residue would not be sufficient. Once again, we see how little it takes to exceed the radiated limit. Notice that the 50 mV, shown to scale on Fig. 3.11, would go almost unnoticed on a simple oscilloscope display of the full 5 V differential signal.

## REFERENCES

1. D. Bush, in *Spread Spectrum Clocks*, IEEE/EMC Sympos, Chicago, 1994
2. R. Crawhall, in *EMI Potential of non-periodic signals*, IEEE/EMC Sympos, Anaheim, 1992
3. L. Hill, in *Video signals analysis for EMI control*, IEEE/EMC Sympos, Chicago, 1994
4. M. Kuhn, *Compromising emanations from computer displays*. University of Cambridge, Tech. Report #577 Dec., 2003

# Chapter 4

## General Strategy for Designing a Low-Radiation Product

Compliance with radiated emission limits does not occur by chance. With the fairly severe specifications in force today, and with the number and types of fast switching or continuous wave (CW) devices to be found in any equipment, there is practically no example of a product which, having been designed with complete disregard to these aspects, clears through the certification test with an OK label. Therefore, for the sake of self-compatibility (i.e., no self-jamming) as well as compliance with applicable standards, it is necessary to make EMI control a design parameter and to integrate it within the normal process of design activities and reviews.

We will examine briefly, at a managerial level, the following topics:

- System design decisions that impact EMI emissions
- Areas of design activity for keeping emissions under control
- EMI control milestones to be observed during the design process

### 4.1 BASIC SYSTEM DECISIONS THAT IMPACT EMI CONTROL

The designer must make a lot of fundamental decisions in the early stages of a product development, many of which having an impact (good or bad) on the product's EMI characteristics. Therefore, it is of prime importance that an EMC specialist (or someone in design engineering management with an EMC background) presents a clear picture of how all of the given technical options will affect EMC performance. The principal items on this "product design checklist" are as follows (*an asterisk (\*) indicates that radiated EMI levels are affected*):

1. **Interface choice** (e.g., RS232, I2C, RS422/485, Ethernet, CAN, USB, IEEE1394, etc.).
  - **Balanced or unbalanced link\***. A balanced pair with a symmetrical driver/receiver reduces CM loop coupling, for both emission and susceptibility.

- Connector pin assignment\*. Typical interface standards impose a fixed pin assignment. Some imposed assignments result in poor performance with regard to cross talk, radiated emission and susceptibility, and immunity to ESD and fast transients induced on cables.
  - Data rates and maximum permissible rise times\*. These considerations have a direct effect on the spectrum profile and the ability or not to apply signal filtering.
  - Handshake protocols, error detection, error recovery, etc. These affect the device's susceptibility to transients and ESD.
  - Connector type and mounting style\*. Being generally imposed by the standard interface, this may have a direct impact on emissions and susceptibility. Depending on the style (e.g., sub-D, Micro-D, USB, RJ45, FireWire, BNC, SMA, circular), the locking method (threaded, bayonet-mount, screw-mount), and material and finish, bonding between cable shields and the equipment cabinet will range from excellent to poor.
2. **Type of I/O cable used\*** (e.g., twisted pair, shielded twisted pair, shielded twisted pair plus overall shield, ribbon, shielded ribbon, coaxial). This choice affects:
    - Radiated and conducted emissions
    - Radiated and conducted susceptibility
  3. **Cabinet/housing style\*** (e.g., nonconductive plastic, conductive plastic, metal with or without seams and aperture shielding). The choice of the envelope is usually driven by aesthetics, weight and manufacturing considerations, but there are significant related EMC implications. They include:
    - Radiated and conducted emission and susceptibility. Although cables are the predominant radiators, box emissions are frequently found in a range beginning above 100 or 150 MHz. Even with minimal box emissions, a metallic surface may be needed to correctly terminate the I/O cable shield and shielded connectors and to bond EMI filters.
    - Internal EMC. A metal cabinet facilitates the mounting of internal shielded compartments to prevent self-jamming.
  4. **Internal technologies and clock rates\***. Here again, the choices are driven by functional necessities but have a serious (maybe the highest) impact on radiated EMI. Quite often, a designer chooses a technology with a super-fast clock frequency and corresponding rise times for the whole circuitry. Then, after EMI emissions have haunted the engineers and the prototype failed evaluation testing, it is found that 90% of the internal lines must (and can) be decoupled to slow down the rise times.
  5. **Power supply type** (e.g., linear, phase control, switcher with or without a front-end transformer, switcher with multiple isolated outputs, resonant switching power supply). The EMC implications related to power supplies include:

- Conducted and radiated (magnetic) emissions\*. Switcher frequency and topology directly affect conducted and radiated EMI levels. There is also the possibility of self-jamming.
  - Maximum permissible ground leakage current. This is a safety issue that relates to the type of filter allowed by applicable regulations.
  - Primary-to-secondary isolation\*. The topology and type of transformer also affect clock and other harmonics that return and re-radiate via the power cord.
  - Isolated multiple outputs\*. These may be required when there is a mix of analog, RF, and digital circuits in the same equipment. This approach will avoid ground pollution of one circuit by another. This affects self-jamming as well as external emissions.
6. **Applicable mandatory EMC standards** (e.g., FCC Class A or B, CISPR/CE, MIL-STD-461, STANAG, DO160, TEMPEST). These standards are dictated by market regulations (for a civilian product) or the procurement contract (for a military or government supply). Some products that were liberally quoted as “FCC Class A” devices at the design phase have been determined to be relevant to Class B requirements shortly before the first customer shipment. This distinction may translate into a different administrative route (self-verification versus certification) and tougher limits.
7. **Frequency management and frequency plan**\*. This item applies only in cases where the equipment is part of a larger telecom or radiocommunication system or is installed near to one. In such a case, all functional and accessory oscillator frequencies inside the equipment should be checked for possible coincidental co-channel interference with the host installation.

## 4.2 DESIGN CONTROL AREAS FOR RADIATED EMISSION REDUCTION

Once the designer has made the appropriate choices enumerated in Sect. 4.1, with full knowledge of the EMI implications they bear, he should proceed to a comprehensive EMC analysis in the following areas (four of which are illustrated in Fig. 4.1):

1. **Digital ICs and high-frequency generating components.** Identify  $dV/dt$ ,  $dI/dt$ , instant current demand, and package type (DIP, SO, SMC, PGA, plastic or metal can). Establish noise margin and decoupling capacitor needs. For the largest ICs with complex internal functions (MCMs, ASICs, processors), try to obtain from the manufacturer some EMI characterization. These can be gathered from specific component emission database [3], or testing like SAE J1752/3 (TEM cell method) and IEC 61967 conducted signature methods.
2. **PC board.** Review power distribution and return paths. Consider single- vs. multilayer-board design, the need for controlling traces characteristic impedance, and the need of separate ground planes to reduce common ground noise coupling.

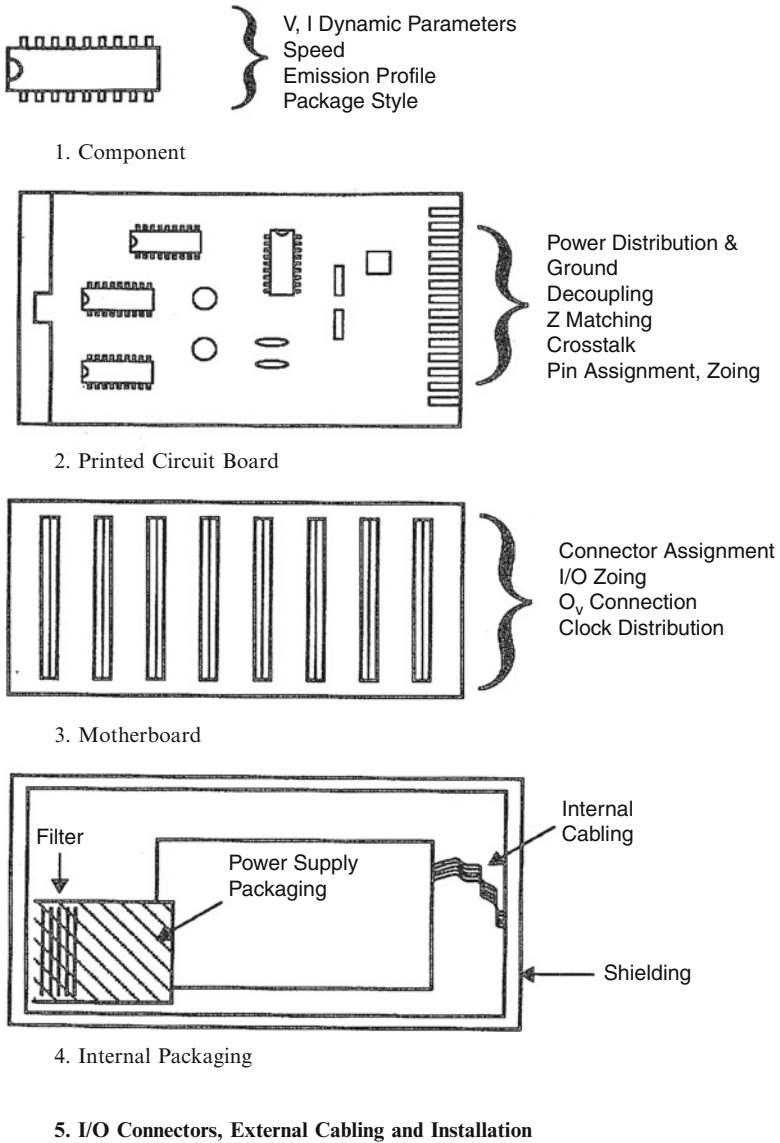


Fig. 4.1 Areas of design strategy for radiated EMI control

Examine radiated emissions at board level. Foresee a possible need to onboard compartmented shields; this is especially critical for equipment using a mix of RF circuits and digital ICs.

- 3. **Motherboard.** Considerations include single or multilayer design, surface vs. buried signal traces, and ribbon cables (with or without a ground plane). Also examine DC voltages and 0 V distribution, and pin assignment to daughter cards.



4. **Internal packaging.** Determine the need for compartmental shielding around noisy or especially sensitive components, and review *I/O* port placement and decoupling. Also relevant are power supply location and filtering (an excellent discussion of this subject can be found in [1]). Possible grounding schemes include isolated 0 V ref vs. chassis, grounded 0 V, or a mix of the two. These choices must be justified.
5. **Housing design and shielding.** If calculated predictions or early tests show that a conductive housing is necessary, it has to be consciously designed rather than thrown in at the last minute. Conductive plastics require a careful analysis of their internal shapes and ribs for coating adhesion and component grounding, as well as for the integrity of the mating edges. Metal housings need a proper tolerances analysis and knowledgeable choice of surface treatment to ensure effective, continuous covers contact.
6. **Installation and external cabling.** Depending on whether the system supplier must provide the external cables and installation guidelines, this may be another area where EMC must be considered. The designer must properly specify (1) external cable type, (2) vendor reference, and (3) any acceptable substitutes. Otherwise, unacceptable “look-alike” cables may be installed.
7. **Testing and certification.** All the items enumerated above will be reviewed in detail in the remainder of this book.

## 4.3 DESIGN MILESTONES FOR RADIATED EMI CONTROL

Radiated EMI is but one of several facets of the EMC discipline, which also includes radiated susceptibility, conducted emissions, and conducted susceptibility. Because these are interrelated, there is no reason for the designer to address them separately; that is, one should not first address radiated emissions, then conducted EMI, then electrostatic discharge, etc. There is a strong reciprocity between emissions and susceptibility, so they should be considered in concert. A calendar of EMC design can incorporate all aspects of EMI reduction, so the reader should keep in mind that the following discussion applies to interference reduction in general, not just to radiated EMI. The following milestones are recommended, for a methodical radiated EMI control.

### 4.3.1 Radiation from Differential-Mode (DM) Loops

**Step 1. Calculate an approximate radiation profile plot,** for PCBs and internal parts (DM radiation). This is done using the Fourier envelopes described in Chap. 3, and the loop models of Sect. 2.3 (especially Fig. 2.6), using the following procedure (see Fig. 4.2):

- Make a list of all the PCBs and other building blocks generating or using pulsed periodic signals, including the signal waveforms and the circuit dimensions.
- For each flow of signal  $S_1, S_2, S_3$ , and so forth listed in the above step, count the number of traces or wires in a given PC board, power supply, or other component. For a purely digital board, this can be approximated quickly: number of traces for signal  $S = 0.5$  (number of modules  $\times$  average number of clocked or synchronous pins per module).
- For each signal  $S_1, S_2, S_3$ , etc., evaluate the average  $\ell \times s$  product of the radiating loop. A rigorous evaluation would require one to physically measure each conductor length, but a good approach is to estimate quickly an average length via the following equation:

$$\ell(\text{average}) = \left( \sum \text{all } S_1, S_2, S_3 \text{ etc. run lengths} \right) / N \text{ runs}$$

An even quicker way is to take the coarse approximation: average length  $\ell = 0.25 \times$  (PCB diagonal span). Dimension  $s$  can be taken as the average distance to the next parallel return trace (single-layer boards) or the dielectric thickness above the 0 V plane (boards with Gnd planes).

- (a) Add the following to the previously calculated  $\ell \times s$  areas:
- Module package areas (0.4 cm<sup>2</sup> for a 14-pin DIP, 0.1 cm<sup>2</sup> for a 14-pin SMT, etc.)
  - Area of decoupling capacitors to IC pins
  - Eventually, areas of *I/O* wire pairs for related signal from PCB to *I/O* connector
- (b) For each signal  $S_1, S_2, S_3$ , etc., perform a quick plot of the NB or BB Fourier envelope.

We know that for each circuit carrying  $S_1, S_2, \dots, S_n$ , the corresponding radiated field is calculatable from the electromagnetic moment volt  $\times$  cm<sup>2</sup> or amp  $\times$  cm<sup>2</sup>, per the following function:

$$\begin{aligned} \text{at frequency } F_x : E_1(\mu\text{V/m}) &= V_1 \times A_1 \times K_{F_x} \\ E_2(\mu\text{V/m}) &= V_2 \times A_2 \times K_{F_x} \end{aligned}$$

etc.

Where  $K_{F_x}$  is the loop-to-field transfer function for 1 V-cm<sup>2</sup> (see Chap. 2, Equ. (2.22)), a constant for a given frequency  $F_x$ , except for the circuit impedance adjustment if less than 377  $\Omega$ .

- (c) For the desired test interval  $F_{\min}, F_{\max}$  (e.g., 30-1,000 MHz, for FCC regulations), we will fill in Table 4.1.

If, while still at the drafting level, the design meets the bottom line criteria in Table 4.1, there is nearly a 100% chance that the equipment alone, unshielded and without its external signal and power cables, will comply. This is due to the several small, but cumulative overestimations that were made intentionally.

**Step 2. If step #1 shows excessive radiation**, the designer must consider the following options while the design is still flexible. The appropriate one will depend on which signal and which circuit has caused the limit violation:

- (a) Enlarge 0 V ground areas and add guard traces running along noisy traces.
- (b) Provide better IC decoupling.
- (c) Use a multilayer board, and bury noisy traces between two Gnd layers
- (d) If all else fails, add box shielding, or compartmented shields at board level.

**Step 3. As soon as prototypes of the major subassemblies are available**, run a coarse emission test in an anechoic chamber, at 1 m distance, to see if a sufficient margin exists at individual block levels. For some components (e.g., microprocessor boards, master clocks, oscillator circuits, I/O drivers), it may be convenient to power the prototype by a battery pack strapped under the board instead of using a bench-type power supply.

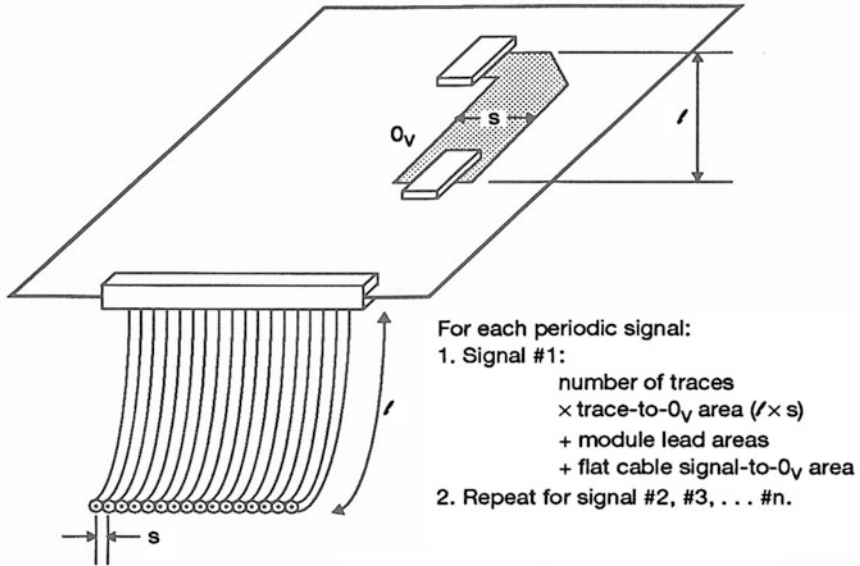
If the limit to be met is specified at 10 or 30 m (FCC, for instance), apply 1/D conversion factor to the Fig. 2.6 results, above  $\approx 30$  MHz. If a same board is to be present  $N$  times in the future equipment, add  $20 \log N$  to the measured field, for coherent addition, and  $10 \log N$  for random, noncoherent addition. In practice, above 2–3 identical daughter boards, the quasi-peak detector used for FCC/CISPR makes that the addition is seldom coherent.

### 4.3.2 Radiation from Common-Mode (CM) Excitation

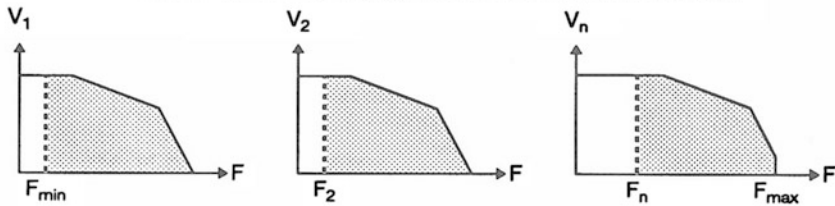
**Step 4.** Up to this point, we have focused mostly on controlling DM radiation from PCBs and internal circuits. As soon as a breadboard prototype of the complete product exists, check it for CM current leakage on I/O cables. This is made in the lab (not necessarily a shielded room if ambient RF noise, especially from FM and TV stations, is low enough). This is done rather easily with a current probe and a spectrum analyzer. Apply the following criteria for each spectral line:

- (a) For FCC or CISPR/CE Class (B),  $I_{cm} < 10 \text{ dB}\mu\text{A}$  at  $F > 30 \text{ MHz}$
- (b) For FCC or CISPR/CE Class (A),  $I_{cm} < 20 \text{ dB}\mu\text{A}$  at  $F > 30 \text{ MHz}$
- (c) For MIL-STD-461-RE102 most severe limit,  $I_{cm} < 10 \text{ dB}\mu\text{A}$  at  $F = 50 \text{ MHz}$ , down to  $4 \text{ dB}\mu\text{A}$  at  $300 \text{ MHz}$

If the CM current criteria are not met, add filters to I/O ports, use ferrite beads or cable shielding, and reiterate until  $I_{cm}$  decreases sufficiently. Full details on this evaluation method are given in Chap. 13.

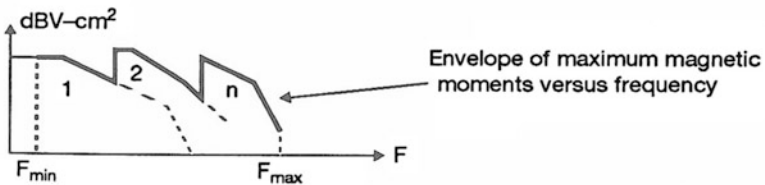


3. Plot each signal spectrum, starting from the lowest rep. frequency.



	F <sub>min</sub> ----- F <sub>max</sub>							
Signal #1	V-cm <sup>2</sup>	V-cm <sup>2</sup>	V-cm <sup>2</sup>	V-cm <sup>2</sup>	V-cm <sup>2</sup>			
Signal #2	X	X	V-cm <sup>2</sup>	V-cm <sup>2</sup>	V-cm <sup>2</sup>	V-cm <sup>2</sup>	V-cm <sup>2</sup>	
...								
Signal #n	X	X	X	X	V-cm <sup>2</sup>	V-cm <sup>2</sup>	V-cm <sup>2</sup>	V-cm <sup>2</sup>
ΣV-cm <sup>2</sup>								

4. Sum up all V-cm<sup>2</sup> across the spectrum.



5. Use dBV - cm<sup>2</sup> to calculate composite field across frequency.

Fig. 4.2 Method for making a coarse estimate of cumulative fields from all DM loops

**Table 4.1** Calculated radiation profile data sheet

$F_{min}$	$F_1$	$F_2$	$F_3$	$F_4$	$F_n$	$F_{max}$
<b>Signal #1</b>						
$V_1$ , harmonic amplitude (dBV)						
Area, $A_1$ (dBcm <sup>2</sup> , including $\lambda/4$ limitation)						
<sup>a</sup> dB current adder = $20 \log(377/Z_L)$ if $Z_L < 377 \Omega$						
$M_1$ (dBV-cm <sup>2</sup> ) = $V_1 + A_1 + (^a\text{dB})$						
<b>Signal # 2</b>						
$V_2$ , harmonic amplitude						
Area, $A_2$ (dBcm <sup>2</sup> )						
<sup>a</sup> dB current adder, if $Z_L < 377 \Omega$						
$M_2$ (dBV-cm <sup>2</sup> ) = $V_2 + A_2 + (^a\text{dB})$						
<b>Signal # n</b>						
$V_n$ , harmonic amplitude						
Area, $A_n$						
<sup>a</sup> dB current adder, if $Z_L < 377 \Omega$						
$M_n$ (dBV-cm <sup>2</sup> ) = $V_n + A_n + (^a\text{dB})$						
$K_{\text{dB}\mu\text{V/m}}$ for 1 $V_x$ 1 cm <sup>2</sup> and 377 $\Omega$ at frequency $F_x$						
<sup>b</sup> $E_{\text{total}} = K + \log[10^{M_1/20} + 10^{M_2/20} + \dots + 10^{M_3/20}]$						
Specification to be met (dB $\mu$ V/m)						
$\Delta = E$ - specification						

<sup>a</sup>The current multiplier is to account for the  $E$ -field increase, especially in far field, for circuits with low-load impedance, i.e., higher currents than  $V/377 \Omega$  (or 2.6 mA per volt)

<sup>b</sup>A quicker way is to retain, in each frequency column, only the larger value among lines  $M$ , provided it dominates the others by  $>20$  dB. This is not always possible

## 4.4 INFLUENCE OF THE RESIDENT SOFTWARE ON RADIATED EMI

Although radiated emissions above 30 MHz are generally dominated by the clock frequency spectrum (see Chap. 3, Fig. 3.8), amplitudes variations up to 10 dB have been recorded for a same product with two versions of the software. The version which was radiating the most had simply more instructions and a particular shift in a sequence of the main program (e.g., changing from address 7FFF to 8,000, where 16 bits are switching simultaneously). Because they kind of “undercarry” the clock spectral lines, data and address bus are non-negligible contributors to total radiation. The software dependency of their contribution depends on how they are multiplexed. In the main operating program, instructions which are constantly cycling in a repetitive mode will contribute to measured EMI, since typically the radiated test is made with the spectrum analyzer/receiver in a peak/hold mode.

Several software/firmware precautions can reduce this contribution [2]:

- To access frequently used variables, use as much as possible the RAM internal to the processor.
- Do not send high-rate bus signals on peripheral devices if these signals are only needed a few times/s. For instance, on a display, use a software latch such as multiplexed data are sent to the display flat cable only when needed.
- When a clock sync. is needed between different equipments, do not send clock pulses directly on the interconnecting cables. Use scrambling or similar techniques.
- A keyboard does not need 4 MHz multiplexing. A multiplexing made at  $<1$  kHz still allows keystroke detection while generating less average radiation.

## REFERENCES

1. J. Fluke, *Controlling conducted Emissions by Design* (Van Nostrand, New York, 1991)
2. O. Roy, *Influence of resident Software on Radiated EMI*. In Encyclopédie "Mairise de la CEM", Dunod, Paris, 2000
3. E. Sicard, S. Ben Dhia, *EMC of Integrated Circuits, Chap. 7 Guidelines for low Emissions*, Springer, 2006

# Chapter 5

## Controlling Radiated Emissions at Chip and Integrated Circuit Level

Controlling necessarily implies understanding. Let us start by remembering that it takes two things to constitute a radio transmitter, intentional or not: a signal source and an antenna. The many fortuitous antennas have been discussed in Chap. 2. This chapter will address the most elementary building block in the system with regard to its ability to act as an RF source. Choosing ICs designed with low-RF signature makes the whole process of EMC compliance an easier target to hit. Interestingly, most of the IC parameters and behaviors that we will show are also major players in the susceptibility, self-compatibility, and signal integrity of our equipment.

This chapter does not pretend addressing in depth the EMI-free design of an IC. There are several excellent, though not widely distributed, documents on this subject, like [12] by E. Sicard, a masterpiece of the kind. But we will review, through practical descriptions and numerical examples, the important role of the digital ICs in the generation of unwanted RF fields.

### 5.1 LOGIC FAMILIES

Table 5.1 lists the typical characteristics of the most popular digital families, including the parameters of interest for radiated emission. They correspond to one simple active device (an elementary gate, or a driver) in a module that may contain from four up to hundreds of thousands of these devices. This elementary gate will be the switching device we will always consider in our analysis of noise generation.

All the discrete values in the table, voltage swing,  $t_r/t_f$ , input capacitance, output resistance, etc., are those that are in the realm of the end user. Many complex ICs have internal circuitry operating at much higher speed (way above GHz), faster transitions, and lower capacitances than what is shown, but such parameters are essentially under the control of the IC designer, not of the user.

The bandwidth is calculated by  $1/\pi t_r$ , with  $t_r, t_f$  being the rise and fall times. For bipolar technologies, rise and fall times are generally different, but the equivalent

bandwidth has been calculated from the shorter of the two. Rise and fall times also depend on loading, with the faster transition (e.g., the highest bandwidth) corresponding to the lowest loading. The table values for  $t_r$ ,  $t_f$  correspond to a moderate loading (20–40 pF), representing reasonably fast conditions.

Column captioned “output resistance” is indicative of the worst-case internal resistance of a single device output, in low or high state. Logic gates being nonlinear, these dynamic resistances have been derived from a piecewise approximation of the  $V_{OL}$ - $I_{OL}$  and  $V_{OH}$ - $I_{OH}$  curves. For immunity analysis, the designer is concerned with the highest value of  $R_g = \Delta V/\Delta I$ , since this corresponds to a high impedance condition for crosstalk and  $E$ -field coupling. For emission control, our concern here, the worst condition corresponds to low values of  $R_g$ , since this will be the current limiting parameter when, to the extreme, the gate will drive a heavy capacitive load, or the equivalent of a shorted line at resonant frequencies of the PCB trace layout. Accordingly, even a shorted gate output (during the time of a transition) cannot deliver a current greater than  $V/R_g$ .

**Table 5.1** Essential characteristics of logic families

Logic name	Volt. swing $\Delta V_{L-H}$ (V)	$t_r/t_f$ (ns)	Equivalent bandwidth (MHz)	Input cap. (pF)	Output resist. $L/H$ ( $\Omega$ )	DC noise margin (V) worst case
CMOS	5	50/50	6.5	5	500/350	1.2
TTL7400 <sup>a</sup>	3.5	10/8	40	5	30/100	0.4
LS	3.5	10/5	65	3.5	20/40	0.4
HC240	5	4/4	80		20/25	0.7
HC00, AHC	5	3.5/3.5	95	3.5	50/80	1.3
HCT	5	3.5/3.5	95	4.2	50/80	0.7
LVMOS	3.3	3/3	110	4.2	50/100	0.6
FAST and AS	3.5	3/2.5	125	4.5	15/20	0.3
ABT240	3.5	1.5/1.5	220	3	6/200	0.5
LVDS	0.4	$\leq 1$	$>320$	4	100/100	0.15
ACT	5	0.7/0.7	500	3	10/15	0.4
ECL, PECL	0.8	0.3/0.3	1000	3	7/7	0.1

<sup>a</sup>The straight TTL is an obsolete family, shown only for comparison with its successors. ABT240 and HC240 are driver series. Although abandoned in new designs, CMOS has been shown for reference.

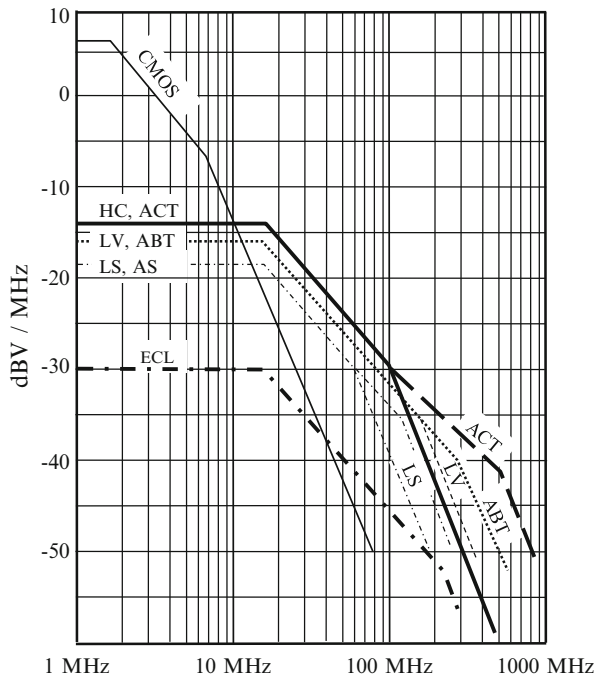
One word of caution: vendor-published rise/fall times are often the maximum (longest) or typical ones, that is, the manufacturer guarantees that the device will not be slower than this. Minimum  $t_r/t_f$  are generally not published, assuming that nobody would complain if the device is faster than announced. Unfortunately, EMI concerns aggravate with shorter transitions. IC specialists have at their disposal large databases like IBIS library that allow simulations of “corner technological parameters.” For instance, for a 0.8 V drain-source voltage, a typical device current



of 0.8 mA/gate can vary from 0.55 to 1.15 mA due to extreme temperature variations and manufacturing process spread.

Figure 5.1 shows comparative plots of the spectral densities for several popular logic families, which are a direct measure of their propensity to EMI generation. The BB spectra are calculated for a single pulse of each family, all with a same 20 ns pulse width, except for CMOS (200 ns). The associated table shows the relevant parameters of the comparison, like spectral density  $2A\tau$ ; corner frequencies  $F_1, F_2$ ; and the spectral density at  $F_2$ . Notice that in spite of a slightly slower rise time, HC generates higher spectral density than FAST and AS, because of its larger  $dV/dt$  at the transitions. In spite of its high-speed capability, ECL has the lowest spectral amplitude.

	A (V)	$2A\tau$ (V/MHz)	$F_1 = 1/\pi\tau$ (MHz)	$F_2 = 1/\pi t_r$ (MHz)	Ampl. at $F_2$ (dBV/MHz)
CMOS	5	2	1.6	6.4	-6
LVMOS	3.3	0.13	16	110	-34
LS	3	0.12	16	65	-30
FAST, AS	3	0.12	16	125	-37
HC	5	0.2	16	90	-29
ABT	3.5	0.14	16	220	-40
ECL	0.8	0.03	16	220	-66
ACT	5	0.2	16	500	-43



**Fig. 5.1** Voltage spectra of logic devices, assuming 20 ns bit pulse width for all technologies except CMOS (200 ns)

## 5.2 CONTRIBUTORS TO IC UNDESIRE EMISSIONS

The major players in noise generation mechanisms, some of them appearing on Table 5.1, are reviewed hereafter.

1. *Rise and fall times.* The shorter they are, the wider the occupied spectrum of the corresponding logic pulses. Since EMI problems aggravate with  $F$  (for conducted EMI and crosstalk) and often  $F^2$  (for radiated EMI), the consequence is obvious.
2. *Power supply transition current.* This is the instantaneous demand of the device alone during switching, regardless of its loading. Its peak value and duration are intrinsic to the technology. It can be very large, having nothing to do with the quiescent current during an established “1” or “0.” In TTL-derived families, and to some extent in the fast HCMOS technologies, this inrush current is due to the partial conduction overlap of the two output transistors arranged in “totem pole.” During this overlap, the  $V_{cc}$  bus is virtually shorted to ground via two partially saturated transistors plus a limiting resistor. Recent designs have reduced this effect by using Schottky barrier diodes (SBDs) to prevent the output transistors from going into excessive saturation. Some manufacturers are also using “edge control” circuits by replacing one large-output transistor with a group of smaller ones. However, the current peak is still significant and can pose PCB problems or even on-the-chip problems with gate arrays or other highly populated chips.
3. *Voltage swing.* This low-high or high-low excursion relates directly to  $E$ -field radiation and capacitive crosstalk.
4. *The instantaneous gate output current* that is forced into (low-to-high transition), or pulled from (high-to-low), the driven gates. It is also larger than the quiescent current. For short lines, this load current can be calculated by

$$I_2(\text{max}) = \Delta V / (R_g + dt/C_L) \approx C_L \times \Delta V / \Delta t \text{ if } R_g < \Delta t / C_L \quad (5.1)$$

In Equ. (5.1),  $C_L$  is the sum of the driven trace capacitance to ground (0.1-0.3 pF/cm for single-layer boards, 0.3-1 pF/cm for multilayers) and the input capacitance of the driven gate(s), as given in Table 5.1. For instance, a 3.5 V/3 ns rise front, driving a 5 cm-long trace on a single-layer board with a fan-out of 5 gates at the end, will cause a transient output current:

$$I_2 = (5 \text{ cm} \times 0.3 \times 10^{-12} \text{ F/cm} + 5 \times 5.10^{-12} \text{ F/gate}) \times 3.5 \text{ V} / 3.10^{-9} = 30 \text{ mA}$$

### 5.2.1 Transient Peak Currents

The way the internal power transition current  $I_1$  and the output current  $I_2$  are adding during gate switching is described on Fig. 5.2a. We see that the two currents combine in a nonsymmetrical manner. For low-to-high transitions, load current  $I_2$  is adding up to  $I_1$  in the  $V_{cc}$  lead, but not in the Gnd lead. For high-to-low,  $I_2$  adds up to  $I_1$  in the Gnd lead, since the gate is “sink” and the capacitive charge from the load has to

discharge into the driving gate output, which appears as a short to ground. This can be displayed as follows:

	Low-to-high transition	High-to-low transition
Currents in $V_{cc}$ lead:	$I_1 + I_2$	$I_1$
Currents in Gnd lead:	$I_1$	$I_1 + I_2$

During a low-to-high switching, currents are adding up in the  $V_{cc}$  lead, causing a maximum  $V_{cc}$  noise (negative voltage drop). All the same, during a high-to-low switching, currents add up in the Gnd lead, causing a maximum PCB ground noise.

When the driven line is electrically long, i.e., when its propagation delay is not small compared to the pulse rise time, the instantaneous output current  $I_2$  becomes limited by  $Z_0$ , the characteristic impedance of the driven trace. In epoxy glass, propagation speed is approximately 14 cm/ns, corresponding to a propagation delay of 70 ps/cm. Transmission line problems become serious when line delay  $T_d$  exceeds half of  $t_r$ , the pulse rise time. So, for estimating  $I_2$ , we can simply define a “long line condition” as follows: if trace length  $\ell$  is  $\geq 7 \text{ cm} \times t_r(\text{ns})$ , the maximum possible output current during transition is equal to

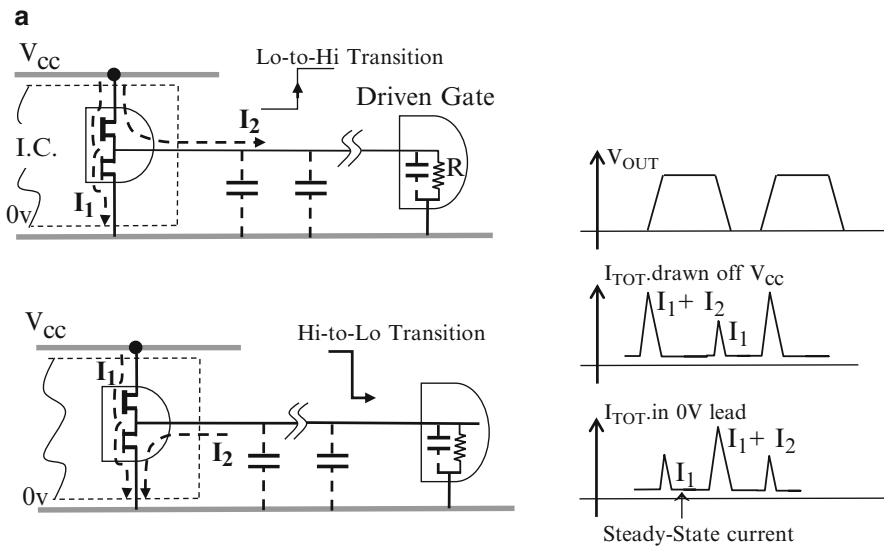
$$I_2(\text{max}) = \Delta V / Z_0 \tag{5.2}$$

where  $Z_0$  is the characteristic impedance of the driven trace.

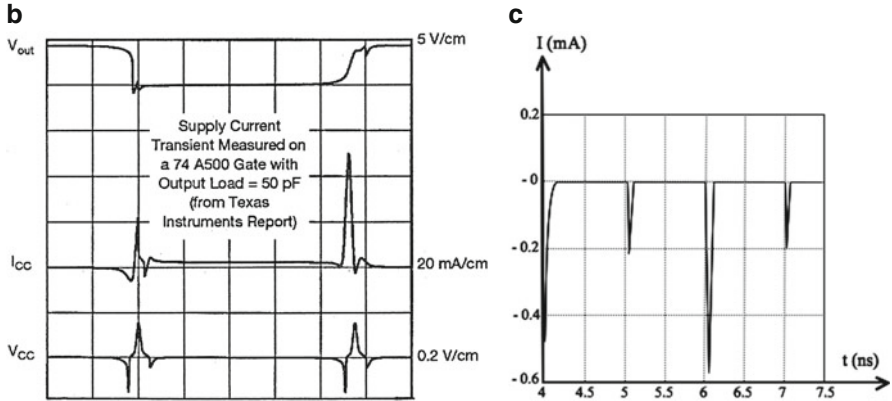
For instance, if  $Z_0 = 90 \Omega$ , a 3.5 V swing will cause:

$$I_2 = 3.5 / 90 = 38 \text{ mA, at the time of the rising front}$$

Ultimately, since very low-line impedances cannot create infinite currents,  $I_2$  is limited by the output resistance of the gate.



**Fig. 5.2a** (a) Transient currents drawn by a gate off the power distribution bus, with the different combination of  $I_1, I_2$

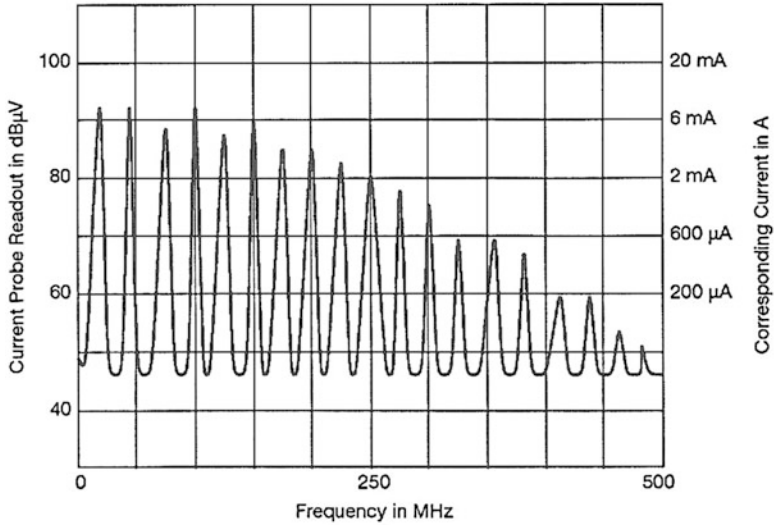


**Fig. 5.2b** (continued) (b) Power supply instantaneous current on a 74AS00. The difference between the current peaks for a positive and negative output swing is clearly visible. Notice also the corresponding noise glitches on the  $V_{cc}$  bus. (c) Instantaneous consumption of an internal gate in a VLSI (0.18  $\mu\text{m}$ ) device [12]

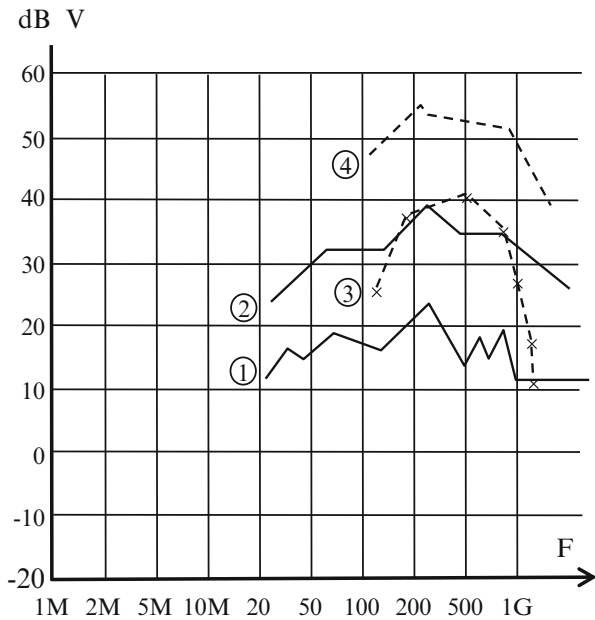
## 5.2.2 Fields Radiated by the IC Alone

Figures 5.3, 5.4, and 5.5 show measured and computed values of conducted currents and radiated fields during the logic devices operation. Since generally the basic building block of an LSI or VLSI chip is still a gate, the radiation from a module can be estimated starting from that of an elementary gate, as shown in Fig. 5.5. However, since thousands or more gates can exist in a single chip, the radiation from the entire module cannot be the arithmetic sum of all the gates' radiation. Not all gates operate synchronously, and as the orientation of the radiating doublets in the chip is random, they can add or subtract as well [3].

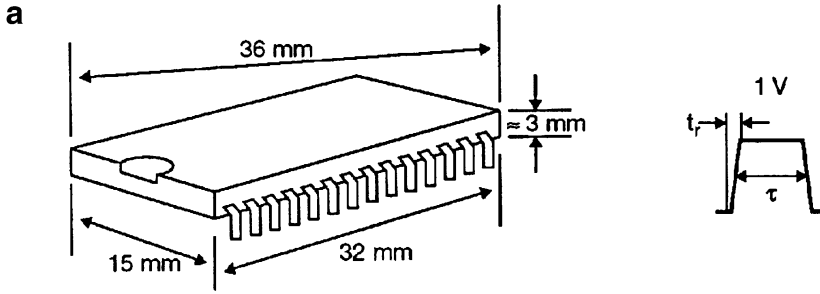
Either some randomization is accounted for in math models or actual measurements must be made of complex chips [8, 9]. For microprocessors (since many operations with various data rates take place inside the chip), radiated and conducted profiles contain all frequencies corresponding to internal transactions between the arithmetic logic unit (ALU), the registers, buffers, and so forth. Their frequencies are the clock rate and its submultiples, plus all their harmonics.



**Fig. 5.3** Frequency spectrum of current demanded by a typical digital device (74LS gate)

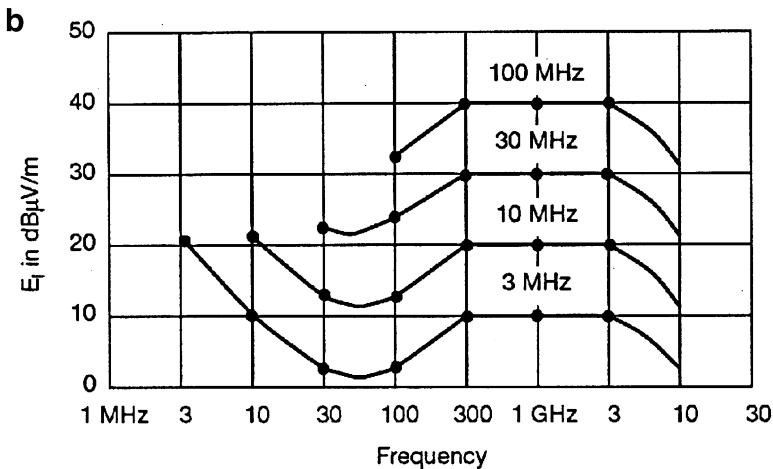


**Fig. 5.4** Measured emissions from a  $\mu$ Controller (INFINEON Tri-Core with 32 bit  $\mu$ C + DSP + bus interface). Curve (1): only core internal 16 MHz clock active. (2) External clocks active, linked with memories activity. (3) Calculated values for case #2. (4) Internal clock increased to 120 MHz. TEM voltages shown are approximately equivalent to  $E$  field at 1 m (from Sicard, Steineke, [11, 12])



		<i>F</i> in MHz							
$\tau$ in ns	$t_r$ in ns	<i>E</i> field @ 1 m in dB $\mu$ V/m/MHz	3	10	30	100	300	1,000	
100	10	A	0	-10	-18	-24	-24	-24	
30	3	B	-10	-10	-18	-14	-14	-14	
10	1	C	-20	-20	-18	-14	-4	-4	

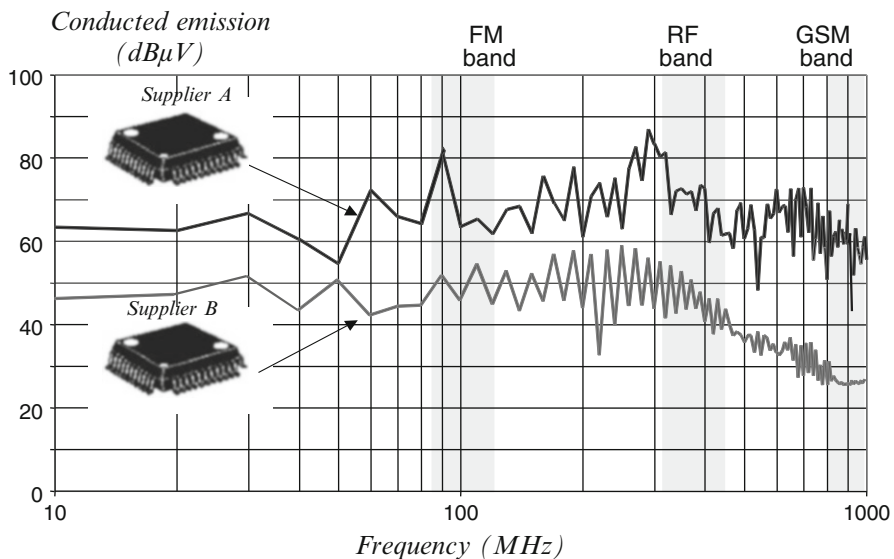
Calculated BB field for a 1 V pulse, one gate, and three different pulse characteristics. For different pulse voltages, fields will vary proportionally.



NB fields for fast 3.5 V/1 ns rise time and four different clock frequencies. Duty cycle = 50%, and there are 30 clock-triggered gates on the chip.

Fig. 5.5 BB (a) and NB radiated fields, 1 m from a typical 28-Pin DIP Module. Above 50 MHz, the field has been calculated assuming an average 300  $\Omega$  load. For the NB example (b), a statistical spread has been assumed for the 30 loops dimensions.

Large modules, and furthermore multi-chip modules (MCM), consist of entire sets of gates (clock-driven blocks) synchronized by a same clock. Clock sync. operations are also found in memories read/write/refresh, or fast *I/Os* switched in parallel. The trend in lower DC voltage, from 5 to 3.3 V, then to 1.2 or 0.8 V, often results in an increase of  $dI/dt$  slopes, even though the absolute value of current  $I$  is smaller. Finally, another aspect of radiated EMI from logic chips is the wide variance between manufacturers for the same IC device. An example of differences is shown in Fig. 5.6, between two vintages of a large flat pack ICs, mounted on the same test board.



**Fig. 5.6** Radiated emission of 2 ICs from different suppliers. Measured voltages ( $\text{dB}\mu\text{V}$ ) on TEM cell correlate approximately with  $E$  field at 1 m (from E. Sicard et al. [12])

With large IC modules, and especially processors with clock rates above 150-200 MHz, a point is reached where the IC alone, even resting on a perfectly shielded PCB, may radiate above the authorized limit. Figure 5.7 shows an example of the radiated field from a 200 MHz Pentium<sup>®</sup>. The field value, translated at 3 m, exceeds the FCC Class B limit. This peculiar aspect will be addressed in detail in the next sections. It must be remarked that such devices are topped with large heat sinks, which contribute significantly to the radiated field: being electrically floating, they behave as an electric dipole, capacitively excited by the  $\mu\text{P}$  die just underneath.

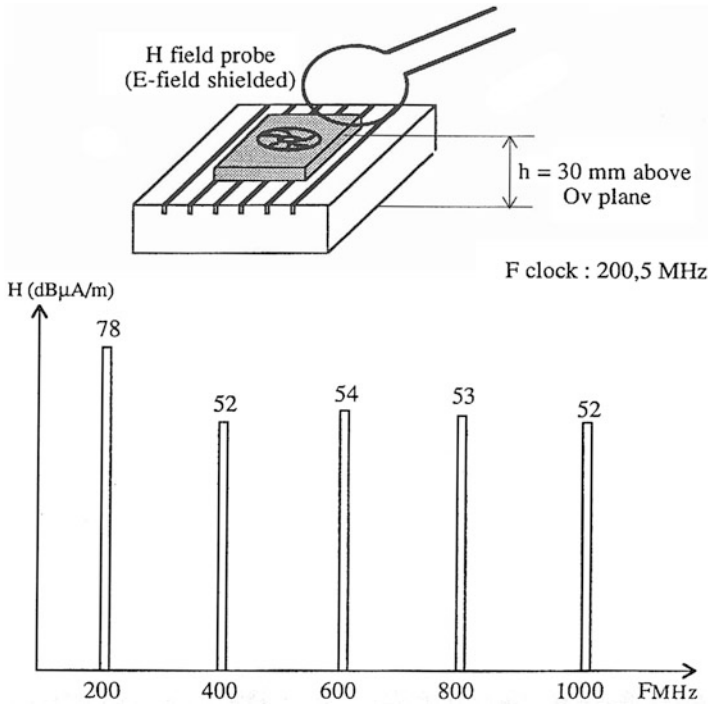


Fig. 5.7 Measured  $H$  field at 3 cm above a 200 MHz Pentium®

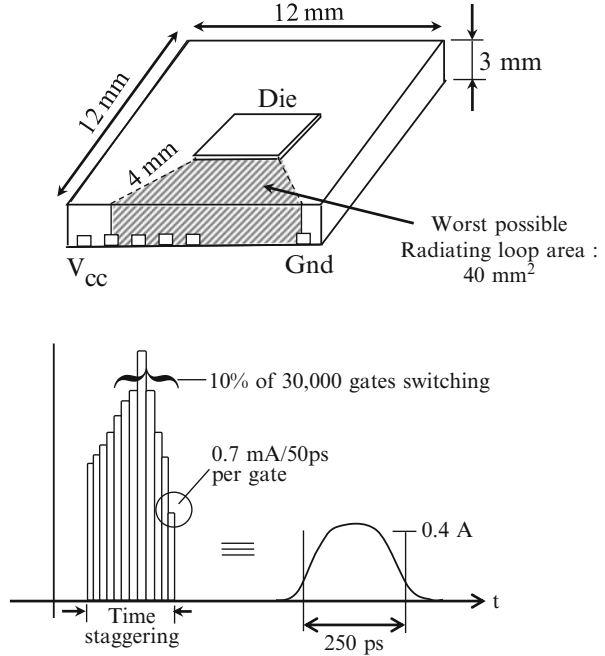
**Numerical Example 5.1** The module in Fig. 5.8 is a VLSI device run by a 1 GHz clock. The 32 bit  $\mu P$  is using 30,000 gates. The peak transient current for each gate is 0.7 mA, with a 50 ps duration. During the most busy operating mode, 10% of the gates are switching simultaneously, so the total, instantaneous peak demand is

$$0.7\text{mA} \times 30,000 \times 10\% = 2.1\text{A}$$

Because of small differences in path lengths inside the chip, due to physical placement, small delays (7 ps/mm) exist between the exact current peaking of the various gates. Simulation and measurements have shown that the sum of the scattered delays results in a five times spread, such as the theoretical 2.1 A/50 ps spike actually resembles a 0.4 A peak stretched over  $50\text{ps} \times 5 = 250\text{ps}$ . Estimate the radiated  $E$  field at 1 m distance, for the 1,000 MHz fundamental frequency.



**Fig. 5.8** IC radiation from Example 5.1



**Solution** We start by calculating the fundamental term of the Fourier series. From Figs. 3.1b or 3.2, we obtain the amplitude of the first term, given that the pulse duration  $\tau$  is  $\ll$  period  $T$ :

$$\begin{aligned} \text{Current } I @ 1,000 \text{ MHz} &= 2 \times 0.4 \text{ Amp} \times \tau/T \\ &= 2 \times 0.4 \times 250 \text{ ps}/1,000 \text{ ps} = 0.2 \text{ A} \end{aligned}$$

The worst possible area is that formed by the bonding wires farthest from the V<sub>CC</sub> or Gnd wires. For the 40 mm<sup>2</sup> loop, differential-mode radiation is calculated from Equ. (2.22), by directly entering the current:

$$\begin{aligned} E(\mu\text{V}/\text{m}) &= [1.3 \times 0.2 \text{ A} \times 40 \times 10^{-2} \text{ cm}^2 \times (1,000 \text{ MHz})^2]/D \\ &= 1.04 \times 10^5 \mu\text{V}/\text{m} \text{ or } \approx 100 \text{ dB}\mu\text{V}/\text{m} \text{ at } 1 \text{ m} \end{aligned}$$

Given that there will be an integral ground plane underneath the chip, at a height  $h = 3 \text{ mm}$ , we can consider that the loop will benefit from the reduction by the image plane Equ. (2.29), under the condition that  $h < \lambda/10$ . The reduction factor is

$$K_r = 20 \log 10h/\lambda$$

Thus, for 1 GHz (with  $\lambda = 300 \text{ mm}$ ),  $K_r = 20 \log 10 \times 3/300 = -20 \text{ dB}$

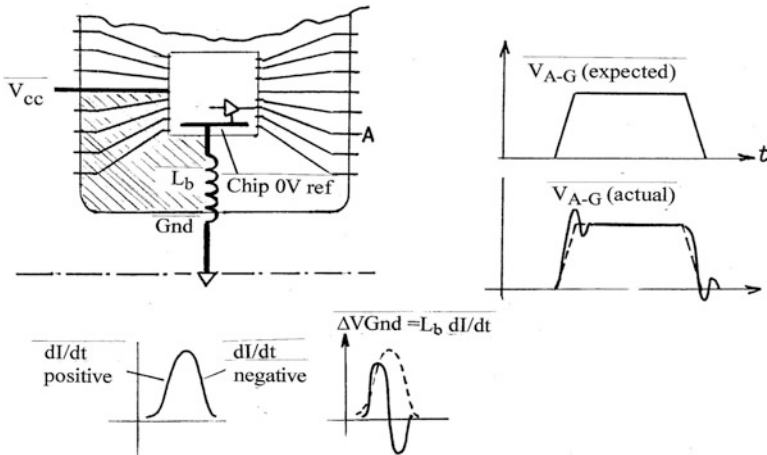
$$\text{Actual field at } 1 \text{ m} : 100 \text{ dB}\mu\text{V}/\text{m} - 20 \text{ dB} = 80 \text{ dB}\mu\text{V}/\text{m}$$

Should the host equipment have to meet MIL-STD-461-RE102 limit of  $44 \text{ dB}\mu\text{V/m}$ , there is a 36 dB violation<sup>1</sup> that must be corrected by several possible solutions, at IC design/packaging level:

- Reducing the loop area by rearranging the die-to-leads bonding wires
- Installing a storage capacitor right under, or embedded in, the chip
- Fragmenting the  $V_{\text{dd}}\text{-}V_{\text{ss}}$  loop in several, smaller loops, with opposing magnetic moments

### 5.2.3 Generation of Common-Mode Noise by IC Ground Bounce

The so-called ground bounce is a common impedance problem between the chip and the host PCB [5, 15] caused by the  $dI/dt$  effect in the IC ground lead (bonding wire plus pin). A single poorly designed oscillator, or drivers with too much peak current demand, can lift the whole chip 0 V reference vs. the PCB ground. This transient voltage shift will be carried over by all the  $I/O$  signals pins, exporting this noise spike to the rest of the PCB, and ultimately causing  $I/O$  lines radiation (see Chap. 2, CM radiation mechanisms). Figure 5.9 shows the basic cause for ground bounce, and Fig. 5.10 displays comparative results for an ALS driver and an AC driver. In both cases, 7 out of 8 outputs are switched simultaneously while the last one is set to “0.” The ground bounce on the non-switched pin reaches 1.5 V for the AC family, a potential cause of EMI. The overshoot/undershoot of the waveform can be easily mistaken for a mismatch problem. The shaded area corresponds to the radiating loop of the IC alone.



**Fig. 5.9** The ground bounce phenomena at IC level.  $\Delta V_g$ , the voltage drop in the bonding wire inductance  $L_b$ , is adding to the normal signal of the device being switched, but it also offset the entire chip 0 V reference for all the other  $I/O$  pins

<sup>1</sup>The violation could be even worse if the device was intended for a motor vehicle application, relevant to a more severe clause of CISPR 25 for onboard equipments.

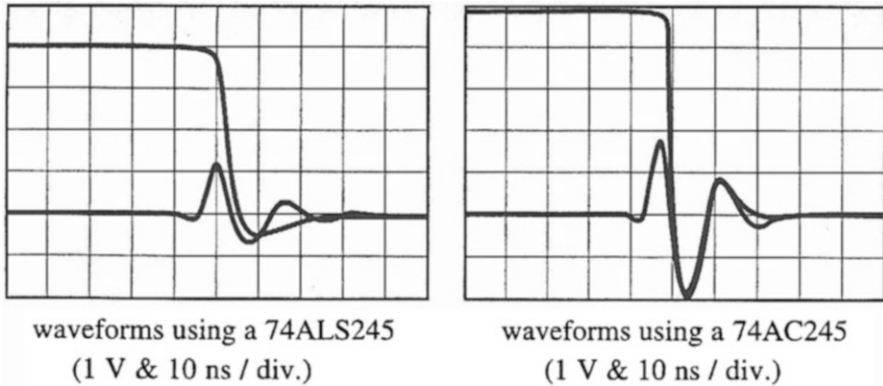


Fig. 5.10 Ground bounce with two logic drivers families

Improved packaging styles (see Sect. 5.5) exhibit less ground bounce, owing to the reduced parasitic inductance. For instance, a 16-driver-SSOP module with 48 pins, including 8 distributed Gnd have only 0.4 V of ground bounce during a 15/16 output simultaneous switching, i.e., three to four times less than a DIP package with corner Gnd pin.

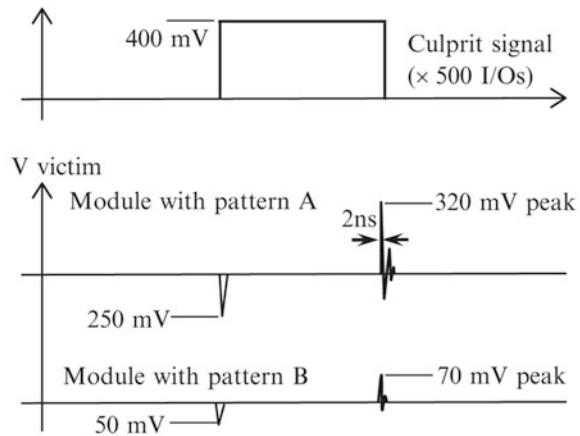
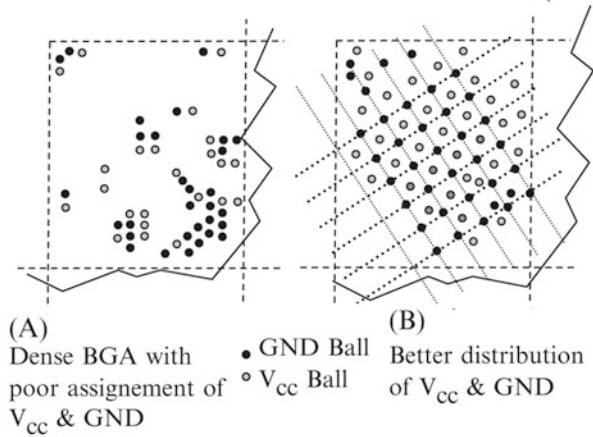
Figure 5.11, adapted from a remarkable experiment by H. Johnson [6], shows how critical for ground bounce the pin assignment can be with densely populated ICs. The test consists in switching simultaneously many outputs of 1,100 pins FPGA and monitoring one single inactive output, labeled as “victim.” One trial, rightfully designated as “the hammer,” is toggling 500 outputs at the same time. Although such test is forcing a rather extreme situation, it can be regarded as paramount for assessing the ability of a particular IC to noise generation. Two devices are compared: package A has 1,120 balls, with about 95  $V_{cc}$  pins and 95 Gnd pins, and package B has 1,148 balls, with 120  $V_{cc}$  pins and 200 Gnd pins.

With package A, although the total number of power pins (190) might seem sufficient, their pattern shows that they have been scattered more or less randomly, without apparent consideration in reducing the return loops areas. Some regions are “ground pins rich,” but other ones are void of ground pins. Package B shows a much better distribution of  $V_{cc}$  and Gnd, closer to a chessboard pattern: there are never more than 5 pin intervals between two Gnd or  $V_{cc}$ , and power pins are “paired” as often as possible. The measurement results speak for themselves: module A exhibits a 320 mVpeak (570 mVp-to-p) glitch on the victim output, that is almost five times more coupling than module B. There are several reasons for these poor results of device A:

- The Gnd and  $V_{cc}$  pins have been located with no attention to magnetic couplings.
- The number of Gnd +  $V_{cc}$  pins is 3.3 less than with package B.
- The culprits voltage rise in device A is 400 mV/0.5 ns, compared to 400 mV/ns with B.

Sometimes termed crosstalk, this problem is nothing other than the specific common impedance coupling that is addressed in this ground bounce section. Notice that the induced transients have the opposite sign with the culprit fronts, a clear indication that the coupling mechanism is magnetic. A similar problem, symmetrical to ground bounce, may take place on the  $V+$  distribution as well: during transitions, the steady “high” state of a given output may suffer a voltage dip because of the  $dI/dt$  demand of other gates sharing the same  $V_{cc}$  bus.

**Fig. 5.11** Ground bounce with high-density PGAs from two different sources (adapted from Johnson [6])



### 5.2.4 Low-Voltage Differential Logic, Benefits, and Problems

Low-voltage differential system (LVDS) drivers and receivers are deemed to reduce EMI problems, thanks to their smaller voltage excursion (typ. 0.3-0.5 V) and the symmetrical nature of the interface (see Chap. 2, Sect. 2.5).

Although the benefits are substantial for immunity to CM conducted and radiated interference, it may not be the same for radiated EMI and RF pollution in general, as explained next.

Let us consider two types of logic pulses train, using a same bit rate, hence same bit duration:

- Logic # 1 Unipolar pulse technology with amplitude  $A_1$  and rise time  $t_{r1}$
- Logic # 2 Differential technology with amplitude  $A_2$  and rise time  $t_{r2}$

Up to frequency:  $1/\pi\tau$ , the spectral amplitudes for these two digital pulses (see Chap. 3, Sect. 3.2) are:

- For signal  $S_1$ :  $2A_1 \tau$
- For signal  $S_2$ :  $2A_2 \tau$

Of course, the spectral amplitude of  $S_2$  is  $<$  spectral amplitude of  $S_1$ . However, at the second-corner frequency of signal  $S_2$ ,  $F_2: 1/\pi t_{r2}$ , we can calculate the spectral amplitudes of the two pulses:

- Spectral amplitude for  $S_1$ :  $2A_1 t_{r1} [(1/\pi t_{r1})/(1/\pi t_{r2})]^2 = 2A_1 (t_{r2})^2/t_{r1}$
- For  $S_2$ :  $2A_2 \times (t_{r2})$

This reflects the fact that spectrum of  $S_1$  is already falling off like  $1/F^2$ , while  $S_2$  spectrum is only decreasing like  $1/F$ , as visible on Fig. 5.12. Therefore, we can sort out three categories:

1. **If  $A_2/t_{r2} < A_1/t_{r1}$**

The spectral amplitude of  $S_2$  will always be  $<$  spectrum of  $S_1$ , even beyond the second-corner frequency  $F_2$ . LVDS spectrum  $S_2$  will radiate less than  $S_1$  even in the higher frequencies.

2. **If  $A_2/t_{r2} > A_1/t_{r1}$**

Somewhere beyond the second-corner frequency  $F_2$ , the spectral amplitude of  $S_2$  will exceed that of  $S_1$ ; although of lesser amplitude, the potential risk for radiated EMI in the higher frequencies is greater with  $S_2$ , especially considering that field radiated by a loop increases with  $(F)^2$ .

1. **If  $A_2/t_{r2} = A_1/t_{r1}$**

This is the case where the two digital pulses have the same volt/ns slope, hence are potentially identical offenders for radiated EMI above frequency  $F_2$ . Only the size and configuration of the radiating elements (traces, wires) will make the difference.

**Numerical Example 5.2** Compare the spectral amplitudes for the following pulses, above their second-corner frequencies:

- $S_1$ : straight LVMOS nondifferential logic: 3.3 V/3 ns, pulse width: 20 ns
- $S_2$ : LVDS differential output: 0.5 V/0.3 ns, pulse width: 20 ns

**Solution** The second-corner frequency for pulse  $S_1$  is  $1/\pi t_{r1} = 106$  MHz

The second-corner frequency for pulse  $S_2$  is  $1/\pi t_{r2} = 1,060$  MHz

The amplitude of pulse  $S_2$  being much lower than  $S_1$ , one might expect that  $S_2$  will be less of an aggressor. Let us do the check described before

- $A_2/t_{r2} = 0.5 \text{ V}/0.3 \text{ ns} = 1.67 \text{ V/ns}$
- $A_1/t_{r1} = 3.3 \text{ V}/3 \text{ ns} = 1.1 \text{ V/ns}$

Thus, although having 6.6 times less amplitude, the  $S_2$  pulse has a higher volt/ns switching slope than  $S_1$ , so its spectrum is stretching farther in frequency, with a progressively higher amplitude than  $S_1$  spectrum (Fig. 5.12). The exact crossover ( $F_x$ ) where  $S_2$  spectrum begins overriding that of  $S_1$  can be found by calculating the frequency for which spectrum amplitudes of  $S_1$  and  $S_2$  become equal

$$F_x = \left(\frac{A_1}{A_2}\right) \times \frac{1}{\pi t_{r1}}$$

That is, for our example

$$F_x = (3.3/0.5)/(3\pi \times 10^{-9}) = 0.7 \times 10^9 \text{ or } 700 \text{ MHz}$$

The dashed area on Fig. 5.12 (bottom) shows that above 700 MHz the risk of EMI radiation by signal  $S_2$  pulse train can be higher than by  $S_1$ . Chapter 11 will analyze another inherent weakness of the LVDS: the imperfect symmetry of the up- and down-going fronts will hamper the dynamic balancing of the outputs.

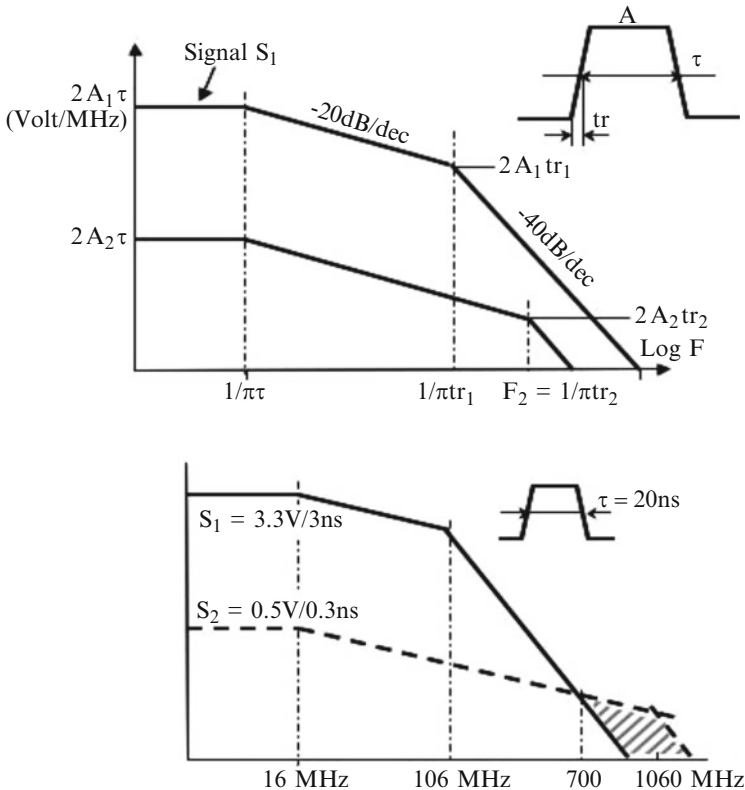


Fig. 5.12 Compared spectra of standard vs. LVDS logic outputs

### 5.3 CALCULATING THE IDEAL BYPASS CAPACITOR

Two things are important in delivering the necessary instantaneous currents while the device is switching:

- The proper capacitor value, which we will address here.
- The way this capacitor is mounted, which will be described in the next chapter.

This capacitor and its associated conductors play an important role in the radiation from the PCB elements. The so-called decoupling capacitor can be regarded as a reservoir providing the inrush current that the logic device needs to switch in the specified time. The reason for this is that the long wiring from the power supply regulator to the chip cannot deliver the peak current without excessive voltage drop. The value of the decoupling capacitor,  $C$ , associated to the logic chips requiring a given switching current is

$$C = I/(\Delta V/\Delta t) \quad (5.3)$$

where  $\Delta V$  = acceptable voltage drop at capacitor output ( $V_{cc}$  sag) caused by the demand of a current  $I$  during the time interval  $\Delta t$

$\Delta t$  = logic switching time  $\approx t_r$  (10-90%)

$I$  = total transient current demand of the logic family =  $I_1 + I_2$  (see Fig. 5.2a).

Table 5.2 lists values of  $C$  for some popular logic families, based on a maximum allowable  $V_{cc}$  drop equal to 25% of the noise immunity level. This comes from an equal spread of the PCB noise budget over four contributors: power distribution noise, radiation pickup, crosstalk, and mismatch reflections. Calculated value of  $C$  is for only one active device switching at a time and driving a fan-out of five gates. Several devices clocked in the same module will multiply the requirement for  $C$  by as many. Total current  $I_1 + I_2$  has been checked against the maximum current imposed by the gate output resistances of Table 5.1.

In the case of the standard (low-speed) CMOS, table value is conservative because the assumption that the power supply wiring cannot provide the peak current without excessive voltage drop is not true. For rise times in the 50 to 100 ns range, even with 1  $\mu\text{H}$  of  $V_{cc}$  lead inductance, the voltage drop would be acceptable. So unless severe ambient EMI is expected, this decoupling is not necessary, and one capacitor per row of modules is enough. Notice also that although presumably “quieter” than bipolars, high-speed CMOS still exhibits significant switching currents due to its fast transitions.

**Table 5.2** Decoupling capacitors needed for some popular logic

Logic family	Peak transient current requirements (mA)		Decoupling capacitor for a fan-out of 5 gates +10 cm trace length (pF)
	One gate overcurrent $I_1$ (mA)	One gate drive $I_2$ (mA)	
CMOS	1	0.5	(700)
HC	15	6	1,100
ACT	40	20	1,300
LS	6	2	1,700
FAST	15	4.5	1,700
AS	30	4.5	2,400
ECL	1	7	850

Some chips are more complex than a handful of gates. For instance, a dynamic 64 k RAM may need an extra current (above its normal consumption) of about 70 mA during a refresh cycle of 500 ns. To keep the supply rails within the desired voltage, tolerance requires 220-270 nF of buffer capacitance. For a 256 kRAM, 330-390 nF are required. The same is true for a microprocessor module which, too, requires about 220 nF (for a 16 bit device). Another example is the high-density pin grid array (PGA) modules with 128 pins or more. In such packages, it is common to find simultaneous switching of 16 or 32 bus driver outputs capable of driving 100 mA each, with rise times of 2 or 3 ns. This, plus all the internal functions of the module, requires more than 150 nF per module.

From Equ. (5.3) and accounting for the number of devices that are switching synchronously, a proper value of  $C$  is selected for each module. Generally, rounding up to the next standard value gives sufficient size. More is not necessarily better, and excessive capacitance on boards could, in turn, draw too much current when power is switched on, or when the card is hot plugged into its socket.

With the ever growing integration of more functions in a same IC, the instant need of many internal circuits switching at the same time creates a peak current demand that can reach several tens of amperes for a single chip. Although the duration of this peak is  $<1$  ns, no external capacitor, even close to the module, can deliver such current in a such short time. Just as a reminder: 1 amp/ns flowing in a 1 mm-thin wire causes 1 V of  $V_{cc}$  dip. So, an ultimate solution has been progressively adopted by the IC designers: incorporating the current storage (the decoupling capacitor), on the package substrate, or in the multilayer die itself. As early as 1990, some vendors started installing on-site chip decoupling by including a multilayer ceramic pellet in the substrate. Another technique [12] consists of using multilayer IC substrates where supply voltages and zero-volt returns are made by internal planes. Signals between the  $I/O$  pads and die are sandwiched between the Gnd and  $V_{cc}$  planes, as shown in Fig. 5.13.

When packaged in a logic array, this mounting allows voltage planes, signal layers, and several ground planes to be stacked with minimum intra-IC crosstalk supply and ground noises. Compared to the typical 5 nH of package inductance of a standard PGA, the total inductance is reduced to less than 100 pH.



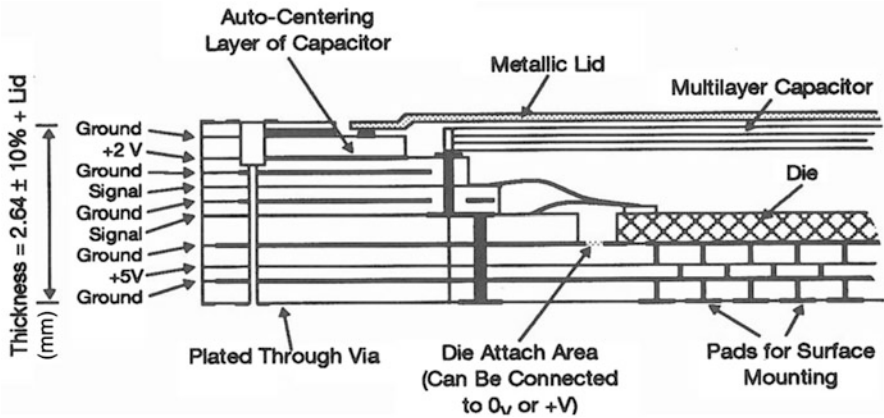


Fig. 5.13 An early version of large LCC module with internal decoupling capacitor and a multilayer stack of  $V_{cc}$ -0 V-signal planes [14]

For instance, with a device having 224 I/O pads, 8 bus drivers can switch 100 mA each in 3 ns, with less than 100 mV of common ground noise at the chip level. Of these 100 mV, only 20 mV are due to inductance, the rest being caused by the bonding wires and contacts dc resistances. No external decoupling capacitor is needed because it is built in. Chip-embedded capacitor values of several nF up to tens of nF can be obtained by providing thin oxide layer between metallized areas.

## 5.4 REDUCING EMI GENERATION AT THE IC ITSELF

Since the early 1990s several IC manufacturers who were aware of these problems have started incorporating EMC in the design of their chips. This includes geometrical improvements to reduce radiating loops areas and parasitic inductances, and voltage or current control to reduce the emission spectra. These efforts are supported and documented by now-standard methods for the characterization of chip emissions. Efficient software tools, like IC-EMC [11], are available to the IC designers. This “EMC-on-the-chip” approach is somewhat remindful of those (not-so-old) days where EMC engineers had to struggle for convincing the designers to apply EMI analysis to their PCB.

### 5.4.1 EMI Quiet Microprocessors and Fast ICs

Microprocessors, being the heart of a majority of functions and using the fastest clock frequency, can often be regarded as one prime excitation source throughout the equipment.

This can be true for Flash memories as well. Eventually, a point can be reached where all efforts in reducing PC board radiation will stumble on some uncompressible value: the field radiated by the processor module itself.

Many EMI reduction techniques are currently applied inside the IC:

- Reducing the peak current demands from the internal signal bus buffers.
- Improving the on-chip power supply distribution layout to the CPU core, ROM, RAM, data and address, oscillator, etc. to reduce ripple on the internal DC rail. This is made by wide, fingered  $V_{cc}$  and Gnd metallizations [7].
- Softening the 0-20% and 80-100% edges portions of the  $dV/dt$  transitions at the output stages, by using pre-drivers. This soft profile reduces the higher-frequency contents.
- Providing in situ diffused capacitors of  $\approx 1$  nF/mm<sup>2</sup>.
- Adding small value resistance (few ohms) or lossy ferrite material, for damping high-Q resonant effects between the on-chip capacitor and  $V_{cc}$  distribution inductance. These resonances appear typically in the 20-100 MHz range. The advantage of absorbing ferrite incorporated in the chip power lead [14] is the absence of power waste at DC or low frequency, while a 1 nH of lossy inductance will add 1  $\Omega$  of resistive loss at 150 MHz.
- Reducing loop areas in the die and the package.
- Increasing the number of  $V_{cc}$  and Gnd pads, with a more even spread.
- Die down mounting on the substrate.
- Using lower voltage excursions (low to high), like 1.5 or 2 V.
- Using on-chip canceling effects by opposing equal currents in adjacent  $V_{dd}$ - $V_{ss}$  loops.

### 5.4.2 Advantages with “3-D” Packaging

By stacking vertically several dies with planar decoupling capacitors between each level, substantial real-estate savings can be obtained, along with a proportional reduction of the  $V_{cc}$  and 0 V interconnects lengths, and less parasitic inductance for the decoupling capacitors (Fig. 5.14). This in turn results in less inductance and smaller loop areas for the switching currents paths inside the module. The internal capacitors between IC<sub>1</sub> and IC<sub>2</sub> result in a decrease of the peak current pulses drawn by the  $V_{cc}$ /Gnd pads off the PCB power distribution. In terms of signal loops, the internal connections can be shorter and more evenly spread than with a 2-D multi-chip module (MCM) having the same number of circuits.

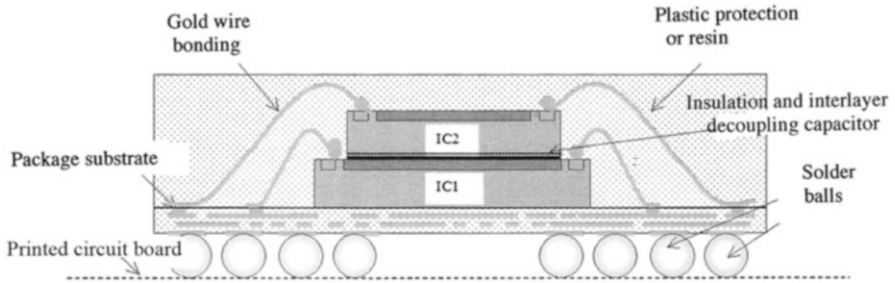


Fig. 5.14 Example of a 3-D “system-in-package” [12]

### 5.4.3 EMI Contribution of Clock Oscillators

High-frequency oscillators are serious players in radiated EMI, not just because they are the clocking master for all the fastest digital switching, but by the emission characteristics of the oscillator circuit itself [10].

CMOS gates are often used as amplifiers in their linear region, to build inexpensive oscillators. This may create large loops, whereas the current in the L-C tank formed by the crystal with its two associated capacitors is highly nonsinusoidal, hence rich in harmonics. It is better to use elementary gates, like HC-U family, with a drive capability and bandwidth limited to what is strictly necessary. If the oscillator is made from a 4 or 8 gate module, do not assign unused gates to other functions than clock distribution, since the corresponding IC will tend to be heavily polluted by CM voltages at clock harmonic frequencies.

Substantial EMI reduction can be obtained by using microprocessors with integrated PLL [2]. While standard oscillators run typically at two or four times the base system clock rate, a PLL-based oscillator can run at the system clock frequency. For instance, for generating a 4 MHz main clock, a 4 MHz PLL integrated in the processor is sufficient, instead of the 16 MHz external resonator which one would normally use. On a Texas TMS370 microcontroller, the radiated EMI above 30 MHz was typically 10 dB below that of a standard oscillator version.

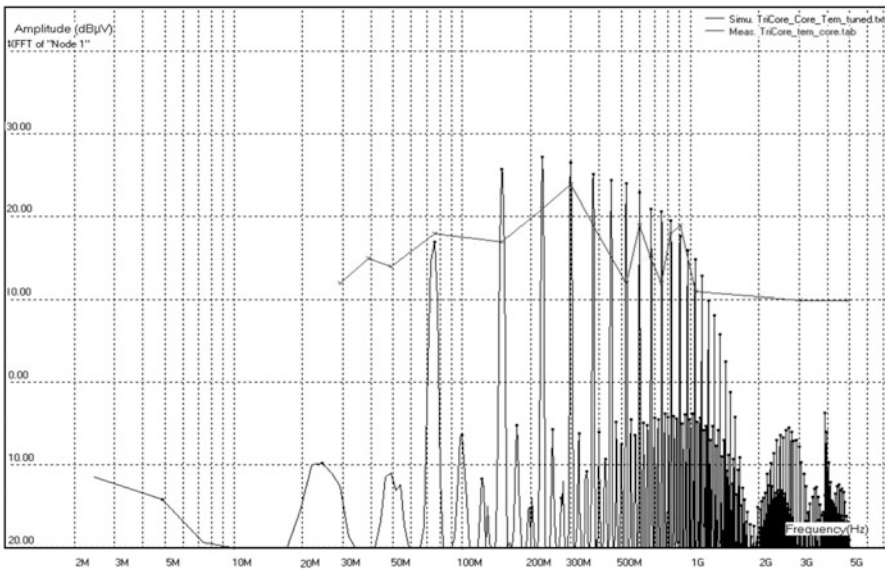
With critical applications like airborne/shipborne equipment or automotive electronics, a safe and simple precaution with fast clock is to select a base frequency whose fundamental and first harmonics do not fall into protected frequency bands, like FM radio, VHF navigation, GSM, GPS, etc.

### 5.4.4 Simulation Software for IC Emissions

Software packages are available that predict reasonably well the emissions from an IC. They can help the IC designer for optimizing its die floor plan, power and ground leads assignments, and so forth.

One of them, IC-EMC [11] is based on the WinSPICE version of the SPICE program. The freeware (downloadable from <http://www.ic-emc.org>) includes a schematic editor, interface to WinSPICE, and an electromagnetic solver for radiated emissions prediction. The software is using IC suppliers' component models like IBIS and combines them with best-fit equivalent circuits of the principal internal activities of the chip, using a set of current sources, internal decoupling caps, and R/L/C elements representing the die, bonding wires, and pads or balls.

The SPICE tool generates time or frequency plots of the conducted emissions on identified IC ports, like  $V_{dd}$  or  $V_{ss}$ . It is possible to integrate actual measured values-if available-in order to “fine-tune” the model for a better correlation. Then, the radiated emissions are computed by virtually installing the IC equivalent circuit in a simulated TEM cell, represented by a set of known coupling capacitance and coupling inductances. The results are displayed as  $\text{dB}\mu\text{V}$  on the  $50\ \Omega$  measuring port of the TEM cell, which can be kept as is, being a standard measurement practice, or translated approximately in actual radiated  $E$  field at 1 m. Figure 5.15 shows examples of simulation results. It is also a good illustration of what is theoretically described in Chap. 2 (Sect. 2.3.1, Equ. 2.18 or Fig. 2.6): the field radiated by a loop increases as  $(F)^2$ . Therefore, while conducted emission spectrum is constantly falling off with frequency, the radiated emission from the same device keeps increasing up to  $\approx 500\ \text{MHz}$ .



**Fig. 5.15** Example of emission spectrum obtained by the IC-EMC software [11]. Discrete frequencies are simulation results. *Solid line* is the envelope of actual TEM measurements for the same IC. Vertical scale:  $\text{dB}\mu\text{V}$  readings at the TEM cell port

## 5.5 STANDARD METHODS FOR IC EMISSIONS MEASUREMENTS

With the growing need for “quieter” ICs, standard methods of measurements become necessary for characterizing and comparing the EMI signatures of various devices, or similar devices from different sources. Even a minor change in the production masks or manufacturing process may cause significant changes in the emission level of a same  $P/N$ , from the same supplier.

Characterization methods belong to two general categories: conducted and radiated. Since one has to make sure that the measured emissions are coming from the sole IC and not from the test circuit, all methods impose a precise standard test jig: 4-layer PCB with integral ground plane,  $I/O$  lines treated as microstrip or striplines, coaxial fittings and impedance matching for the whole test gear, etc.

***IC-Conducted Emissions Measurements:*** Several techniques are proposed, which are generally studied by the IEC Technical Committee 47A and ultimately released in the subsequent IEC 61967-xx series:

(a) The RF current and voltage method (IEC 61967-4)

The principle is shown on Figs. 5.16 and 5.17. The IC under test and its associated loads and controls are connected to the ground plane via  $1\ \Omega$  noninductive resistors. The RF current waveforms and/or spectrum are derived from the voltage measured across each  $1\ \Omega$  shunt. The shunt in the IC ground common lead displays the instantaneous power supply “through current,” when the entire device is operating. The  $1\ \Omega$  resistors in each load ground lead(s) give the characteristics of each individual output current. These current measurements are complemented by voltage waveforms and spectra, the  $I/O$  pins being loaded by  $150\ \Omega$  (or other) resistors. The standard describes a set of templates with a 3-digit coding (for instance, B-4-F), corresponding to the three slopes: flat,  $1/F$ , and  $1/F^2$ , of the overall spectrum envelope. The problem is that the template scale corresponds to extremely low amplitudes, quite unrealistic when toggle frequencies are exceeding few MHz. Yet, the principle is valid.

(b) The workbench Faraday cage (Philips Co., [1] and IEC 61967-5)

The IC, mounted on its test board, is located in a small Faraday box. All  $I/O$  leads are fed through the box wall via coaxial connectors and loaded with  $150\ \Omega$  to ground. These  $150\ \Omega$  are deemed to represent the average CM impedance of the  $I/O$  cables in the final applications of the device.

***IC-Radiated Emission Measurements:*** In its simplest form, the method is using a miniature  $H$ -field loop, like a shielded 5 mm-diameter loop, probing just above the IC in various orientations (see, for instance, the measurements in Fig. 5.7). The more elaborate method of SAE J1752-3 or IEC 61967-2 places the test board on top of a miniature TEM cell, with the IC looking down through a square aperture in the top plate (Figs. 5.16 and 5.17). The power measured at the cell output port is converted in form of magnetic loop and electric dipole moments ( $\mu\text{A}\cdot\text{cm}^2$  and  $\mu\text{A}\cdot\text{cm}$ ), such as the  $E$  and  $H$  fields at any distance  $D$  can be derived. A coarse but practical correlation consists in using  $V_{50}$ , the output voltage into

50  $\Omega$ , to compute the total IC-radiated power ( $P_{\text{rad}}$ ), and then translates it into an equivalent-radiated field:

$$E = \left( \sqrt{30 \cdot P_{\text{rad}}} \right) / D = \sqrt{(30 \times 2 \times V_{50}^2 / 50)} / D \quad (5.4)$$

So,  $E$  (dB $\mu$ V/m) @ 1 m  $\approx V_{50}$  (dB $\mu$ V)

In many cases, the 30-300 MHz correlation is rather close such as plots of  $V_{50}$ (dB $\mu$ V) and actual one-meter measurements of  $E$ (dB $\mu$ V/m) are overlaying within +/- 3 dB.

The method is sensitive to the IC placement vs. the cell axis, and directional effects are noted when the IC is rotated 180°, since magnetic and electric moments are combining differently (the highest reading must be retained). Notice that the IC under test is mounted on the quasi-perfect ground plane of the test PCB that is itself part of the TEM “ceiling.” Thus, the radiated emissions results can be extrapolated to an actual equipment application only to the extent that the host PCB would be itself a perfect plane.

The standard miniature TEM cell has an upper frequency limit of 1 GHz. An improved test tool, the GTEM cell can be used up to 18 GHz. The principle is similar, but the cell is a tapered line, with the 50  $\Omega$  measuring port at the narrow end and an RF absorber at the opposite end. The IEC document is suggesting emissions classes that allow the designer to anticipate the amount of EMI suppression hardware he may have to consider, if he intends to use a particular IC. Categories are displayed as received levels at the 50  $\Omega$  output of the TEM cell:

Class	Maximum TEM voltage, 0.1-1,000 MHz (dB $\mu$ V)
1	10
2	20
3	30
4	40

For instance, an IC that complies with level #1 can be used in confidence without any additional suppression hardware, even in the most strict applications like automotive or military aircraft electronics. In contrast, an IC that just meet, or exceeds, level #4 will require a considerable suppression effort in additional filtering, PCB layout and eventually a dedicated compartment shield on the PCB.

**Summary Review of IC/EMC Test Methods:** Existing conducted methods can provide a detailed profile of each pin contribution, allowing fine investigations of a specific device’s output. They have some basic limitations:

- These standard methods imply that conducted measurements up to 1 GHz can be sufficient for characterizing emission properties, that is questionable (as of 2010, processors with >1,000 MHz base clock are common place).
- Accordingly, they are based on the assumption that direct radiation from the IC alone is not a problem and that only its conducted emissions are of importance.

In contrast, the radiated method has the advantage of gathering the full radiated power of the IC. Yet, it does not permit detailed investigation of each pin, although it is always possible to enhance or inhibit a specific function from the test board interface.

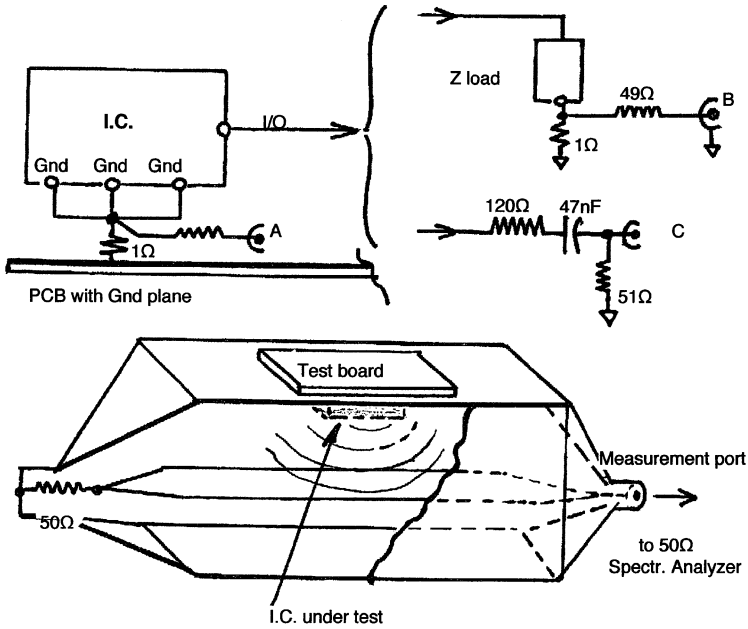


Fig. 5.16 Standard emission test configuration for ICs

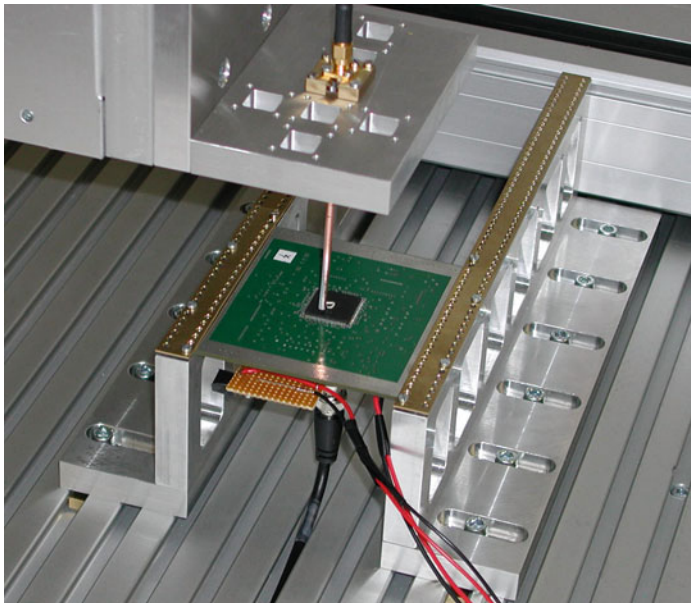
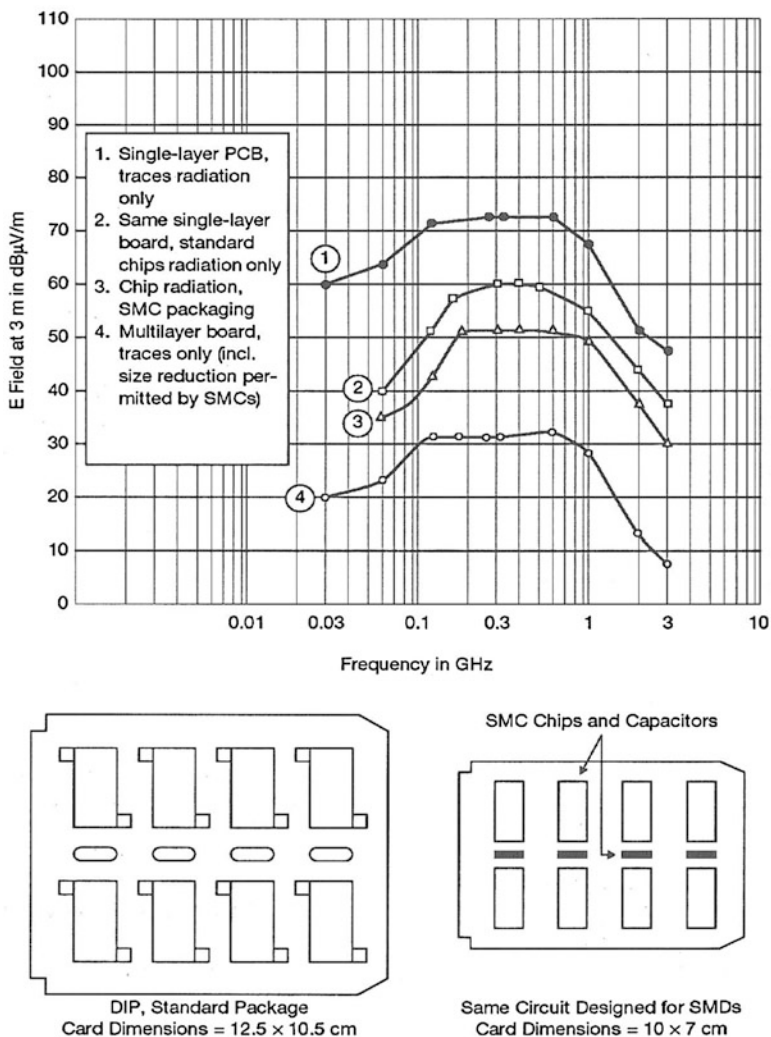


Fig. 5.17 Near-H-field scanner using a miniature field probe and precision X-Y table (IC-EMC User's Manual, [11])

## 5.6 INFLUENCE OF THE IC PACKAGE ON RADIATED EMISSIONS

Although it may seem minuscule, the loop surface made of the chip, its bonding wires, and the module leads can become a significant EMI contributor in heavily populated cards, especially when multilayer boards are used. This is because, with

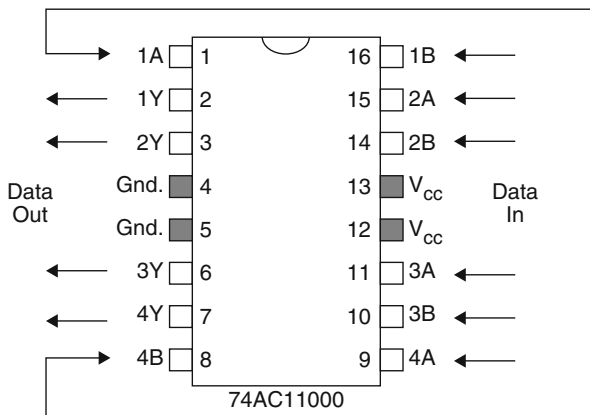


**Fig. 5.18** Radiated field comparison of a single-layer PCB (no ground plane) with DIP devices vs. the same board redesigned as a multilayer with surface-mount components. All modules have the same number of gates, switching 3 V/3 ns at 30 MHz clock rate



multilayer boards, the trace radiating loops become so small that IC leads become the largest antennas. In this respect, the worst of all packages is the standard DIP, especially if mounted on an elevated socket.

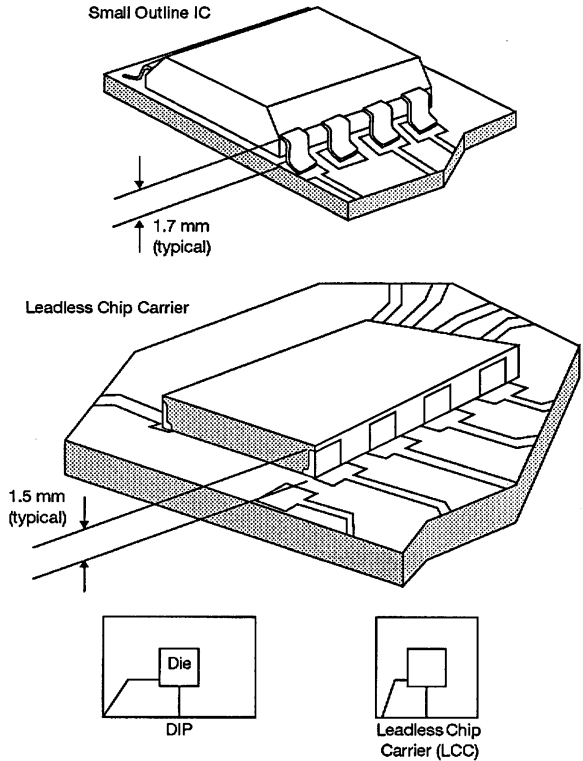
In Fig. 5.18, we see that the sole DIP’s radiation, for instance, is only 20-12 dB below the traces’ radiation. Flat packs with gull wing leads represent a first step in loop area reduction. A further improvement is found with the center  $V_{cc}$  and ground pin layout provided by some IC manufacturers (Fig. 5.19). Although this pin arrangement was designed primarily to reduce  $V_{cc}$  and ground voltage “bounce” thanks to a lower inductance, it also has a beneficial feature in reducing the worst-case loop area.



**Fig. 5.19** TI AC MOS use a flow-through architecture that places Gnd and  $V_{cc}$  pins in the center rather than the usual end-pin location. This allows quieter simultaneous switching, eases board layout, and saves board real estate. For a typical fast transition, the noise glitches on the device’s power distribution are down from about 2 to 0.4 V (Reprinted with permission from TI Tech. Note)

Finally, surface-mount components (SMCs), also known as surface-mount devices (SMDs) and surface-mount technology (SMT), achieve the best possible area reduction, as they exhibit about 40% reduction in component dimensions and, therefore, a 64% area reduction of the module radiating loop (see Fig. 5.20). In addition, they allow a significant reduction in board size and, therefore, in trace radiation. In Fig. 5.18, we see the decrease in radiation when changing (everything else being the same) to multilayer board and SMC. Common characteristics of the PCBs in Fig. 5.18 include eight 16-pin chips, six clocked gates per chip, clock frequency of 30 MHz, and a clock edge of 3 V/3 ns. Multilayer technology reduces trace-only radiation by 40 dB. SMC devices further reduce chip radiation by 6-8 dB. Notice, though, that module radiation now dominates trace radiation. An interesting side benefit of selecting low-profile, low-area packages is that the decoupling capacitor-to-chip loop area will also be reduced.

**Fig. 5.20** Loop reduction by SMT packaging. The 2:1 reduction in pin-to-chip trace area reduces radiated emissions and susceptibility



Number of Leads	Longest LCC Trace Longest DIP Trace	Longest Trace Shortest Trace	
		LCC	DIP
18	0.5	1.5/1	2.6/1
24	0.25	1.5/1	3/1
64	0.17	1.5/1	7/1

## 5.7 SHIELDING AT THE IC LEVEL

The traditional shielding method consists in enclosing the entire equipment or PC boards in a conductive envelope (see Chap. 10), since the printed traces and internal wiring are the dominant radiating antennas, inside the unit. However, with the increasing use of large-size ICs and MCM, there are cases where a perfect EMI suppression at PCB traces will still leave intact the radiation of the IC itself, which alone may approach or exceed the specification limit.

Another situation arises with the increasing number of mass-produced small devices combining data processing, RF communications, and audio/video functions: mobile phones, smartphones, MP3, tablets, GPS navigators, etc. These products often have a common particularity: on few cm<sup>2</sup> of a same PCB, they gather in close proximity components as various as:

- Authorized RF sources: 435 MHz wireless remote controls, 950/1,800 MHz GSM transmitter, Bluetooth transmitter, etc. with RF power ranging from 10 mW to 2 W, that is 10 to 33 dBm
- High-speed logics with clocks >100 MHz
- Sensitive RF receivers, with detection sensitivities as low as -100 dBm (cell phones) down to -140 dBm (GPS)

This can translate as bulk source-to-victim power ratio of approximately 110-173 dB, without any margin. Even though several isolation factors will exist between the aggressor and its victim, physical distance, frequency channel separation, out-of-band rejection, coding/decoding protection, etc., it is sometimes impossible to reach such degree of attenuation without turning to shielding the source IC, the receptor IC, or both.

If only one or few chips are responsible for the specification violation or are causing internal EMI (self-jamming), while the rest of the packaging has been adequately treated, it might be economically justified to shield the IC only. Figure 5.21, from [4] shows some existing off-the-shelf, standard-sizes, or custom-drawn board level shields. Heights as low as 1.5 mm above PCB surface are obtainable. One mounting option is to ground the 5-sided can by soldering its “picket fence” to the vias on the shield perimeter, such that the PCB internal Gnd plane is acting as the sixth side of the Faraday cage. This allows eventually surface traces to get in/out the shielded IC. Much better solution is to have a continuous solder belt around the shield footprint and entering/exiting the covered IC only via buried traces.

Another or complementary solution for reducing the emission right at the source is to stick a small lossy ferrite plate, acting as a noise absorber on top of the noisy IC [13].

Both approaches-shield or ferrite-have hard-to-predict performances. Being in the extreme near field of the source chip, the efficiency is strongly dependent on the actual radiating source impedance and distance to the shield. Shielding factors of 10-40 dB are obtainable, but the user must be cautious with performances derived from one-meter-distance tests, since they do not reflect the actual application.

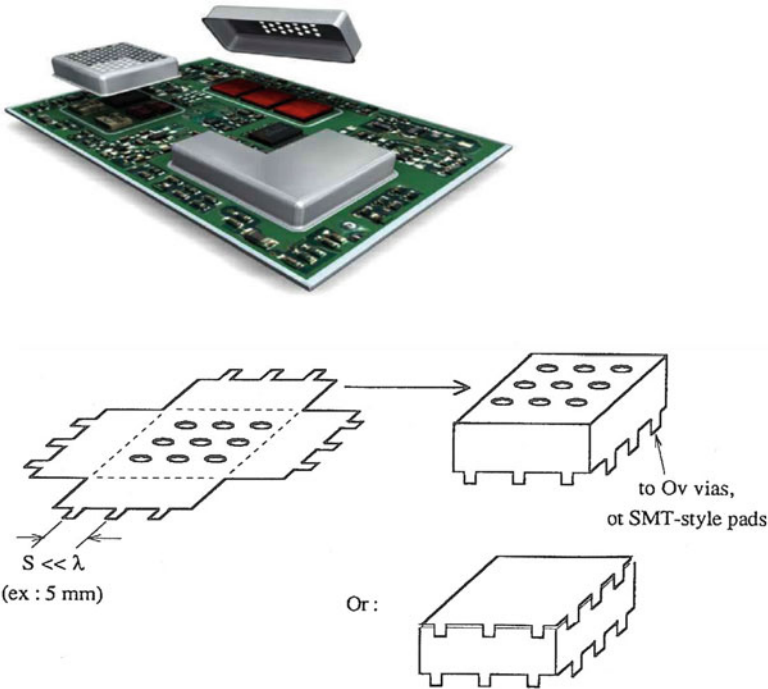


Fig. 5.21 Partial shielding at the IC/module level

## 5.8 SUMMARY OF RADIATION CONTROL HINTS AT THE CHIP AND IC LEVEL

- Among the viable technologies to perform a given function, try to select the ones that are less “current hungry” at transitions; average power consumption is meaningless in this regard: transient current demand is what counts.
- Reserve fast switching technologies ( $t_r, t_f < 7$  ns) for functions where such fast transitions are truly vital.
- Select package styles with minimal loop areas and optimized  $V_{cc}/Gnd$  pins location. Twenty-five DIP modules easily add up to  $10 \text{ cm}^2$  of radiating area (about  $2.5 \text{ cm}^2$  with SMT)
- Use metal-enclosed modules (if cost permits) and connect the can to the ground plane.
- When defining ASICs, specify output devices with the lowest driving capability suitable for the application: do not oversize.

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# Chapter 6

## Printed Circuit Board Design

Other than choosing component technologies and packages that offer lower radiation levels, the designer has very few EMI reduction options at the device level. In contrast, the PCB, as a building block, offers the first area in which a strong design action is possible. A multitude of EMC “war stories” arrive at the inevitable conclusion that an in-depth look at PCB design would have saved thousands of dollars in testing, last minute fixes, and retesting, plus additional hundreds of dollars per unit, in hardware costs for shielding, gasketing, and so forth.

Not only is the PCB a radiating element by itself, but insufficient attention to board-level EMI can result in noise coupling to I/O lines and other external elements. These, in turn, carry the undesired signals away and radiate them. There are many cases where a handful of three-cent surface-mount capacitors and a cost-free rerouting of few traces will eliminate the need for expensive shields and filters. Once the technical aspects of the board’s radiation are understood, another stumbling block often appears: the computer-aided design (CAD) package for traces routing. Such programs often ignore EMI aspects and require manual data reentry.

### 6.1 BOARD ZONING

Circuit boards, especially single-layer ones, should be laid out such that the higher frequency devices (e.g., fast logic, clock oscillators, bus drivers) are located in the edge connectors area, as illustrated in Fig. 6.1. Although other arrangements can be advocated with good results, this one is a trade-off for the lesser of several evils: radiating loops made by trace-to-edge connector pins, back and forth, are among the most offending ones in a PCB, so they are kept short for the faster logic. High  $dI/dt$  return currents paths, causing common-mode voltages along ground conductors, are also kept short.

The lower speed logic and memory can be located farthest from the connector because they tolerate longer trace lengths without the proclivity for radiation, ground noise, and crosstalk. Opto-isolators, signal isolation transformers, and signal filters should be located as close to the edge connector as possible to avoid crosstalk between undesired signals and the “clean” side of these isolators.

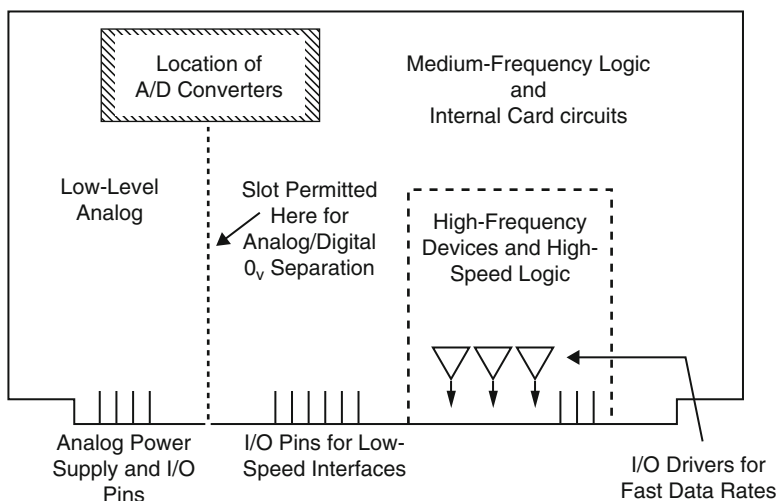


Fig. 6.1 Applying board zoning guidelines

## 6.2 BRUSHUP ON SELF-INDUCTANCE OF CONDUCTORS AND PLANES

Any conductor, in addition to its ohmic resistance, exhibits self-inductance. Although such a blunt statement may seem trivial in a book written for electronic engineers, the author has seen so many instances where self-inductance was misunderstood, that a short brushup may be useful.

### 6.2.1 Inductance and Impedance of Wires and Traces

The term self-induction defines the counter electromotive force caused by the magnetic field around a wire, when the current is changing rapidly. Strictly speaking, self-inductance can only be calculated precisely if the two-way path of the current is known. For such “hairpin” shape, the total self-inductance is

$$L = 0.4 \ln(2h/d) \mu\text{H/m} \quad (6.1)$$

where  $h$  is the wire separation and  $d$  the wire diameter.

If half of the total loop inductance is attributed to one of the wires, this “partial” inductance becomes

$$L = 0.2 \ln(2h/d) \mu\text{H}/\text{m} \quad (6.2)$$

Notice that this one-wire self-inductance can only be determined if one knows where the other wire is. However, to simplify calculations, one may consider a practical worst case for one wire [9, 12]. This is the value reached when the other wire is very far away; practically, an asymptotic value called “free-space” inductance is reached when the separation  $h$  becomes greater than the length  $l$  of the conductor pair. This worst-case value is

$$\begin{aligned} L_{(1\text{-wire})} &\approx 1.5 \mu\text{H}/\text{m} \text{ for a round wire} \\ &\approx 1 \mu\text{H}/\text{m}, \text{ or } 10 \text{ nH}/\text{cm}, \text{ for a trace} \end{aligned}$$

This is the default value we will be using when a PCB trace is far from the one carrying the opposite current. The table in Fig. 6.2 shows more precisely calculated impedances, including the slight variations brought by various trace widths. No values are given for lengths  $\geq \lambda/4$ , whereas a trace can no longer be seen as single resistance and inductance, but as a transmission line with distributed  $L, C$  parameters.

## 6.2.2 Inductance and Impedance of Planes

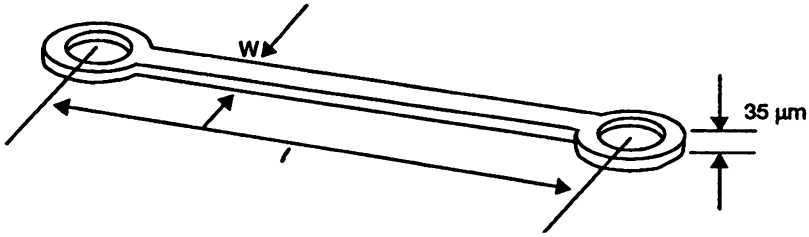
By comparison, Fig. 6.2 shows also the impedance curve for a perfect, infinite copper plane. Such an ideal plane has no self-inductance, since no magnetic field lines can close around the conductor: it only exhibits resistance, skin effect, and a very small internal inductance, within the metal. These increase only like the square root of frequency once the metal thickness exceeds the skin depth region. This is an advantage over wire or trace impedance that increases like frequency. For example, at 100 MHz (the equivalent bandwidth for a 3.5 ns rise time), a wide plane shows only 3.7 m $\Omega$ /sq: the switching of 30 mA will cause only 100  $\mu$ V voltage drop along the common ground, regardless of the path length.

Unfortunately, quasi-infinite 0 V (or  $V_{cc}$ ) planes seldom exist in practice. Actual ground planes are finite, and current distribution across their width is not uniform. Cross section in Fig. 6.3 shows the return current spreading in the extended “shade” of the overhead trace, a gross rule-of-thumb being that approximately 90% of the return current is found in a width equal to  $10 \times h$ . This, alone, corresponds to a strangled path which is no longer a surface impedance in  $\Omega$ /sq but a linear impedance in  $\Omega$ /cm. In addition to this, the last few percent of current reaching the edges corresponds to the actual closure of the magnetic field lines around the finite plane, which is a self-inductance [4, 9]. A close approximation to this partial inductance of a finite plane having a width “ $w$ ” is given by

$$L_{\text{plane}}(\text{nH}/\text{cm}) < 5 h/w \quad (6.3)$$



**a Impedance of PCB Traces**



ℓ =	Impedance										
	W = 0.16 mm				W = 1 mm				W = 3 mm		
	1 cm	3 cm	10 cm	30 cm	1 cm	3 cm	10 cm	30 cm	3 cm	10 cm	30 cm
DC 50 Hz											
To 1 kHz	36 mΩ	106 mΩ	360 mΩ	1.07 Ω	5.7 mΩ	17 mΩ	57 mΩ	170 mΩ	5.7 mΩ	19 mΩ	57 mΩ
10 kHz	36 mΩ	106 mΩ	360 mΩ	1.07 Ω	5.75 mΩ	17.3 mΩ	58 mΩ	175 mΩ	5.9 mΩ	20 mΩ	61 mΩ
100 kHz	37 mΩ	108 mΩ	370 mΩ	1.12 Ω	7.2 mΩ	24 mΩ	92 mΩ	310 mΩ	14 mΩ	62 mΩ	225 mΩ
300 kHz	40 mΩ	123 mΩ	456 mΩ	1.44 Ω	14.3 mΩ	54 mΩ	225 mΩ	800 mΩ	40 mΩ	175 mΩ	660 mΩ
1 MHz	70 mΩ	230 mΩ	1 Ω	3.4 Ω	44 mΩ	173 mΩ	730 mΩ	2.6 Ω	0.13 Ω	0.59 Ω	2.2 Ω
3 MHz	0.2 Ω	0.7 Ω	3 Ω	10.2 Ω	0.13 Ω	0.52 Ω	2.17 Ω	7.8 Ω	0.39 Ω	1.75 Ω	6.5 Ω
10 MHz	0.7 Ω	2.3 Ω	9.3 Ω	32 Ω	0.44 Ω	1.7 Ω	7.3 Ω	26 Ω	1.3 Ω	5.9 Ω	22 Ω
30 MHz	2.2 Ω	7 Ω	30 Ω	102 Ω	1.3 Ω	5.2 Ω	21.7 Ω	78 Ω	3.9 Ω	17.5 Ω	65 Ω
100 MHz	7 Ω	23 Ω	93 Ω	320 Ω	4.4 Ω	17 Ω	73 Ω	260 Ω	13 Ω	59 Ω	220 Ω
300 MHz	22 Ω	70 Ω	300 Ω		13 Ω	52 Ω	217 Ω		39 Ω	175 Ω	
1 GHz	70 Ω	230 Ω			44 Ω	170 Ω			130 Ω		

**b Impedance of Copper Planes**

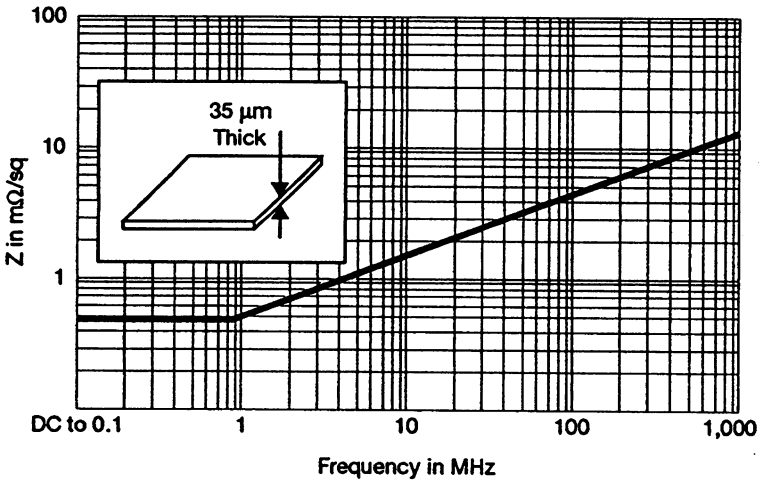


Fig. 6.2 Impedance comparison of printed circuit power distribution traces and planes. (a) Impedance of PCB traces, (b) impedance of copper planes

Notice how interesting the concept of partial inductance is: once the  $h$ ,  $d$ , and  $w$  geometry is set, one can calculate trace impedance regardless of the plane width, and vice versa, plane impedance regardless of the trace width. Summarizing these issues, Fig. 6.4 shows, for a same 10 cm path length, a comparison between:

- 1 mm-wide, isolated trace, typical of a single-layer board with  $V_{cc}$  and ground far apart
- The same trace, 1.6 mm above a ground plane ( $V_{cc}$  trace for instance)
- A gridded ground with 5 mm mesh size ( $\approx 3$  nH)
- A perforated ground plane with 1 mm circular holes (1.25 mm center to center)
- A plain copper plane 35  $\mu\text{m}$  (1 oz) thick, 10 cm wide (partial inductance  $\approx 0.6$  nH)
- A theoretical infinite plane

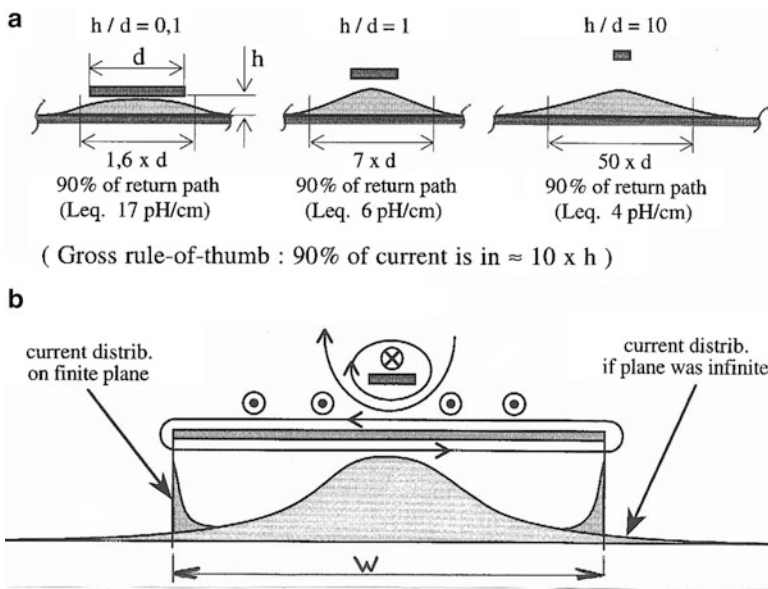


Fig. 6.3 (a) Actual return current density with finite planes [from 4, 9]. (b) Ground planes are finite

**Example 6.1** From Fig. 6.4, calculate the ground longitudinal voltage noise for the following case and different options for return path. We are looking at Harmonic #3 current from a 50 MHz clock signal, 10 cm path length, assuming a fundamental current amplitude of 15 mA:

Harmonic #3 amplitude: 15/3 = 5 mA	Impedance at 150 MHz	$\Delta V$
(a) Return path via thin ground trace (curve A)	105 $\Omega$	$\approx 0.5$ V
(b) Return path via a perfect ground plane (curve F)	5 m $\Omega$	25 $\mu\text{V}$
(c) Return path via 10 cm-wide perforated plane (curve D)	450 m $\Omega$	2.2 mV

It is clear that, although having a hundred times larger impedance than an ideal plane, the perforated finite plane is two hundred times less noisy than the isolated trace.

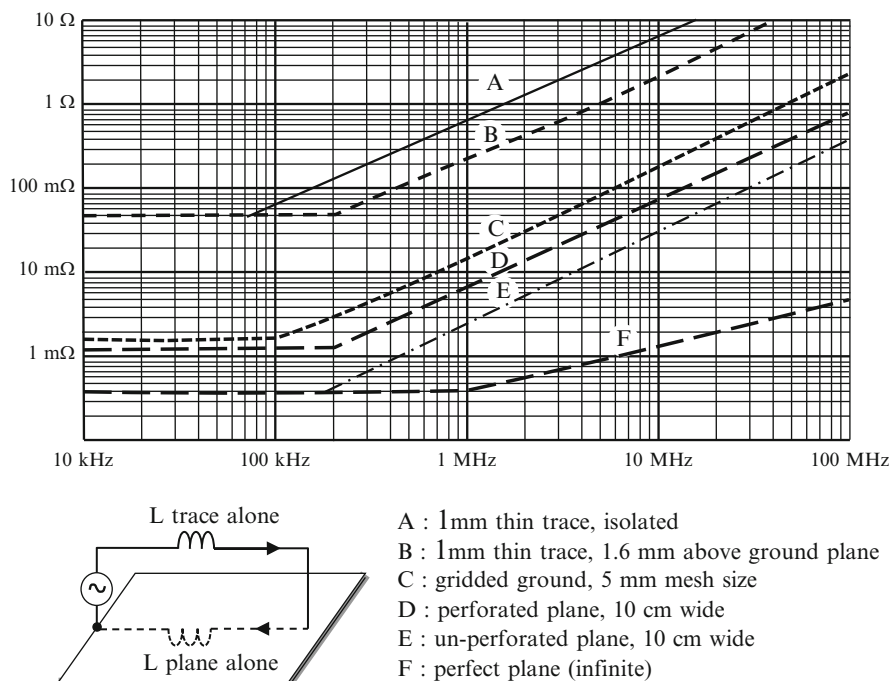


Fig. 6.4 Partial impedance of several traces and planes for a same 10 cm path length

### 6.2.3 Parasitic Radiation by a Finite PCB Ground Plane

Although it can be thought of as a perfect, zero-impedance area, we have seen that a PCB power plane (Gnd or  $V_{cc}$ ) represents some impedance, especially when perforated by via holes. The small longitudinal voltages resulting from the  $Z \times I$  drop of all the signal and power distribution currents are able to generate a capacitive (displacement) current (Fig. 6.5), turning the PCB plane into an electrically excited dipole [5, 7]. This CM radiation mechanism is independent from the DM radiation of the trace-to-Gnd loops. We already described it as one of the causes for CM radiation of I/O cables, but this time we are addressing the case where the PCB plane itself radiates, even without the enhancement by the I/O cables.

The radiation efficiency of this “plate” dipole can be estimated by an approach similar to that of the voltage-driven, open wire of Chap. 2, Fig. 2.14. Once the longitudinal voltage has been computed for a given Gnd (or  $V_{cc}$ ) plane, a quick estimate of the  $E$  field at distance  $D$ , for far-field conditions, can be made as follows.

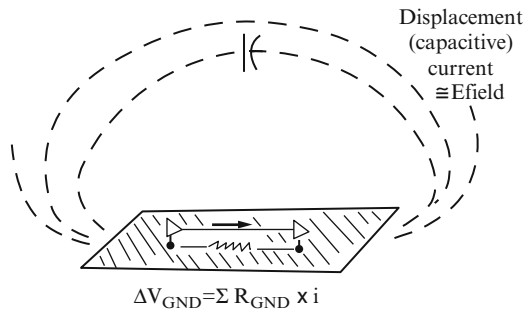
Based on the free-space capacitance of a plate:

$$C_p \approx 40 \text{ pF} \sqrt{A(\text{m}^2)}$$

the  $E$  field is given by

$$E \text{ (}\mu\text{V/m)} = \left( V \cdot 40\sqrt{A} \right) \ell(\text{m}) F^2(\text{MHz}) / D \tag{6.3a}$$

with  $A$  the area of the plane in  $\text{m}^2 = \ell(\text{m}) \times w(\text{m})$ , provided that  $\ell$  and  $w$  are  $\leq \lambda/2$  and  $D$  the measuring distance, should be  $\geq 48/F$  (MHz), for far-field conditions.



**Fig. 6.5** Conceptual view of a ground plane acting as a radiating dipole

**Follow-Up of Example 6.1** Let us take a PCB with  $\ell = 0.25$  m and  $w = 0.10$  m. The Gnd plane noise at 150 MHz is 2.2 mV, caused by the third harmonic of a 50 MHz clock (Example 6.1). Estimate the radiated  $E$  field at 3 m distance, due to this sole Gnd plane noise. Per Eq. (6.3a),

$$\begin{aligned} E \text{ (}\mu\text{V/m)} &= 1/3 \left[ V \left( 40\sqrt{0.25 \times 0.10} \right) \right] 0.25 \text{ m} \cdot (150)^2 \\ &= 12,000 \mu\text{V/m for 1 V drive,} \\ &\text{or } 12 \mu\text{V/m (22 dB}\mu\text{V/m) per mV of drive} \end{aligned}$$

Notice that the (bracket) term results in a capacitance of 6.3 pF for the plate.

Our 2.2 mV PCB ground noise will cause  $2.2 \times 12 \mu\text{V/m}$ , that is,  $26 \mu\text{V/m}$  (28.5 dB $\mu\text{V/m}$ ). This is 14 dB below FCC Class B limit of 43 dB $\mu\text{V/m}$ ; therefore, a Gnd noise of 11 mV would make the power plane radiation alone reaching Class B. At 300 MHz, this threshold would reduce to 4 mV, for a 46 dB $\mu\text{V/m}$  limit.

Except from shielding the entire product or subassembly, the only solution against such sly, hard-to-find source of radiation is a better control of the current paths and impedances in the common Gnd and  $V_{cc}$  planes, like

- Use of blind vias (semi-vias where possible) for traces that are not connected to Gnd.
- Decoupling  $V_{cc}$  to Gnd close from the chip current demand.
- When capacitive filters are used for signals, put the capacitor close to the source side, rather than load side, and lower the capacitive current by adding a series resistor or ferrite upfront.

### 6.3 SINGLE-LAYER, ONE- AND TWO-SIDED BOARDS

Under this term, we mean single-layer, one-sided boards where only one side is copper coated as well as single-layer, two-sided PCBs with copper on both sides. Less expensive to produce and sometimes made of cheap phenolic substrate, they demand more precautions in controlling EMI (and radiated EMI in particular) because loop sizes are necessarily larger in all circumstances. This is true for the decoupling capacitor loop, the  $V_{cc}$ -to-Gnd trace separation, and the signal trace-to-Gnd trace loops. Thus, single-layer PCBs are only acceptable for circuits whose basic operating frequencies do not exceed  $\approx 1$  MHz. But although multilayer boards have progressively outranked the single-layer ones, these latter continue to be preferred and used in mass-produced consumer devices, for cost reasons. There are cases where even an extra-cost as small as \$0.1-0.3 per board is unaffordable when quantities like 100,000 parts/year or more are the rule. The following recommendations are meant for accommodating such situations [10].

#### 6.3.1 Power Supply Distribution and Decoupling with Single Layers

Power distribution on single-layer boards is traditionally provided by supply and return traces. Their impedance (inductive reactance) is unimportant for low-speed and/or low-power logic families such as ordinary CMOS (e.g., #4700 series). The need for capacitor decoupling is only of one for every row of five or ten modules, plus one at the connector input. As the logic speed increases, considerably more care in layout is required due to increased trace impedance. High-frequency ceramic disc caps come to the rescue here, with one typically used to serve several modules, but precautions must be taken to ensure that the capacitor works properly at the highest frequencies.

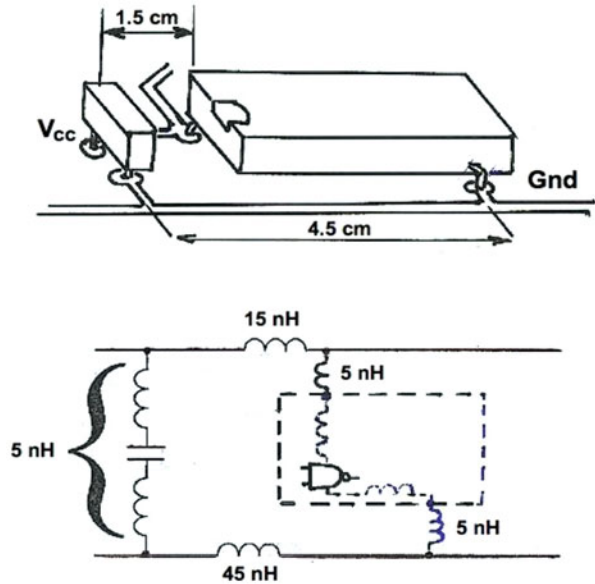
Figure 6.6 shows a layout of power supply and return traces which are too far apart and therefore a poor design practice. The problem, as shown in the equivalent circuit, results in an inductance of about 5 nH for the capacitor leads (assuming they are cut very short) between the 5 V and ground traces and  $2 \times 5$  nH for the DIP pin leads, outside the package itself. For a trace supply and return totaling 6 cm, the traces inductance is about 60 nH; therefore, a total loop inductance of

$$60 + 5 + 10 = 75 \text{ nH}$$

The IC internal inductance has not been considered because they are already taken into account in the manufacturer’s data for intrinsic device characteristics: HF noise, ground bounce, etc. A first, coarse approximation of the voltage drop from the capacitor to the IC, resulting from total loop inductance  $L$ , is

$$\Delta V = L di/dt \tag{6.4}$$

**Fig. 6.6** Parasitic inductances with DIP and decoupling capacitor



Let us take an HCMOS gate having a transient supply current demand  $I_1$  of 15 mA/gate (from Table 5.2), plus a transient load demand  $I_2$  of 35 mA (for this device driving five gates). The situation of Fig. 6.6 results in a voltage drop:

$$\Delta V = 75 \times 10^{-9} \times (15 + 35) \times 10^{-3} / 3.5 \times 10^{-9} \approx 1 \text{ V for one gate}$$

First, this is above the worst-case noise immunity level for this type of logic. Second, for emission aspects, this is a significant radiating loop, both by its size (about 4 cm<sup>2</sup>) and by the current it carries (hundreds of mA when several gates are toggled simultaneously). Finally, the too large inductance, and hence voltage drop, also participates in  $V_{cc}$  and Gnd trace pollution, which enters into the whole equipment parasitic emission picture. Although the loop formed by the IC and its associated decoupling capacitor may seem rather modest compared to the signal traces, all the internal IC currents are exactly adding up in this loop, and their contribution to total radiation can be significant (Figs. 6.7 and 6.8).

After such a gross estimation, let us look more in detail how this voltage drop distributes itself along the loop segments (Fig. 6.7): during a positive-going edge (low to high),  $I_1$  and  $I_2$  are adding up in the following traces: AB, BC, CO, and EF; during a negative-going edge (see Chap. 5, Fig. 5.2),  $I_1$  and  $I_2$  are adding in

segments OE and EF. This latter one EF is responsible for the ground bounce of the IC, causing a CM impedance pollution of all the other IC leads.

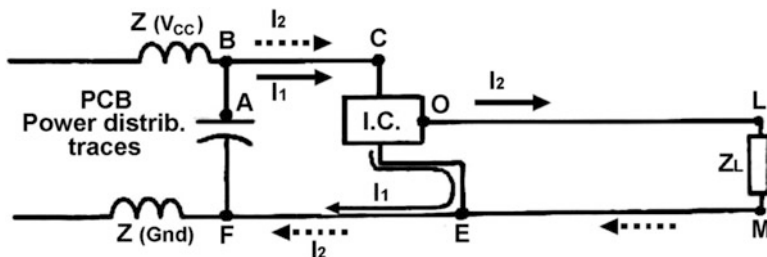
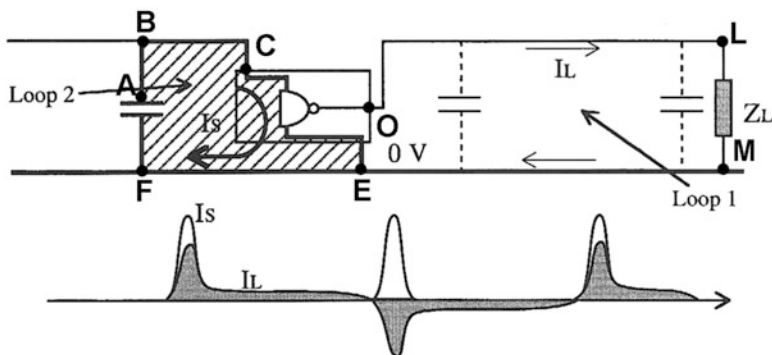


Fig. 6.7 Actual current paths during logic gate switching



**Example:**

Single layer PCB, comparison based on 1 gate only.  
 30 MHz pulses, 20-pin module, TTL family  
 Loop # 1 : 10 cm x 1 cm,  $Z_L \geq 300 \Omega$ , trace inductance = 15 nH/cm (two-way trip)  
 Loop # 2 : 1.5 cm<sup>2</sup>

Spectrum of magnetic moments ( $I \times S$ ) for loops # 1 and 2, based on current spikes only

F (MHz)	30	90	150	330
Loop # 1 (15 mA pk), dB $\mu A$	73	67	58	44
Magn. moment, 10 cm <sup>2</sup>	93	87	78	64
Loop # 2 (40mA peak), dB $\mu A$	82	76	67	53
Magn. moment, 1.5 cm <sup>2</sup>	85	79	70	56

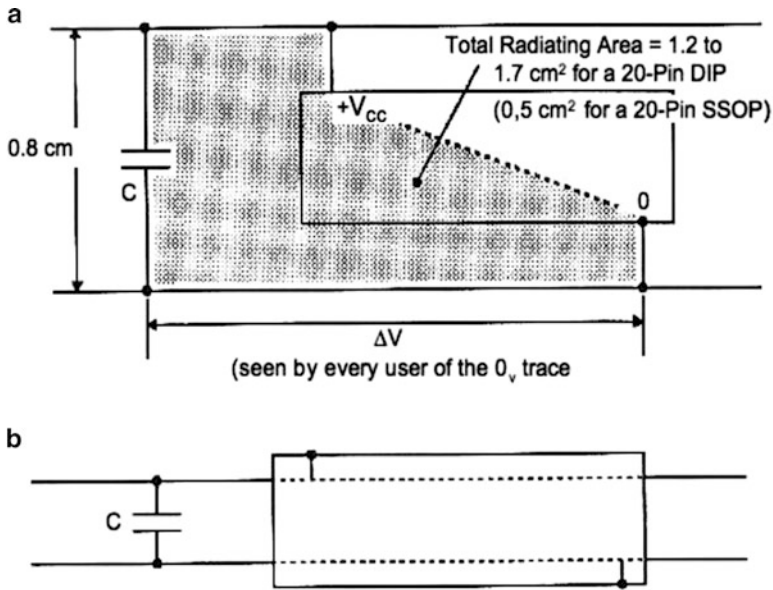
For 1 gate switching : the magnetic moment of  $V_{cc}$  loop # 2 is = close to that of signal loop # 1, adding 3 dB to the radiated field.

Fig. 6.8 Radiation contribution of the IC capacitor loops

Voltage drops along the BC (for positive-going) and EF (for both transitions) segments are the most critical ones because:

- They do affect all the users on this PCB DC distribution branch, not just the gate or chip of concern.
- This is where all the individual gate currents  $I_1, I_2$  are adding up in a single  $V_{cc}$  or ground trace, causing longitudinal voltages that excite CM radiation of I/O cables.

Notice that in terms of self-disturbance,  $\Delta V(BC)$  and  $\Delta V(EF)$  are not critical simultaneously:  $\Delta V(AB)$  relates to the high-state noise immunity, while  $\Delta V(EF)$  relates to low-state immunity which is generally more critical. Figure 6.9 illustrates how  $V_{cc}$  and return traces could be routed close together to reduce capacitor-to-device loop area. This brings down the loop area by about 50%, self-inductance also dropping to  $\approx 8$  nH/cm.



**Fig. 6.9** Bringing supply traces closer to reduce supply current loop (single-layer board). (a) Initial layout, (b) loop area reduced via closer traces

An interesting concept (although as old as electromagnetism) is shown in Fig. 6.10. Whenever two identical circuits are simultaneously switching identical currents, one should try arranging the current paths such that the magnetic moments are subtractive. Doing so, the overall radiation seen at distances greater than the loop separation is significantly reduced.

When a close routing of  $V_{cc}$  and Gnd traces is not possible, another option is to lay an additional  $\approx 0.3$  to 1 mm trace from the capacitor's positive terminal to the module's  $V_{cc}$  pin (see Fig. 6.11). The negative capacitor terminal is located very close to the module Gnd pin. This reduces loop size and provides lesser voltage drop on the ground path (DE) which can be common to other users, therefore more critical. In this arrangement, the loop inductance of the capacitor- $V_{cc}$  pin-chip-ground (ABCDE) loop must be regarded in 3D. Its height above the PCB surface depends on the type of IC package, varying from 0.3 mm (SMT) to  $\approx 3$  mm (DIP). Its length and width depend on the traces' layout, especially with single layer.



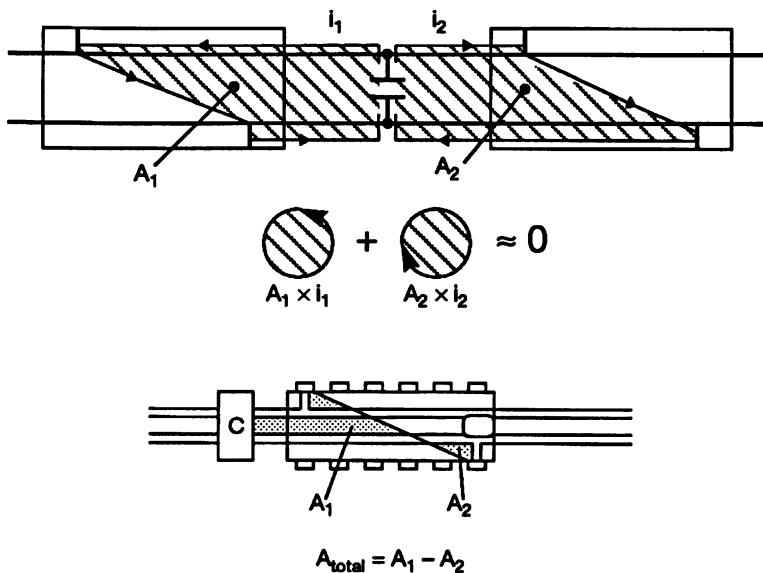


Fig. 6.10 Field cancellation by opposite amp  $\times$  cm<sup>2</sup> magnetic moments

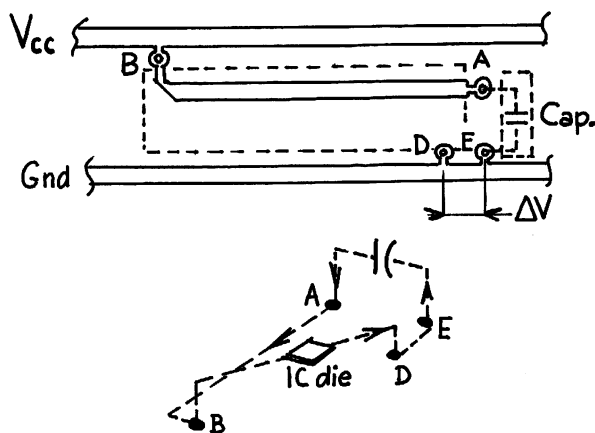
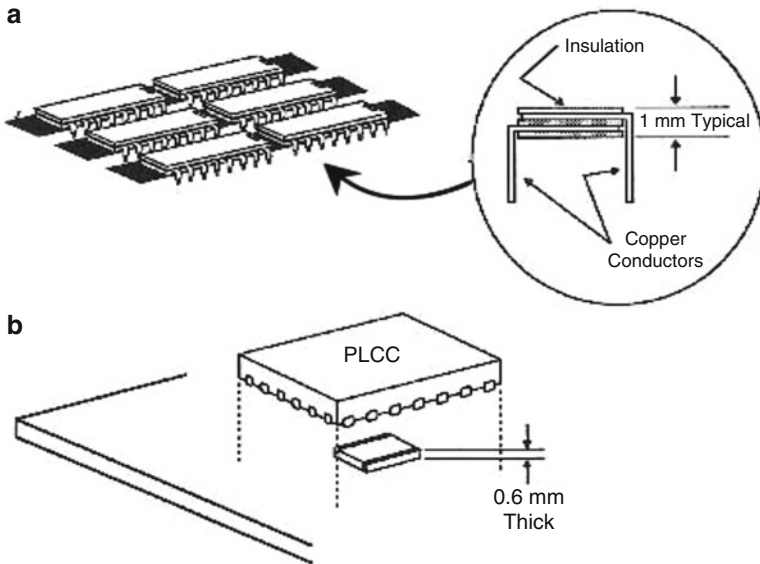


Fig. 6.11 Dedicated capacitor trace to reduce loop size and CM impedance pollution of the ground trace

Other methods of power supply decoupling with minimal inductance and radiation are shown in Fig. 6.12. These include leadless parallel plate capacitors located directly under the Leadless Chip Carrier (LCC) or DIP packages or minibus power distribution. The latter is especially useful when a ground plane cannot be incorporated, or as a retrofit, come-late fix for an already manufactured board. An ultimate solution is to integrate embedded decoupling in the chip or the substrate, as described in Chap. 5, Sect. 5.3. It is worth mentioning another method,

where an embedded capacitance is included in the PCB material itself. This thin layer between the power and 0 V planes acts as a perfect leadless distributed capacitance. It is more expensive too, since it introduces an additional dielectric layer in the standard prepreg epoxy stack of the PCB, so this solution is generally reserved for high-tech multilayer boards.



**Fig. 6.12** (a) Flat-bus Mico-Q by Circuit Comp. Inc., ex-Rogers. (b) MLC leadless decoupling capacitor. Both offer minimal parasitic inductance

### 6.3.2 The Problem with Bypass Capacitors in Parallel

With one decoupling capacitor per IC or pair of ICs, there are unavoidably many places where two or more capacitors will be close and parallel on a same  $V_{cc}/Gnd$  traces pair, forming a resonant  $L/C$  tank. A self-resonance frequency will exist, with a  $Q$  factor limited only by the DC resistance of traces and vias [3, 13]. As a result, in a narrow-frequency band, some of the switching current demand of IC<sub>1</sub>, while IC<sub>2</sub> is quiet (Fig. 6.13), may be in fact pumped out of  $C_2$  instead of  $C_1$ . This causes a larger radiating loop than expected for the capacitive current that may well never show up if there is no frequency to excite this mechanism. It could be predicted by a careful simulation with SPICE or other software, and if it occurs, it can be reduced by the following solutions:

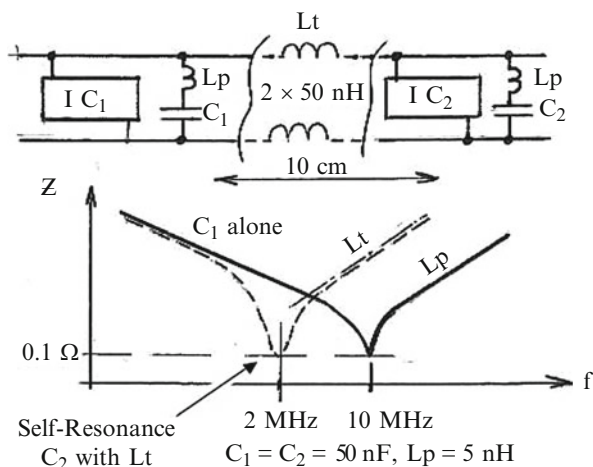
- (a) Enlarging the  $V_{cc}$  and Gnd traces, bringing them closer, or on top of each other, or better changing to a ground plane. By decreasing the trace's self-inductance  $L_t$ , the self-resonance  $L_t/C_2$  is shifted upwards in frequency. This may not seem very helpful, but in fact this new frequency corresponds

to a lower impedance value for  $C_1$ , which will compete more efficiently with  $C_2$  for feeding the current to  $IC_1$ , hence reducing the effective radiating loop size.

- (b) Provide some resistive damping of the resonant circuit. This may prove less easy, technically and cost wise. Adding a few ohms to the DC distribution creates a permanent waste and an undesirable voltage drop for all the users on this particular board. For some critical devices like RF amplifiers, this can be done in the form of an RC decoupling instead of a simple  $C$ .

A better option is to insert a small, surface-mount, lossy ferrite between the  $V_{cc}$  rail and the capacitor lead. The ferrite must have a low inductance value but a high-resistive term to act as a frequency-dependent resistor. This both reduces the  $Q$  of these unintended  $L/C$  circuits and forces the current demand of each IC to be taken from its dedicated capacitor.

**Fig. 6.13** Parasitic  $L/C$  resonances with bypass capacitors in parallel



### 6.3.3 Decoupling at the Board Power Input

Because many decoupling capacitors installed on a board need to be recharged after each logic transition and even though the corresponding time constant is greater, the resulting  $\Delta V$  voltage dip at the board interface and subsequently on the rest of the power distribution may be too high; this, in turn, would export the daughterboard noise emissions into the rest of the power distribution circuit, motherboard, and the like. To avoid this, it is a good precaution to install a large ceramic (MLC) or aluminum capacitor near the edge connector  $V_{cc}$ /ground terminals. This capacitor, which becomes part of the “bucket brigade,” should be sized (but not exceed) to the sum of the individual ICs’ capacitors.

### 6.3.4 $V_{cc}$ and Ground Traces Layout (One-Sided, Single-Layer Board)

With regard to power distribution, one consequence of too much separation between the power supply and return rails was discussed in Sect. 6.2.1. This is further illustrated in Fig. 6.14, where a poor PCB layout is used with the “fingered” supply traces on one edge of the board and the return traces along the opposite edge. This, along with excessive inductance, creates huge radiating loops such as ABCDE and AFGHE for transient power supply currents. Similarly, signal currents between modules are forced to return by some snaky path.

A somewhat better layout is shown at the bottom part of Fig. 6.14. Here the  $V_{cc}$  and Gnd traces are laid close together in horizontal parallel runs. They form a low-impedance, low-area transmission line while allowing signals to run horizontally unobstructed on the solder side of the board. However, signal traces to ground return still can form significant loops.

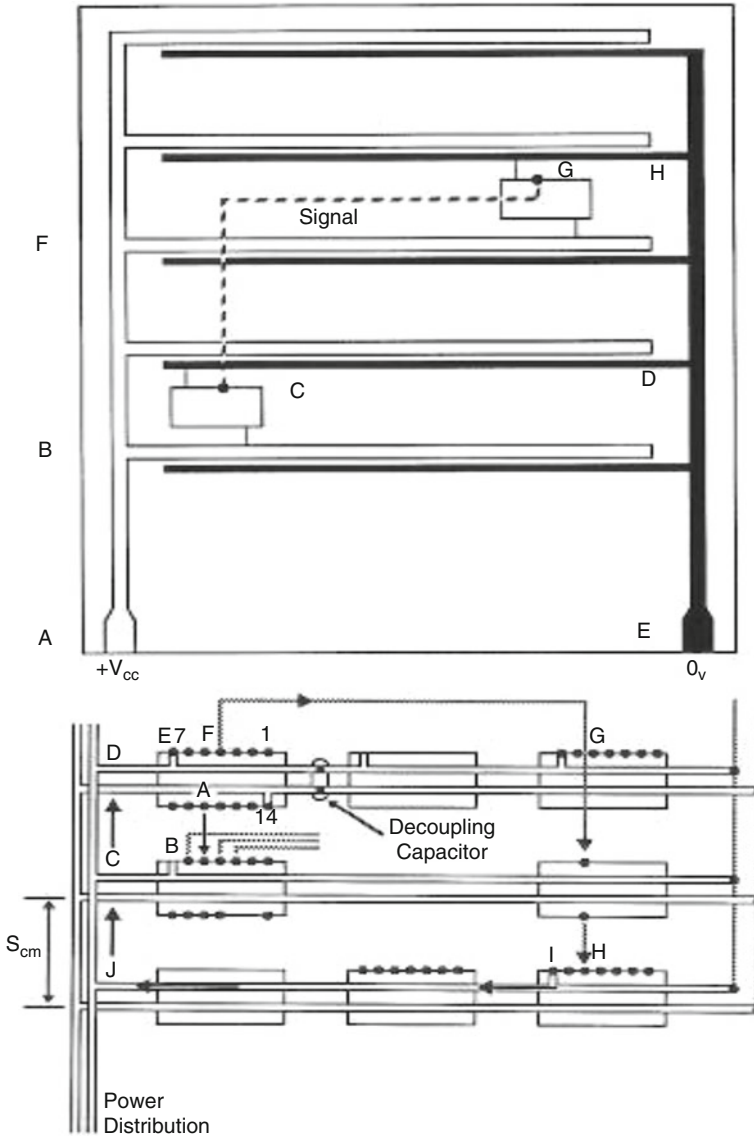
Imposing an additional constraint of running most horizontal signals on the solder side and vertical signals on the component side, an even better layout is suggested in Fig. 6.15 [10]. Although it cannot match the performance of a multilayer board, it offers a gridded pattern for  $V_{cc}$  and Gnd traces; all intersections are connected by via holes. At the edge connector, at least every tenth pin is assigned for ground, unless signal impedance matching requires more ground pins. (This is discussed in Sect. 6.6.)

### 6.3.5 The Need for Ground Planes and Ground Areas (Single-Layer Board)

Single-layer boards do not easily lend themselves to hosting a ground plane. Except for very sparsely populated boards, all of the available real estate is needed for signal traces, with not much room left for power distribution traces, let alone for a whole ground plane. However, even if an entire side of a two-sided, single-layer PCB cannot be sacrificed for a copper foil, several simple arrangements can produce comparable performance.

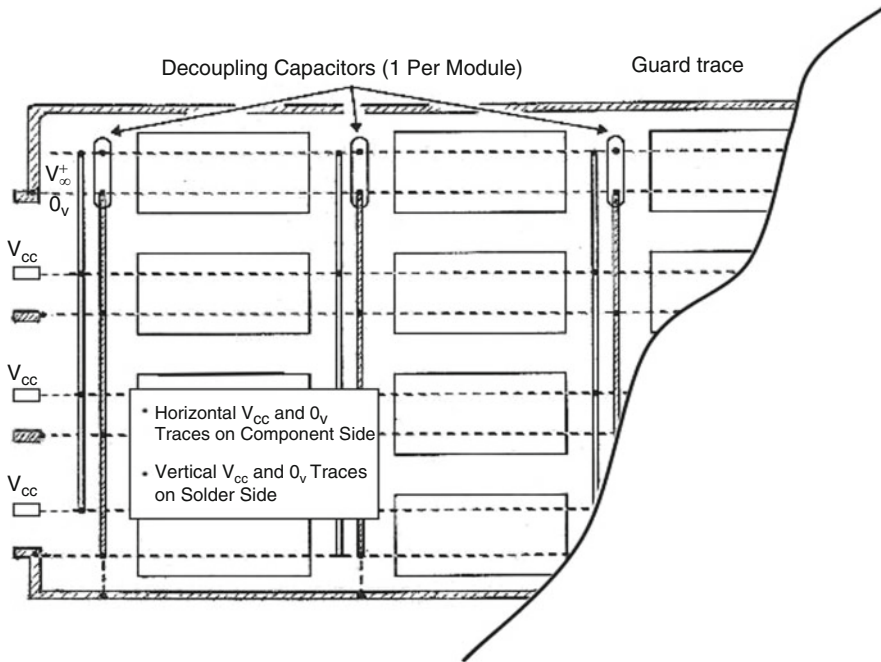
As it was seen in Fig. 6.3 comparison, changing from thin, long traces to a copper plane will bring a drastic decrease in inductance. By leaving as much copper as possible rather than etching it away, a low impedance is achieved for both the supply and ground since they are close together. This can be expressed by a simple guideline: make the PCB as optically opaque as possible by extending supply and ground return traces into large areas.

If the board is a single-layer, single-sided type, the  $V_{cc}$  and signal lines will have a better opportunity to run near a ground copper land (Fig. 6.16). Above few hundred kilohertz, it is true that returning currents will not use the whole copper surface and will concentrate on the edge, so the effective reactance will be higher



**Fig. 6.14** *Top:* A poor layout (single layer) creating huge radiating loops. *Bottom:* A somewhat better layout, reducing power distribution loops. However, signal trace-to-Gnd loops are still large, with typical spacing,  $h$ , of 2-2.5 cm. Areas such as ABCDEA represent  $\approx 3 \text{ cm}^2$ ; FGHIJDEA represent  $20\text{-}30 \text{ cm}^2$

than that of the ideal plane, yet most loop sizes will be reduced significantly. If the board is a single-layer, double-sided type, the  $V_{cc}$  and signal lines often will be above a ground copper land, and less current will circulate on the copper plane edges. Radiating loop size and power distribution noise will be further reduced.



**Fig. 6.15** An even better single-layer design, reducing both power and signal-to-Gnd trace loops

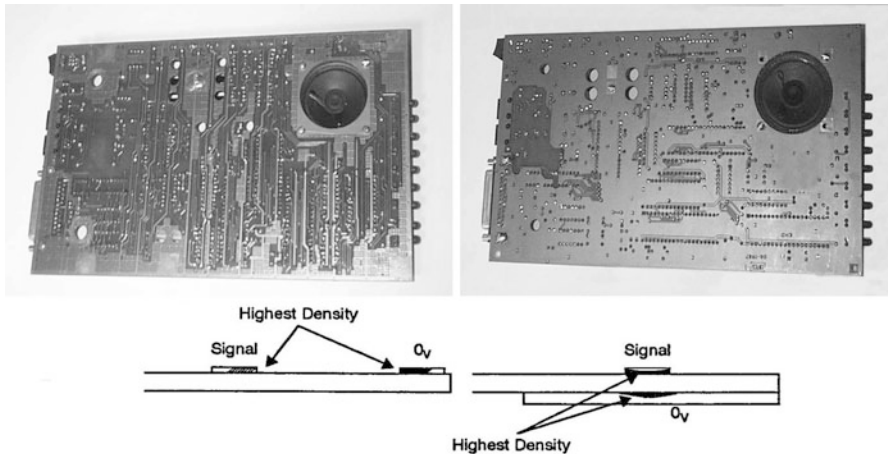
It is sometimes feared that such islands created by copper landfill areas are useless or even counter-effective. When examined carefully, these concerns have some bases that are addressed below:

- The PCB designer (or the CAD auto-router) may neglect to connect some of these islands to the rest of the ground network. A floating copper spot is worse than no copper, because it may aggravate capacitive crosstalk and radiation.
- Sometimes a copper island is linked to the ground grid at only one point, the reason invoked being the famous "single-point myth." Unless it is used simply as an electrostatic screen, the landfill's essential purpose is to reduce the whole ground grid impedance, which means there must be current in it. With a one-point connection, there will be no current.
- Sometimes an island is correctly tied with the ground grid at several points, but there is no critical (high-speed or sensitive) trace running atop or nearby; therefore current paths are elsewhere, and indeed, the island brings no improvement at all.
- If a portion of the PCB is dedicated to low-frequency, sensitive analog circuits (with detection threshold in the range of mV or less), the designer may have chosen to operate with a locally floating (isolated) 0 V reference. In this case enlarging the 0 V areas will increase the stray capacitance to chassis ground, deteriorating the isolation concept of the analog part.

*Answer to (a) and (b):* Landfills must be connected to the general ground patch at every possible occasion and especially at places where a signal trace is running nearby or above.

*Answer to (c):* Even if the copper island is useless for the moment, a future change may move or add traces which will benefit from its proximity.

*Answer to (d):* It requires that the 0 V traces be kept (no landfill) in these purely analog areas; only the digital Gnd will be treated as copper planes. Nevertheless, the I/O interfaces of the low-level analog to the outside world still need to be decoupled to chassis, to avoid unwanted HF signal penetrating or exiting the PCB by passing through the floating analog Gnd (see Sect. 6.8, at the end of this chapter).



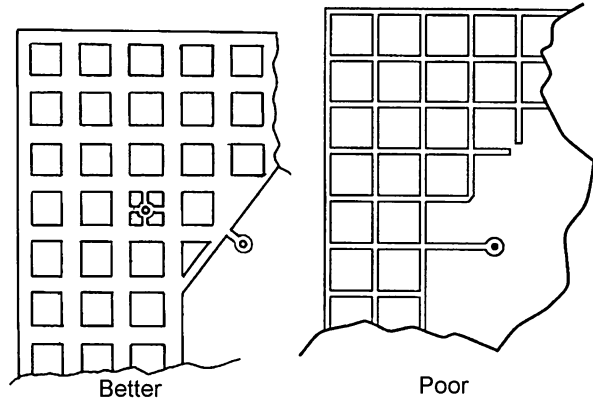
**Fig. 6.16** Benefits of Gnd lands. By not etching copper for  $V_{cc}$  or Gnd (at the right), the cost does not exceed that of board at the left, but radiating loops are smaller, as the current density distribution is tighter thanks to a nearby ground. Photo courtesy of D.L.S Electronic Systems, Inc.

Often, for manufacturing reasons (etching and tin flow or balancing of mechanical strain), large copper lands on the card top are replaced by grids. Although this creates a slight impedance increase, it does not significantly affect the concept, provided there are no flagrant discontinuities and the grid bars remain large (Fig. 6.17). Notice that bottlenecks like those associated to ground vias have been kept to minimum inductance on the left-hand sketch. In contrast, narrow grid bars and long bottleneck severely increase the grounding impedance.

### 6.3.6 Trace-to-Chassis Parasitic Coupling

Fast signal traces should not be placed next to the board edge, which in most cases also places them close to a chassis, causing capacitive leakages. There should be at least a ground trace or plane edge extending far enough to ensure that HF currents will return by the PCB ground rather than by some uncontrolled path over

**Fig. 6.17** Acceptable vs. poor grids in copper planes



the chassis length. Having uncontrolled HF currents returning from a “hot” trace to the source via a long run across the chassis may exacerbate radiation through the enclosure, unless this enclosure has been fully treated as a shielded enclosure. This might seem contradictory with something we will recommend later on, i.e., decoupling I/O lines by capacitive filtering to chassis. However, this will be done in a controlled manner, at the I/O connector zone, where HF current circulation will be confined to a well-defined portion of the chassis, that is, the connector plate.

### 6.3.7 Clock Traces (Single-Layer Boards)

With single-layer boards, clock traces are especially prone to radiation and crosstalk coupling, due to the general lack of a continuous plane as a return. Any trace carrying clocks  $\geq 10$  MHz must have a dedicated ground trace running parallel from end to end, either on the same side at a distance  $< 1$  mm or underneath.

If clocks  $\geq 50$  MHz are run on a single-layer board (not a safe practice), the clock trace must be bound by two ground traces, at equal distances. This creates two identical loops, each one carrying half the return current, but with opposite magnetic moments hence less radiation. This can prove necessary even for a board with a real ground plane on one side. Take, for instance, a thin clock trace like 0.16 mm width (6 mil) and a board thickness of 1.6 mm: two grounded traces at 0.16 mm on each side (center to center 0.32 mm) are more efficient for crosstalk reduction than the ground plane which (in terms of  $h/w$  ratio) is farther.

## 6.4 MULTILAYER BOARDS

Multilayer boards are the ultimate answer to PCB noise in general and especially to radiated EMI. At a bare cost of 1.5-2.5 times that of a single layer, they can sometimes eliminate the need for expensive overall box shielding. Aside from radiated EMI



compliance concerns, it is in general difficult to operate high-speed logic successfully on a single-layer board because of common impedance coupling. While articles have described such single-layer board achievements, they require considerably more attention to fabrication details, making quality control and repeatability difficult during mass production. To avoid a range of problems, including excessive radiation, multilayer boards are recommended wherein the power supply and signal ground are realized on dedicated copper planes.

One major issue with multilayer PCBs is that of layers stack-up: four, six, eight layers, or more are common nowadays, and the number of possible stacking combinations of signal,  $V_{cc}$ , and Gnd (0 V) layers is impressive. Although there is generally a “component side” and a “solder side,” some PCBs can use both the upper and lower layers for components’ mounting. Furthermore, depending on the exact manufacturing process, the interleaved dielectric materials are not exactly of the same nature and thickness, with generally an alternate stack of hard epoxy core and thinner prepreg layers. The number of layers is most generally an even number, in order to better control the mechanical strain and warpage.

Figure 6.18 shows the principal variations from single-layer to eight-layer PCBs. One golden rule must always be kept in sight: “what is actually the return path(s) a signal current will follow in its two-way trip?” This is a driving factor in selecting the layers and the ways the signals and through vias are arranged [8]. As often in engineering, the choice is a double-edged sword with advantages and drawbacks. The stacking order of the layers has a critical impact on signal integrity and EMI in general, as shown in Fig. 6.19 that summarizes the essential aspects shared by multilayers. Upper sketch illustrates an ideal situation simply based on three levels: given that the density of interconnects on this board does not permit all signals a direct point-to-point run, a signal trace on level #1 has to jump to level #3 [11]. The vertical trip from #1 to #3 is made by a via that goes through the Gnd plane level #2 by an isolated antipad. After a run on level #3, the signal goes up again to level #1 using another via. Then, from the load, the current is returning to its source by the Gnd plane #2. For a trace that must change level, this situation is regarded as ideal because:

- The outgoing current is always at a minimum height above its return plane. No matter how sneaky the signal trace, *the opposite return current can always find the least inductance path*, that is, the smallest magnetic loop area, by remaining “in the shade” of the trace above.
- The signs of the magnetic moments for the two loops are opposite; thus even if they do not cancel out perfectly, their inductive effects are subtractive, not additive.
- The length of the vertical current run(s) by the vias is also an inductive segment, but it is kept to a minimum:  $2 \times$  layer thickness.

Lower sketch on Fig. 6.19 shows a common case where the ideal stacking is violated. In this four-layer arrangement with #1 and #4 being signals, the trace on top has to cross vertically three dielectric thicknesses to reach layer #4. On the topside (component side) of its trip, outgoing signal current  $I_s$  and its return  $I_r$  are

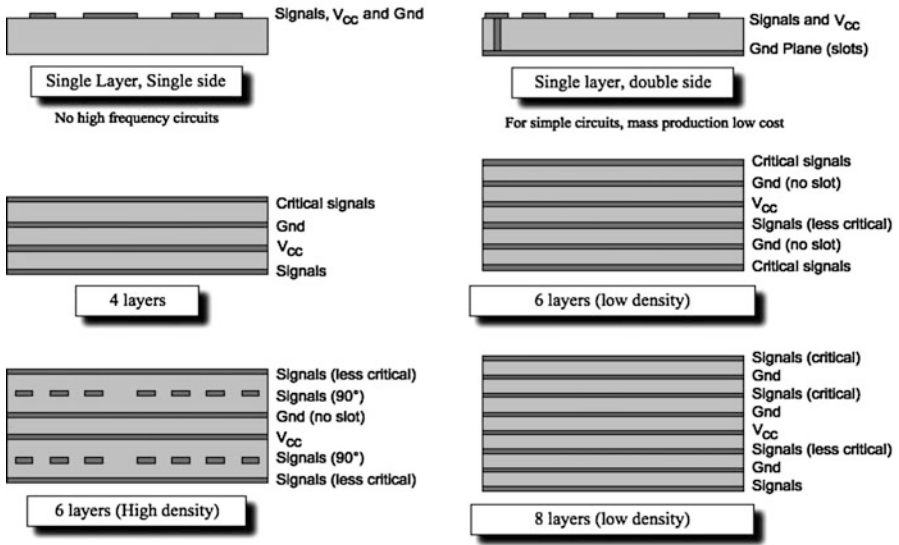


Fig. 6.18 Summary of recommended layer stack for PCBs, from single layer to eight layers (courtesy of AEMC, France)

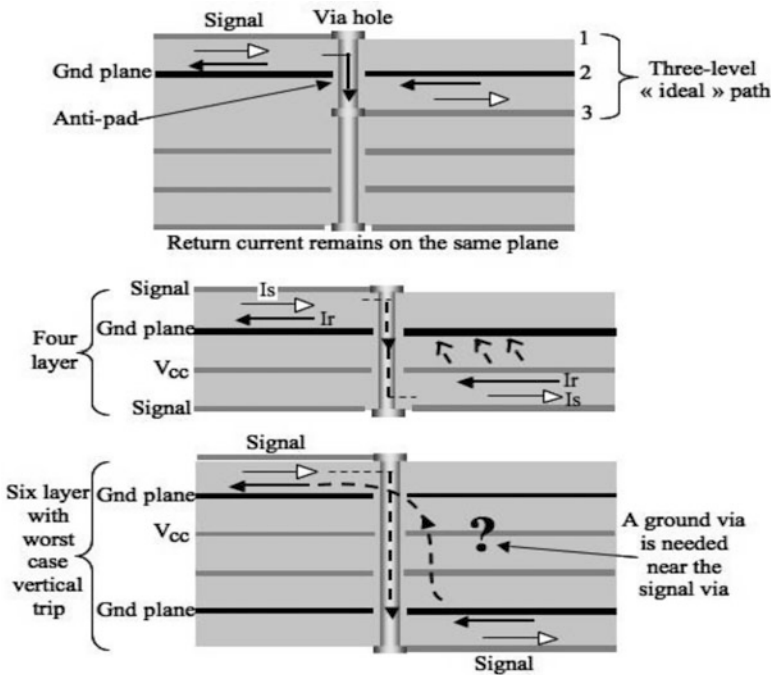


Fig. 6.19 Always beware of the actual return current path and associated magnetic loop

satisfying the least inductance rule (minimum height between trace and plane). On the bottom side, to close the current loop, the  $I_r$  current associated with signal on layer #4 starts by using the  $V_{cc}$  plane (layer #3) as a substitute Gnd path, thanks to the strong capacitive coupling between  $V_{cc}$  and Gnd planes. But, in fact,  $I_r$  is jumping as a capacitive (displacement) current from the  $V_{cc}$  up to the Gnd plane, in order to satisfy the least inductance rule on the left part of the trip. This vertical displacement current excites a TEM mode in the interplane cavity [11]. The PCB being not infinite but finite, it behaves as an open-ended parallel plate line exhibiting mismatch and standing waves. For instance, with a 10 cm-long PCB, this creeping wave phenomenon appears at 750 MHz, causing periodic  $\pm 10\%$  voltage ripple on the  $V_{cc}$  plane. Multilayer arrangements where signal traces are always closest to the 0 V layer do not suffer from this problem.

### 6.4.1 Multilayer Stacking

A commercial-type multilayer board is shown in Fig. 6.20, where a four-level configuration is used. The first level is the component side, and it carries the interconnect traces. Combined with the upper face of level B, they form a microstrip line. The upper and lower faces of ground return level C are, in theory, electrically isolated by three skin depths (about 25 dB) around 30 MHz. Thus, currents returning from fourth level D and flowing on the lower face of level C do not appear on the upper face, and vice versa. This is more academic than applicable to the real world, as ground planes generally are heavily perforated. Thus, signal level A forms microstrip lines with 0 V and  $V_{cc}$  (B) as well, since the two are strongly coupled for high frequencies. Likewise, signal level D forms microstrip lines with 0 V plane (C) but also to some extent with  $V_{cc}$  plane (B). Compared to a typical single-layer/one- or two-sided board without ground plane, where the distances between signal and ground traces are in the range of centimeters, the 0.2-0.5 mm layer separation with multilayers makes radiating loops about 30-100 times smaller.

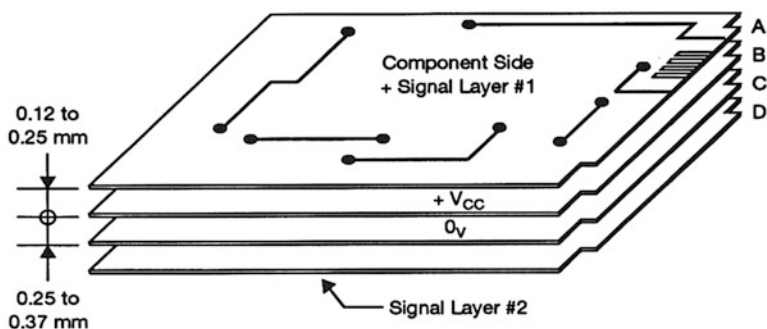


Fig. 6.20 Typical multilayer board with signal traces outside

Other advantages of Fig. 6.20 arrangement are the following:

- Easy access to signal traces for repairs and temporary wiring changes.
- Minimum crosstalk between the two signal layers (#1 and #4).
- Minimum spacing between the  $V_{cc}$  and Gnd planes (only one-layer thickness). This makes the two planes behave as a heavily capacitive line, with very low characteristic impedance (typically a few ohms).

Figure 6.21 shows the inverse arrangement, where  $V_{cc}$  and Gnd are the external planes. This provides some shielding by “sandwiching” all signal lines between two copper foils. It also provides a more even transmission line configuration (true stripline) than the asymmetrical microstrip of Fig. 6.20. The corresponding drawbacks are the following:

- It is almost impossible to access the signal layers.
- It becomes mandatory to run signal on levels #1 and #2 at  $90^\circ$  or to stagger them sideways by at least  $3 \times h$ , for avoiding heavy crosstalk between layers.
- Sensitive signals in layer #3 may suffer capacitive crosstalk from the  $V_{cc}$  distribution #4, which is not a quiet plane.
- With some leadless modules, the top Gnd layer will be heavily perforated (a bad practice).
- It forces lower characteristic impedance for the signal traces (typically 1.4 times less than the Fig. 6.21 arrangement), which causes an increase in dynamic loading for digital IC outputs with fast rise time.
- The natural coupling between  $V_{cc}$  layer #4 and Gnd layer #1 is less efficient than in Fig. 6.20 because of the three times higher separation.

Thus, in spite of a few appealing features, the four-layer arrangement of Fig. 6.21 is not recommended.

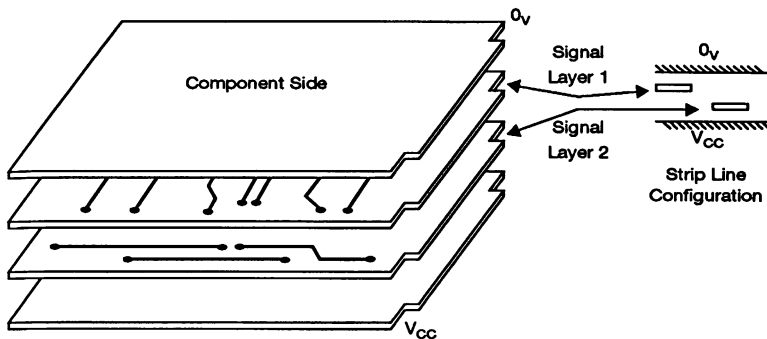


Fig. 6.21 Four-layer board option with buried signal traces

For very dense boards and military or aerospace applications, multilayers with 6, 8, and even up to 14 levels can be used. In terms of radiated emissions, the aspects discussed above are applicable to any number of layers. A recommended

arrangement is shown in Fig. 6.22 for a six-layer board. It has the merit of providing four signal layers and keeping a low-impedance  $V_{cc}$ -0 V distribution, so it is optimal for very dense circuitry, with the following recommended stack:

- Layer #1 (the least protected layer): low-speed or steady-type signals. Possibly, high-speed signals but only for the shortest runs (no more than a few cm).
- Layer #2: high-speed signals. These must be run at a  $90^\circ$  angle with layer #1 or staggered as shown.
- Layer #3 and #4: Gnd and  $V_{cc}$ . Eventually, the dielectric thickness between #3 and #4 can be thinner, and made of a material with a higher  $\epsilon_r$ , for increased buried capacitance.
- Layer #5 and #6: signal layers, treated like #2 and #1, respectively.

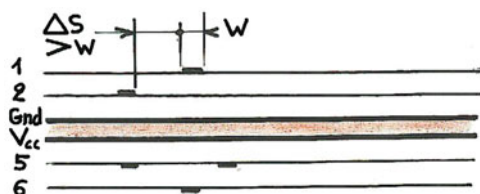


Fig. 6.22 Recommended arrangement for high-density six-layer board

When changing from layer 1 to 2, or 5 to 6, one can use buried (blind) vias, rather than drilling holes in power and ground planes. In certain applications, however, blind vias are suspected of causing long-term reliability problems under harsh environment. As an alternative, layers #2 and #3 can be interchanged, which releases the constraint for the  $90^\circ$  runs and keeps the critical traces buried in a true stripline mode. This is at the expense of doubling the height between the  $V_{cc}$  and Gnd layer, reducing by 50% the buried capacitance, and like with Fig. 6.21, putting a risk of crosstalk from  $V_{cc}$  to signal layer #3.

A variation for six layers is shown in Fig. 6.18 (captioned “low density”). At the expense of losing one signal layer (three instead of four), it avoids the constraint of  $90^\circ$  runs for signal layers and provides for all signal layers a ground plane nearby that stabilizes the characteristic impedance. Layer #4 should have only nonsensitive signals, since it is sandwiched between the  $V_{cc}$  plane (inherently noisy) and Gnd.

Finally, an eight-layer board arrangement is also described on Fig. 6.18, with the following features:

- Signal levels #1, #3, #6, and #8: good impedance control, with small height above Gnd plane
- No need for  $90^\circ$  runs
- Ideal coupling between  $V_{cc}$  and 0 V planes
- Three Gnd planes
- Minimum number of layers to cross vertically for jumping between signal layers

The only drawback remains on layer #6 where the traces have a risk of significant capacitive crosstalk from the  $V_{cc}$  plane. This layer should have only noncritical signals.

When true differential signals like LVDS are routed on multilayer PCB, additional constraints arise:

- (a) When a differential pair of traces is vertically changing from layer 1 to layer  $N$ , the two vias must remain very close in order to prevent any impairment of the characteristic impedance.
- (b) Since the differential pair must, in theory, remain at a same distance from the nearby ground plane, any Gnd via existing near the pair of signal vias has the risk of introducing an asymmetry in the vertical crossing. [1] has shown that if two vias of a differential pair, separated by 50 mil (1.27 mm), are sharing a reference to a same Gnd via that is asymmetrically offset by 50 mil from the nearest via, a DM-to-CM conversion of -50 dB at 1 GHz will take place. That means that an ideally balanced differential signal will create on the corresponding I/O cable a CM excitation of 3 mV per volt, violating the design criteria for external cable contamination vs. FCC Class B radiated limit (see Chap. 2).

Before concluding this review, a word of caution is appropriate. In PC boards that mix digital, analog (slow), high-level RF digital or analog (transmit), low-level RF analog (receive), and so forth, there is often a need for separate power and ground planes. This is to avoid the risk of return currents from one circuit polluting the others and, eventually, reradiating at unexpected places. When such plane segregation is needed, the different planes should be laid side by side, never on top of each other. Due to the large capacitance, stacking planes from different functions would create a strong coupling effect, causing a fraction of the high-level currents to circulate in low-level ground plane.

## 6.4.2 Decoupling Capacitor Requirements with Multilayers

A question often arises: with the  $V_{cc}$  and Gnd planes being so close, do not they create huge in situ capacitance, which reduces or eliminates the need for discrete decoupling capacitors? In fact, except for very specialized boards where a high dielectric compound is laid between the two power planes, a regular multilayer offers only 30-300 pF/cm<sup>2</sup> of “free” capacitance. For a typical 20- or 24-pin package occupying approximately 4-6 cm<sup>2</sup> of board real estate, this is totally insufficient and discrete capacitor requirements remain. Nevertheless, as frequency increases to the VHF (30-300 MHz) region, a point is reached where the unavoidable parasitic inductance of discrete power supply capacitors will make them progressively useless. A typical manufacturing practice is shown in Fig. 6.23, with the soldering lands, via hole and thermal drains concurring to a parasitic inductance that spoils some of the zero-inductance concept of leadless capacitors.

One way of reducing the parasitic inductances' ( $L_1, L_2$ ) effect is to add a second  $V_{cc}$ /Gnd lead + via hole.

Figure 6.24 shows such configuration where the 100 nF SMT capacitor, although close to perfect, will resonate around 12 MHz with the 2 nH inductance of its via hole and soldering pad. By contrast, the 1,000 pF board self-capacitance (for  $\approx 6 \text{ cm}^2$  real estate) is complementing efficiently the discrete component above 100 MHz. Soon after, the  $V_{cc}$  and Gnd planes' stack is seen as a parallel plate line whose distributed  $L, C$  parameters are providing a characteristic impedance  $Z_0 = \sqrt{L/C}$  with typical values of 1-3  $\Omega$ .

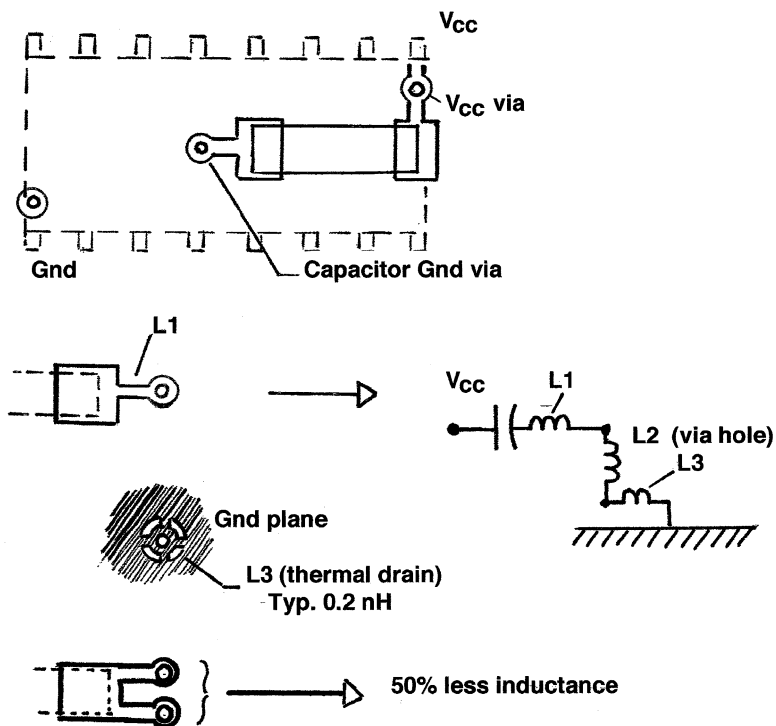


Fig. 6.23 Residual inductance of bypass capacitors in multilayer boards

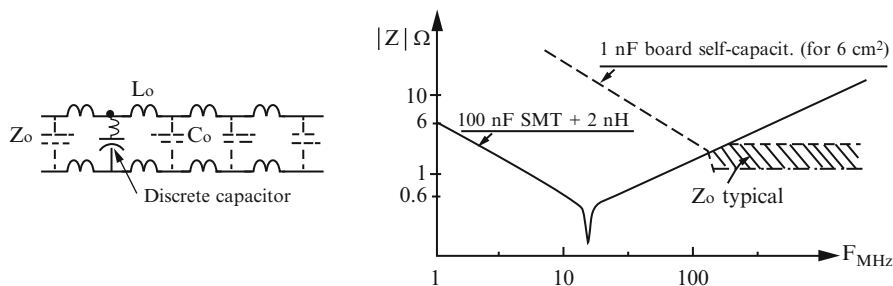


Fig. 6.24 Combined impedances vs. frequency of discrete and buried capacitors

### 6.4.3 Perforated Planes: The Swiss Cheese Syndrome

With densely populated boards, the ideal plane concept that is set forth when advocating multilayers becomes something like the illustration in Fig. 6.25. Not only is the copper area reduced (in fact, by no more than 10-15%, which would be tolerable), but many IC zones are so perforated that some holes overlap, the string of holes becoming a slot ([6], and Sect. 5.3). This leads to three observations:

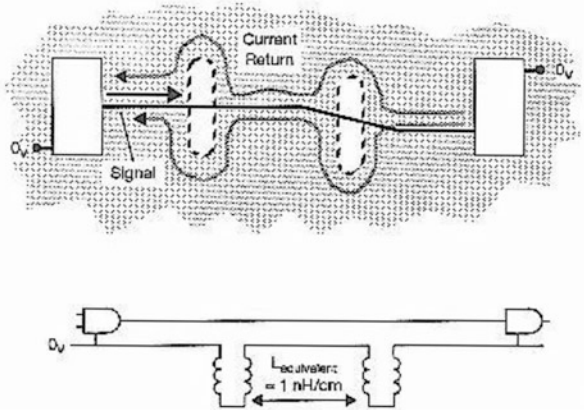
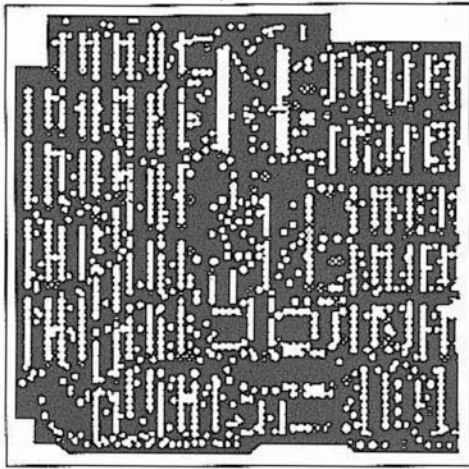
- (a) A slot in itself would be of no consequence; the problem arises when a signal trace (especially a high-frequency one) crosses over the slot. Return current density is disturbed, with current lines concentrating on the slot edges (following a loop route equivalent to an inductance  $\approx 1$  nH/cm). This is like exciting a slot antenna if one were to transmit intentional radio signals, which is exactly what we do not want.
- (b) The problem is reduced if a copper rib is maintained between holes. But this still turns the plane into an array of bottlenecks, especially in high current density areas. For instance, in Fig. 6.26, the decoupling capacitor has to serve the PGA modules through narrow, inductive paths. A better decoupling, therefore less radiation, is achieved by putting one capacitor on each side. SMT packages and BGAs have another plus here: they apparently do not degrade internal planes. Yet, the need for many signal vias results in as many antipad holes in power and Gnd planes. Typically, antipad diameter is 1.5 times the via diameter, and the isolation ring around the pad is adding another 50% increase in the Gnd plane hole.
- (c) One should never make a slot in a ground plane for burying-in a clock trace, hoping that it will reduce EMI. This may effectively reduce this particular trace radiation but increase seriously the radiation of many other signals that will cross this slot.

### 6.4.4 Allowable Slots

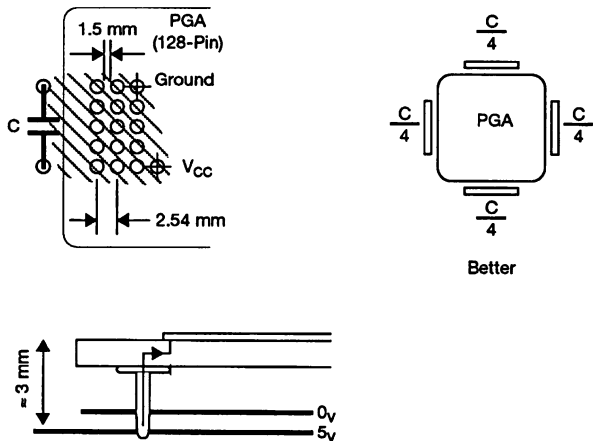
With mixed-function boards, particularly those combining analog and digital circuits, a gapped plane is sometimes used to avoid a certain amount of logic current returning by the analog ground land. With such a layout, absolutely no signal trace should be permitted to cross over the slot area. Signals that must go from one zone to the other should pass only above the small copper land in the upper part of the board (Fig. 6.28) where the A/D converter is located.



**Fig. 6.25** What a ground plane can become



**Fig. 6.26** Perforated plane disturbing capacitor discharge path



### 6.4.5 Placement of High-Speed Traces

Some traces must be routed very carefully, due to their high probability of radiating at discrete, stable frequencies. Such traces include those for clocks, crystals, least significant bit (LSB, especially with address bus), RF oscillators, and video circuits. The following guidelines must be observed for proper high-speed trace placement:

- Above perforated plane areas, do not run critical traces across a row of holes. Run them parallel instead.
- Do not run critical traces at the extreme edge of the card. This will nullify the ground plane advantage and pull return current to the edge, increasing radiation (see Fig. 6.27). Be aware of a frequent manufacturing practice of etching 3-4 mm of copper from around the entire PCB edge, and take this into account.

Many rules-of-thumb recommend to route critical signal traces far from edges. The question is: how much is enough? The portion of current that would spread out all the way if the plane was infinite has no other choice than concentrate on the border of the finite plane (see Fig. 6.3b). This concentration on a virtual, knife-edge conductor can be modeled as a thin radiating wire. It has been calculated [17] that if “ $k$ ” is the ratio of distance-to-edge/trace height, the percent of this plane edge current to the full trace current is as follows:

$k$ :	3	5	10	30	100
% of main current returning by the edge:	10	6	3	1	0.3

The radiation contribution of this “ghost pair” can be estimated by the trace-to-edge loop area, assuming the edge-returning current corresponds to an equal outgoing current on the trace. For low values of  $k$ , this contribution is significant. To reduce it:

- Increasing the  $k$  ratio, by a 5-10 factor will decrease the concentrated edge current.
- Add a ground trace on the top layer, close and parallel to the source trace.

Differential signal traces, like those commonly used with LVDS interconnections, require much specific attention. Due to the crucial importance of balancing, the symmetry of the two traces vs. the Gnd plane must be maintained all along the differential run, from the transmit/receive IC to the PCB connector. This includes the vias that will serve for changing levels in the PCBs (see forthcoming section on matching).

### 6.4.6 Analog/Digital Mix

A PCB hosting both low-level analog and digital circuit is always a designer’s nightmare. Analog circuits for audio or low-frequency applications, like microphone inputs or instrument sensors, are often operating with sensitivity thresholds

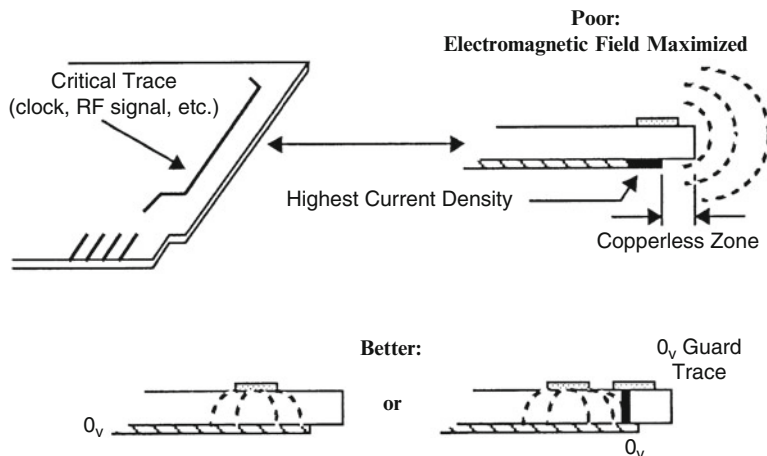


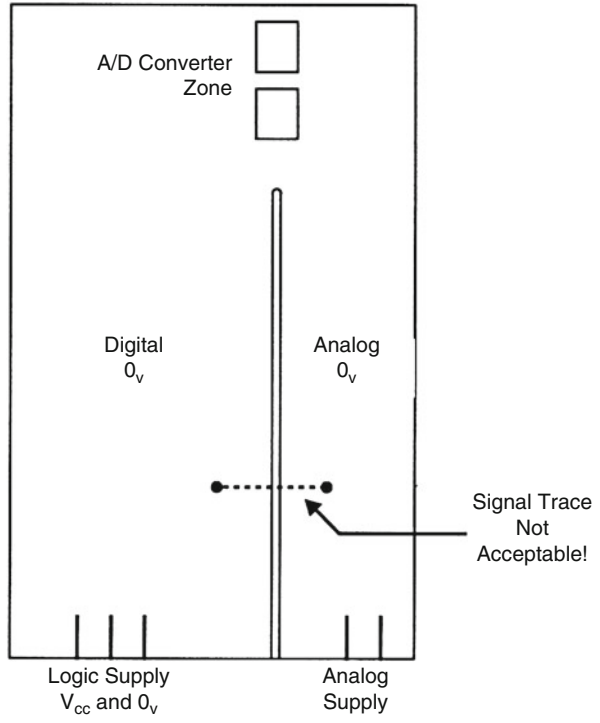
Fig. 6.27 Problems with high-speed traces on board edges

in the mV range or less. They demand the least possible stray capacitance between sensitive traces and surrounding ground. They can be sensitive to low levels of external ground loop currents circulating in their analog reference. Thus, their 0 V should not be grounded locally to chassis ground so as to take the best profit of the high CM rejection of their differential op-amps. On the contrary, digital circuits operate with fractions of a volt, but their 0 V must remain equipotential vs. the chassis at frequencies above few tens of MHz, so as to not cause CM excitation of I/O cables. So, the digital 0 V must be a plane, grounded to chassis at several places. Figure 6.29 shows a way to accommodate such dilemma.

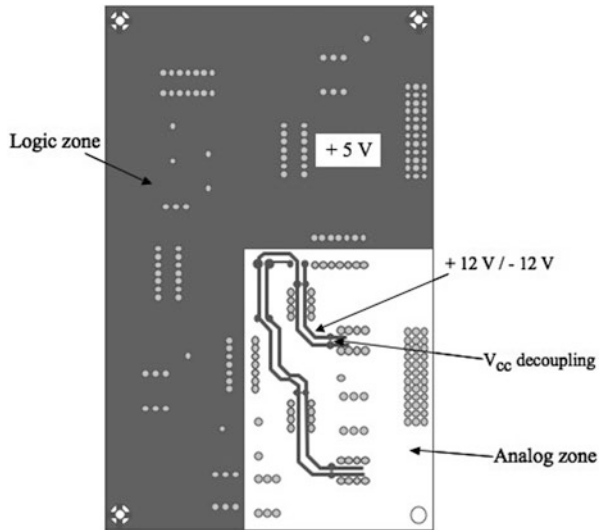
Analog circuits for RF applications often operate with sensitivity thresholds down to the  $\mu\text{V}$  for the input section of RF modules (mobile phones, radio or TV receivers, RF modems, etc.). This is 60-120 dB below the amplitude of digital switched levels, which can be located within a centimeter range on the same board. The compatibility between the two portions is first a matter of functionality, but there also are few typical implications with radiated interference:

- Residues of clock harmonics with few tens of mV can appear on analog traces, out of band of the analog circuits, therefore not of concern for their performance. Nevertheless, the polluted analog signals can turn into fortuitous, efficient RFI radiators (see Sect. 2.5).
- Sensitive RF receiving circuits can be in the near field radiated by the digital portion of the PCB.

**Fig. 6.28** Allowable slot with analog/digital mix on PCBs



**Fig. 6.29** An example of analog/digital segregation on PCB



**Example 6.2** Assume a microprocessor module incorporating a 300 MHz clock, radiating just 10 dB below FCC Class B, at 900 MHz. On this same PCB, a cellular telephone receiving section is laid, with its receiving antenna located at 5 cm from the  $\mu\text{P}$  circuit.

The radiation from the  $\mu\text{P}$  module is estimated from its FCC Class B compliance:

$$46 \text{ dB}\mu\text{V/m} - 10 \text{ dB} = 36 \text{ dB}\mu\text{V/m} \text{ at } 3 \text{ m}$$

The near-/far-field transition for 900 MHz is  $D_{(\text{NF-FF})} = 48/F = 0.05 \text{ m}$ .

Therefore, the 36 dB $\mu\text{V/m}$  field at 3 m can be transposed to 5 cm as

$$E(\text{at } 5 \text{ cm}) = E(\text{at } 3 \text{ m}) + 20 \text{ Log}(3/0.05) = 36 \text{ dB}\mu\text{V/m} + 36 \text{ dB} = 72 \text{ dB}\mu\text{V/m}$$

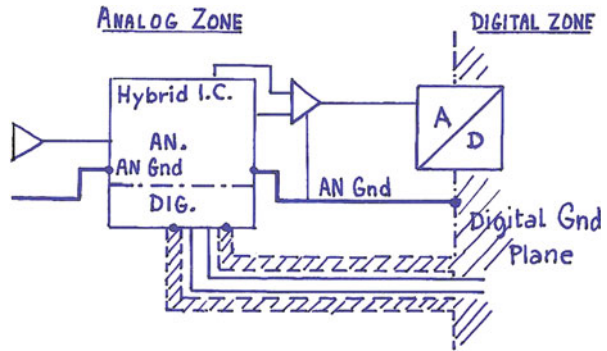
The typical sensitivity of a 900 MHz mobile phone is -100 dBm (7 dB $\mu\text{V}$ ), which can be translated into an equivalent field strength by using a typical antenna factor, ending in 34 dB $\mu\text{V/m}$  of minimum discernible field. Comparing with the field radiated by the processor section nearby,

$$72 \text{ dB}\mu\text{V/m} - 34 \text{ dB}\mu\text{V/m} = 38 \text{ dB} \text{ (a 80 times factor)}$$

Therefore, the parasitic field received at 900 MHz from the  $\mu\text{P}$  circuit is almost 100 times stronger than the RF signal sensitivity. This requires drastic protection of the RF input traces, notwithstanding that of the RF module itself (see shielded ICs, Chap. 2).

Because of such risks, the PCB zoning and DC distribution cleanup at the digital-to-analog interface must be carefully applied. Since, typically, 40-50 dB of decoupling is needed, simple capacitive filtering is generally not enough, and three-stage filter like the feedthrough or SMT “T” style must be provided (see Chap. 9). If an IC module (ASIC, DSP, etc.) performs both analog and digital functions, the dilemma arises as to where it should be located: if placed in the digital section, there is risk of having few analog input/output traces in the middle of noisy logic circuits, and if placed in the analog section, the risk is just the opposite. The best would be to have a module with all critical analog pins, including DC voltages and analog Gnd on the same side and all noisiest logic pins on the other side, allowing the module to be mounted exactly over the AN/DIG interface of the board. However, this is not always possible. A solution in this case (Fig. 6.30) is to locate the AN/DIG module in the analog area, with the digital I/O traces, including  $V_{\text{cc}}$ , enclosed between two wide digital ground traces, such that the digital portion of the IC becomes an “extension” of the PCB digital section.

**Fig. 6.30** Zoning trade-off with a mix AN/DIG module



### 6.4.7 Thin Foil PCBs

The growing trend to miniaturized equipment (laptop PCs, notepads, cameras, iPhones) has called for printed circuits, which are thinner and offer more density than the traditional 1-1.6 mm epoxy glass. This is the case of the RCC (resin-coated copper) where a 5  $\mu\text{m}$  (0.25 mil) copper foil is laminated with a 50  $\mu\text{m}$  resin. This allows for traces that are thinner than the highest-density Class 5 PCB. Trace widths of 50-75  $\mu\text{m}$  (2-3 mil) are obtainable, with 50  $\mu\text{m}$ -diameter microvias. Ultrathin multilayers are made by stacking several RCC foils. The small thickness and absence of glass fibers make the precision drilling of vias by laser economically feasible, including blind vias where needed.

Considering the scaling factor, thin foil PCBs are not much different from regular multilayers, since the width/height ratios for traces above ground plane are comparable. Thus, self-inductance and crosstalk coefficients are similar. The major difference is the trace DC resistance, reaching 0.7  $\Omega/\text{cm}$  for a 50  $\mu\text{m}$ -wide, 5  $\mu\text{m}$ -thick trace, such as resistive voltage drop can become an element of concern.

## 6.5 CROSSTALK CONTRIBUTION TO RADIATED EMI

Crosstalk occurs when a wire or trace carrying fast signals is running parallel to another conductor. By mutual capacitance and inductance, the *culprit* conductor induces a certain percentage of its voltage into the *victim* conductor (Fig. 6.31). Crosstalk increases with the proximity of the culprit and victim wires, increasing frequency (or faster rise times) and higher victim impedance. It also increases when the culprit and victim conductors are far from their return wire or plane.

Crosstalk is defined in dB, as follows:

$$X_{\text{talk}} \text{ (dB)} = 20 \log(V_{\text{vict.}}/V_{\text{culp.}}) \quad (6.5)$$

Therefore -20 dB of crosstalk means that for 1 V of culprit voltage, a 0.1 V spurious will appear on the victim circuit. A more detailed analysis of crosstalk can be found in [6] and [18]. At first glance, crosstalk is primarily an internal, functional EMC concern. The designer will worry mostly about crosstalk causing a self-disturbance in his equipment. But in fact, crosstalk is a subtle and significant player in the generation of radiated EMI. High-speed clocks and HF circuits that are used only for internal functions may unintentionally couple into I/O lines by crosstalk, then radiate. As such, crosstalk reduction is a radiated EMI concern as well as an internal concern.

Based on the CM current criteria described in Sect. 4.3, it can be calculated that for a reasonable probability of staying below FCC (or CISPR) radiated levels, the undesired harmonics induced internally on traces that later exit as I/O cables should not exceed the following levels:

- For FCC Class B: 1 mV per harmonic, at frequencies >30 MHz
- For FCC Class A: 3 mV per harmonic, at frequencies >30 MHz
- For MIL-STD-461-RE102: 1 mV per harmonic, at frequencies >30 MHz

This is assuming a “bare bones” situation with unshielded cables, unfiltered I/O ports, and poorly balanced (10%) I/O links.

To achieve this, with typical digital pulses of 3-5 V peak amplitudes, the internal couplings between culprit and victim traces must not exceed -60 dB (i.e., 1/1,000) for signals having a fundamental frequency around 30 MHz. This is much more restrictive than what it would take to simply avoid self-jamming.

### 6.5.1 Capacitive Crosstalk

Although both magnetic and capacitive mechanisms exist, the capacitive crosstalk generally predominates in PCBs because of the high dielectric constant of epoxy. For the equivalent circuit in Fig. 6.31, crosstalk expresses by

$$X_{\text{talk}} \text{ (dB)} = 20 \text{Log} \left\{ (\omega R_v(C_{1-2}) / \sqrt{[\omega R_v(C_2 + C_{1-2})^2 + 1]}) \right\} \quad (6.6)$$

The simplified prediction in Table 6.1 gives average values of capacitive crosstalk per centimeter length for few typical trace-to-trace distances. For longer runs, crosstalk increases proportionally to length in cm.

The table has been scaled as a function of the  $s/h$  ratio which we found more practical than  $d/h$  (center to center), which is sometimes used. This  $d/h$  ratio has

been shown in parenthesis, for reference. The value of  $C_2$ , trace to ground capacitance has been shown as it governs the maximum possible  $X_{\text{talk}}$ , given by

$$X_{\text{talk}} (\text{max}) = 20 \text{Log}[C_{1-2}/(C_{1-2} + C_2)] \quad (6.7)$$

The last column on the right corresponds to a PCB without ground plane, such as no firm value can be given to  $C_2$ , other than an approximate default value of 0.2 pF/cm. This is assuming that the corresponding ground trace is farther away than the traces separation itself.

Crosstalk increases linearly with the length of the parallel run, as long as this one is small compared to the culprit wavelength. As length or frequency increases, a point is reached where crosstalk will not increase anymore. Since the victim voltage is of a general form ( $V_c \cdot R \cdot C_{1-2} \cdot \omega \cdot \cos \omega t$ ), this maximum value at a given frequency is the sum of the cosine terms over a segment equal to half wavelength. This corresponds to a weighted length of  $0.7\lambda\sqrt{2}$ , corrected by  $\sqrt{\epsilon_r}$  for the wave speed in epoxy. The limit is translated into a maximum coupling length of 5,000 cm/F (MHz). In the table, notice how  $C_{1-2}$  values are falling off rapidly with the separation distance when there is a ground plane and very weakly when there is no ground plane.

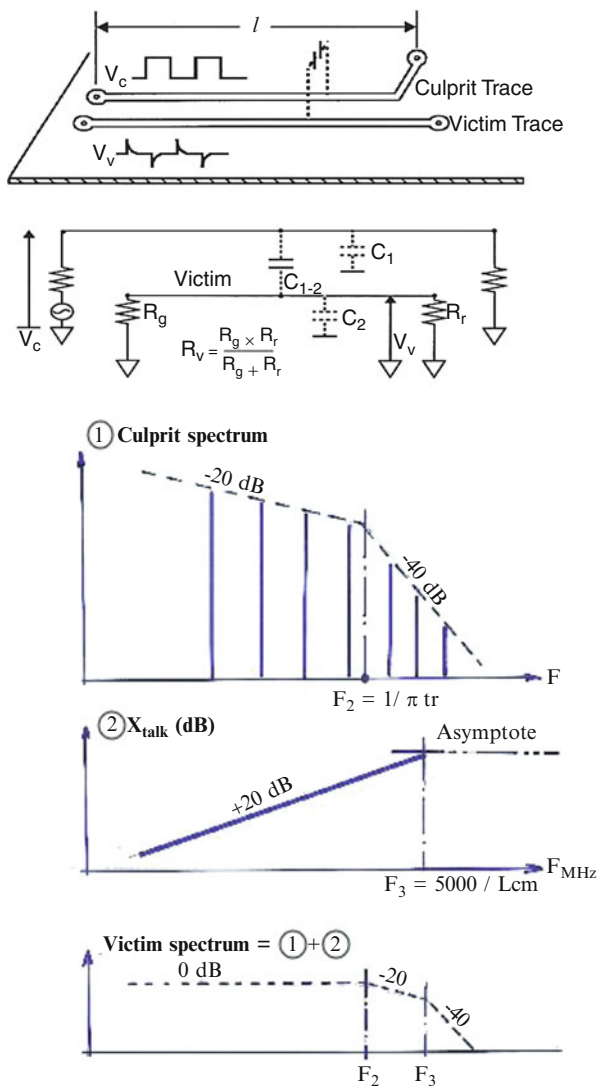
The procedure in using this simplified Table 6.1 and model is as follows:

1. Select (or interpolate) the cross-section geometry of the culprit/victim traces.
2. Define the culprit frequency (or frequencies). This may require a quick Fourier analysis of the culprit signal, based on the repetition frequency and rise time. *Time-domain calculation of crosstalk is not recommended here*, as we need to determine the harmonics of the coupled voltage.
3. Find the corresponding crosstalk (dB) per cm length.
4. Apply length correction =  $20 \log(\text{cm})$ . Do not use above  $\ell_{\text{max}} = 5,000 \text{ m/F (MHz)}$ , corresponding to  $\lambda/2$  maximum coupling length in epoxy dielectric.
5. Apply impedance correction:  $20 \log(Z_{\text{victim}}/100)$ , if  $Z_{\text{victim}}$  (source and load in parallel) is  $\neq 100 \Omega$ .

If the  $\lambda/2$  limit has been passed, replace  $Z_{\omega \text{ victim}}$  by the victim trace characteristic impedance  $Z_0$ , shown in the upper case of the table.

6. At any frequency, whatever is the result of length + impedance corrections, the *maximum possible crosstalk cannot exceed the clamp value* shown at the bottom of the table.
7. If the victim trace is sided by two identical culprit traces, the two crosstalks are adding up, i.e., 6 dB are added to the calculated value.
8. Although this table is for surface traces, it can be extended to buried traces. The  $C_{1-2}$  capacitance for buried strips is approximately 0.5 times that of surface traces (6 dB less  $X_{\text{talk}}$ ), provided that the value entered for "h" is that of the trace above the plane.  $C_2$  is exactly double and  $Z_0$  about  $\sqrt{2}$  times lower; therefore, the limit of maximum  $X_{\text{talk}}$  is  $\approx 10$  dB lower.



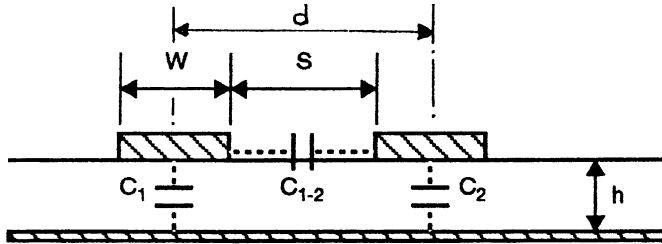


**Fig. 6.31** Basic mechanism for capacitive crosstalk. *Top:* Equivalent circuit. *Bottom:* Frequency domain

**Example 6.3** Two traces have a 10 cm parallel run on a single-layer board without Gnd plane (Fig. 6.24) with the following:

- $w = 15\text{ mil}$  (0.38 mm).
- $s = 15\text{ mil}$  (0.38 mm).
- Board thickness,  $h = 1.2\text{ mm}$ .
- All ground traces or ground areas are more than 1.2 mm ( $3 \times w$ ) away.
- Culprit is a 5 V, 30 MHz clock with  $t_r = 2\text{ ns}$  (i.e., second corner frequency is 160 MHz).

**Table 6.1** Capacitive crosstalk between PCB traces, in dB, for  $R_v$  (total) = 100  $\Omega$  and 1 cm length. For other values of length and  $R_v$ , apply the correction:  $20 \log [\ell(\text{cm}) \cdot R_v/100]$ . The clamp in dB on the bottom line is the maximum possible crosstalk, ever. For buried traces, the clamp is 10 dB lower.



$C_2$ $Z_0$	$w/h=3$ 1.6pF/cm 40 $\Omega$			$w/h=1$ 0.8pF/cm 70 $\Omega$			$w/h=0.3$ 0.5pF/cm 120 $\Omega$			$\bar{w}/h=0.3-0.6$ No Gnd Plane					
$s/h$	10	3	1	10	3	1	0.3	10	3	1	0.3	10	3	1	0.3
corresp.	(13)	(6)	(4)	(11)	(4)	(2)	(1.3)	(10.3)	(3.3)	(1.3)	(6)	(10.4)	(3.4)	(1.4)	(.9)
$d/h$															
$C_{1-2}$ (pF/cm)	.016	.06	.16	.007	.04	.14	.25	.003	.03	.1	.2	.18	.22	.35	.5
<b>Freq.</b>															
1kHz	-160	-148	-140	-167	-152	-141	-136	-174	-154	-144	-138	-139	-137	-133	-130
3kHz	-150	-138	-130	-157	-142	-131	-126	-164	-144	-134	-128	-129	-127	-123	-120
10kHz	-140	-128	-120	-147	-132	-121	-116	-154	-134	-124	-118	-119	-117	-113	-110
30kHz	-130	-118	-110	-137	-122	-111	-106	-144	-124	-114	-108	-109	-107	-103	-100
100kHz	-120	-108	-100	-127	-112	-101	-96	-134	-114	-104	-98	-99	-97	-93	-90
300kHz	-110	-98	-90	-117	-102	-91	-86	-124	-104	-94	-88	-89	-87	-83	-80
1MHz	-100	-88	-80	-107	-92	-81	-76	-114	-94	-84	-78	-79	-77	-73	-70
3MHz	-90	-78	-70	-97	-82	-71	-66	-104	-84	-74	-68	-69	-67	-63	-60
10MHz	-80	-68	-60	-87	-72	-61	-56	-94	-74	-64	-58	-59	-57	-53	-50
30MHz	-70	-58	-50	-77	-62	-51	-46	-84	-64	-54	-48	-49	-47	-43	-40
100MHz	-60	-48	-40	-67	-52	-41	-36	-74	-54	-44	-38	-39	-37	-33	-30
300MHz	-50	-38	-30	-57	-42	-31	-26	-64	-44	-34	-28	-29	-27	-23	-20
1GHz	-43	-31	-23	-47	-32	-21	-18	-54	-34	-24	-18	-19	-17	-13	-10
<b>Asymp.</b>	-40	-29	-21	-40	-26	-16	-12	-44	-25	-16	-11	-7	-6	-4	-3

$$\text{Crosstalk} = 20 \log \frac{R_{\text{victim}} C_{1-2} \omega}{\sqrt{[R_v \omega (C_2 + C_{1-2})]^2 + 1}}$$

- The receiving trace impedance consists in the input of a data line receiver ( $\gg 1 \text{ k}\Omega$ ) in parallel with the characteristic impedance of an I/O pair,  $Z_0 = 125 \Omega$ , so  $Z_{\text{vict}} \approx 125 \Omega$ .

Estimate the crosstalk at Harmonic #3, #5, and #9 frequencies with respect to RF pollution of the nearby I/O wiring (Fig. 6.32).

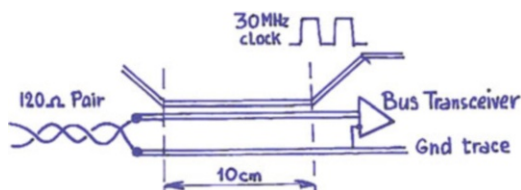


Fig. 6.32 Configuration as in crosstalk Example 6

**Solution** Starting with the Harmonic #3 amplitude of 1 V, calculated values are as follows, for  $w/h = 0.3$ ,  $s/h = 0.3$ , and no ground plane:

$X_{\text{talk}}$ at:	90 MHz	150 MHz	270 MHz
1. Table value (dB/cm)	-31	-26	-21
2. Length correction for 10 cm (10 cm is $< \lambda/2$ ) <sup>a</sup>	+20	+20	+20
3. Impedance correction	+2	+2	+2
4. Total $X_{\text{talk}}$ coefficient	-9	-4	(+1) <sup>b</sup> clamp to -3 dB
5. $V_{\text{culprit}}$ (from Fourier spectrum)	0 dBV	-5 dBV	-16 dBV
6. $V_{\text{victim}} = \#4 + \#5$	-9 dBV (0.35 V)	-9 dBV (0.35 V)	-19 dBV (0.11 V)

<sup>a</sup>The 10 cm length correction will stand up to  $F = 5,000/10 = 500 \text{ MHz}$ . Above this, the  $X_{\text{talk}}$  coefficient will not increase any more

<sup>b</sup>Crosstalk cannot be positive nor exceed the maximum clamp value in the table

These voltages are differential, trace-to-0 V. Taking into account a DM-to-CM conversion of -10 dB for unbalanced link (see Sect. 2.5), this is about 40 dB higher than the permissible voltage excitation for long I/O cables, if FCC Class B compliance is desired (see criteria in par. 6.5), and 30 dB too high if Class A is the goal. Therefore, a crosstalk reduction is in order, as discussed next. Otherwise, shielded I/O cables or filtered I/O connectors will be needed. Notice that, as frequency increases, the harmonic amplitude decreases but  $X_{\text{talk}}$  coefficient increases (Fig. 6.31), resulting in an approximately constant victim voltage. Thus, with periodic rectangular pulses, crosstalk-coupled voltages are  $\approx$  constant with frequency and do not depend on the basic repetition rate, until the second-corner frequency,  $1/\pi t_r$ , is reached.

There are several ways to decrease capacitive crosstalk in PCBs:

1. Increase culprit-to-victim spacing; there is a limited latitude for doing this. Without ground plane, it would takes a tenfold increase in distance (changing from  $s/h = 1$  to  $s/h = 10$ ) to lose  $< 6 \text{ dB}$  of crosstalk. Most of the time, there is

not enough empty room on a PCB to allow generous spacing. A three times increase in spacing will save about 3 dB of coupling, always good to get, but seldom sufficient. A variation of this consists of increasing “ $s$ ” by simply reducing the width (if possible), while keeping the same center-to-center spacing, but this too will not bring a drastic reduction.

2. Decrease the length of the parallel run; crosstalk will decrease in proportion.
3. Preferably, run the culprit and/or victim traces above the return plane or traces. A similar tenfold increase in separation as in #1 will reduce crosstalk by 20-30 dB, decreasing  $C_{1-2}$  and increasing  $C_1$  or  $C_2$ . Multilayers, in this respect, offer more possibilities for crosstalk reduction.
4. Insert a grounded trace (guard trace) between the culprit and victim traces. This guard trace should be grounded at least at each end and more frequently if possible. A grounded trace inserted at the halfway point reduces crosstalk, on typical  $\leq 10$  cm runs, by at least 20 dB up to 100 MHz. As an extension of the above, high-speed culprit traces could be “buried” in a ground land at the same level. But do not slot an existing 0 V reference plane to do this (see the previous Sect. 6.4). In lieu of a ground conductor, any trace that (a) remains on the same PCB (does not exit) and (b) is tied to low-impedance ( $\ll 100 \Omega$ ) circuits like DC lines, bias voltage, status line at “0” level, etc. can be used as a substitute guard trace.

In summary, the best way to avoid I/O line pollution from internal high-frequency circuits is to strictly ban close parallel runs that do not have at least a ground trace between them.

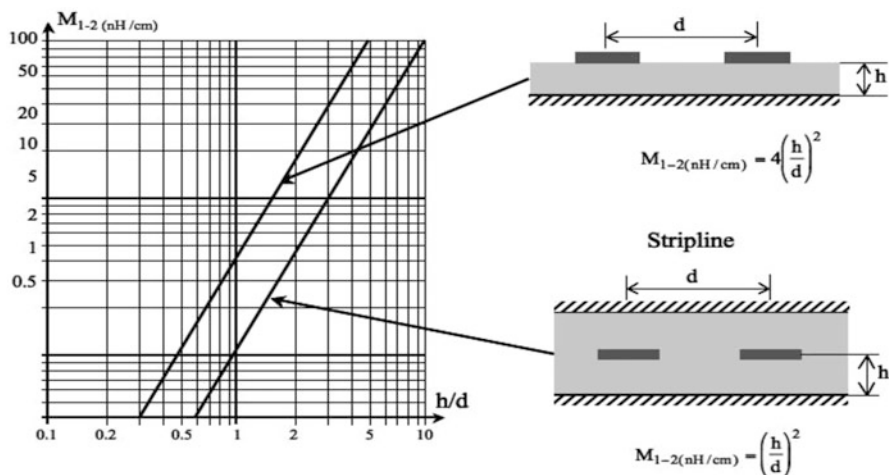
## 6.5.2 Magnetic Crosstalk

For traces carrying larger currents, like those with characteristic impedance of 50  $\Omega$  or less driven by bus transceivers, the magnetic contribution to crosstalk may not be negligible [10]. At worst, magnetic and capacitive crosstalk may combine as additive at the victim’s near end (the side which is close to the culprit generator side). Figure 6.33 shows the mutual inductance value,  $M_{1-2}$ , in nH/cm between two adjacent traces. The *full* voltage coupled on the victim loop is calculated by

$$V_{\text{vict}} = M_{1-2}\omega I_{\text{culp}}$$

Buried traces (striplines) produce significantly less magnetic crosstalk than surface traces (microstrip). Unlike trace-to-trace capacitances of Table 6.1, it is not possible to give a typical value for mutual inductance when there is no ground plane underneath, since  $M_{1-2}$  will depend strongly on the distance to the nearest ground trace. Trace width does not affect much mutual inductance, but width plays a role in the trace self-inductance,  $L$ , which governs the characteristic impedance (hence, the maximum culprit current) and the maximum possible crosstalk ratio  $M/L$ .

Although a full treatment of magnetic crosstalk would outgrow the purpose of this book, we will describe one practical example, related to our radiated emission topic.



**Fig. 6.33** Mutual inductance  $M_{1-2}$  (nH/cm) between PCB traces vs. center-to-center trace separation

**Example 6.4 (Magnetic Crosstalk in Multilayer PCB)** Culprit circuit: internal bus, operating at 5 V/30 MHz. The maximum load, for a long trace, is given by *culprit trace* characteristic impedance of 100  $\Omega$ .

Culprit-victim separation  $d$ : 0.5 mm height above ground: 0.4 mm.

Microstrip configuration. Parallel length: 6 cm.

Calculate magnetic crosstalk at the fundamental, Harmonic #3 and #5 frequencies, since the victim trace is an I/O line, candidate to EMI radiation.

Frequency	30 MHz	90 MHz	150 MHz
$V_{\text{culp}}$ (from Fourier spectrum)	3 V	1 V	0.6 V
$I_{\text{culp}} = V/100 \Omega$	30 mA	10 mA	6 mA
$M_{1-2}$ (nH/cm)	2.5	2.5	2.5
$M_{1-2}$ for 6 cm	15	15	15
$V_{\text{vict}} = M_{1-2} \times 2\pi F \times I =$	85 mV	85 mV	85 mV

This calculated victim’s voltage is the total loop-induced voltage. It is shared by the two termination resistances, the larger one (generally the receptor end) taking the largest part. Checking for  $\lambda/2$  clamp, at the highest frequency of 150 MHz, the coupling length is  $<5,000/F$ . Notice that, because the large value of  $I_{\text{culp}}$  and in spite of the ground plane, this is a significant coupling causing a sizable noise on victim trace. Although about three times less than capacitive crosstalk for a similar geometry, at 150 MHz the  $X_{\text{talk}}$  ratio is 85 mV/600 mV, that is, -17 dB. Our limit objective for maximum crosstalk is exceeded.

This last example was assuming a low impedance for the culprit circuit, with a corresponding large current. While such a condition is not very frequent in ordinary PCBs, it is extremely common in backplanes with high-speed parallel bus (see Chap. 7).

### 6.5.3 Combined Effects of Capacitive and Magnetic Crosstalk

A question often arises: when the magnetic coupling is not negligible, how do the two  $X_{talks}$  combine on the victim's line? Do they add up? Subtract? Combine in an rms addition? The subject could easily fill up a respectable chapter, and reports, thesis, or symposium lectures on this sole topic are in no short supply. For this book, where only the possible contribution of crosstalk to radiated emissions does matter, we will concentrate on the essentials: capacitive and magnetic  $X_{talk}$  effects combine as follows on the victim's terminal impedances:

- (a) Capacitive  $X_{talk}$  acts as a current source attacking the victim's generator and load impedances in parallel. The capacitive current splits in two branches with the same sign, before returning to the culprit's negative terminal.
- (b) Magnetic  $X_{talk}$  acts as a voltage source appearing in series in the victim's loop. Its current does not return to the culprit circuit.
- (c) As a result on the victim's end that is close to the culprit source, termed "near end," capacitive and magnetic crosstalk currents are adding up (Fig. 6.34).
- (d) All the same, on the victim's end that is opposite, termed "far end," capacitive and magnetic crosstalk currents are subtracting.

Depending on the respective amplitudes of each contribution, this combination can be minimal or significant.

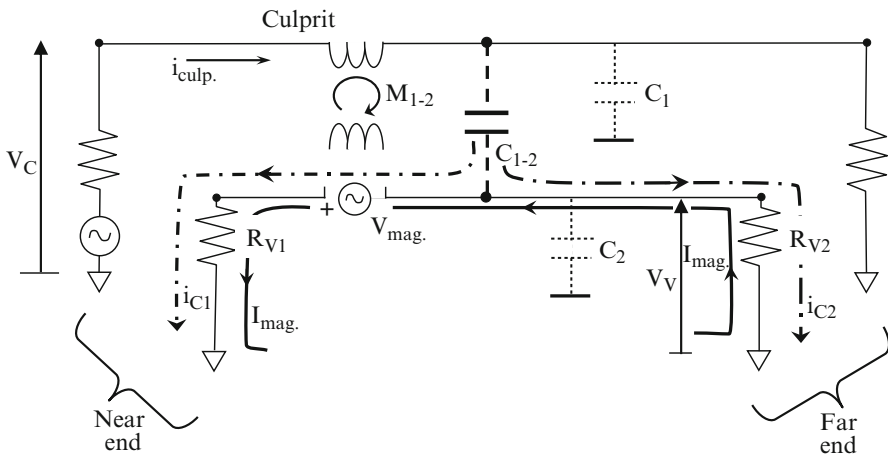


Fig. 6.34 Combined effects of capacitive and magnetic crosstalk

## 6.6 IMPEDANCE MATCHING

With increasing frequencies (or shorter rise times), traces tend to become electrically “long,” i.e., the propagation delay along this line becomes non-negligible compared to the wave front rise time. At this juncture, it is imperative to terminate the line in a matched load to avoid pulse ringing. Here again, we have a case where something that could be a purely functional concern becomes an EMI radiation issue. Unterminated lines will exhibit oscillations that, in addition to possible functional problems, can be as much as double emissions and crosstalk levels (see Fig. 6.35). There is an abundant and accurate supply of literature about transmission line matching, and the subject is beyond the scope of this book. We will simply give some basic guidelines.

### 6.6.1 Parasitic Oscillations with Mismatched Lines

An electromagnetic wave propagates at a speed:

$$\begin{aligned} C &= 3 \times 10^8 \text{ m/s or } 30 \text{ cm/ns in free space} \\ &= 30\sqrt{\epsilon_r} \text{ cm/ns in a medium with dielectric constant } \epsilon_r \end{aligned}$$

For instance, with standard PCB,  $\epsilon_r$  is 4-4.5, so propagation delay over a length  $\ell$  will be

$$T_d = \ell\sqrt{\epsilon_r}/30 \quad (6.8)$$

with  $T_d$  in ns and  $\ell$  in cm; therefore,  $T_d = 0.07$  ns/cm or 7 ps/mm.

This would be for lines entirely buried in epoxy. If the signal and return traces are both on the same surface (one-sided, single-layer board), part of the electromagnetic wave propagates in air instead, and the dielectric constant to use is approximately

$$\epsilon_r' = (1 + \epsilon_r)/2 \quad (6.9)$$

when  $T_d$  exceeds  $t_r/2$  (half the signal rise time) that is approximately when, in PCBs:

$$T_r(\text{ns}) < 0.14 \ell(\text{cm}) \quad (6.10)$$

the line must terminate on a resistance equal or as close as possible to the line characteristic impedance.

It is easy to calculate the ringing overshoot with improper terminations, given that the reflection coefficient at the end of the length  $\ell$  loaded by  $Z_L$  is

$$\rho = (Z_L - Z_0)/(Z_L + Z_0) \quad (6.11)$$

The characteristic impedances,  $Z_0$ , for typical trace geometries are shown in Fig. 6.36. Eventually, 90° corners create an abrupt discontinuity (locally,  $L$  and  $C$  are modified). To reduce the VSWR at this discontinuity, right-angle turns should be made by two 45° corners.

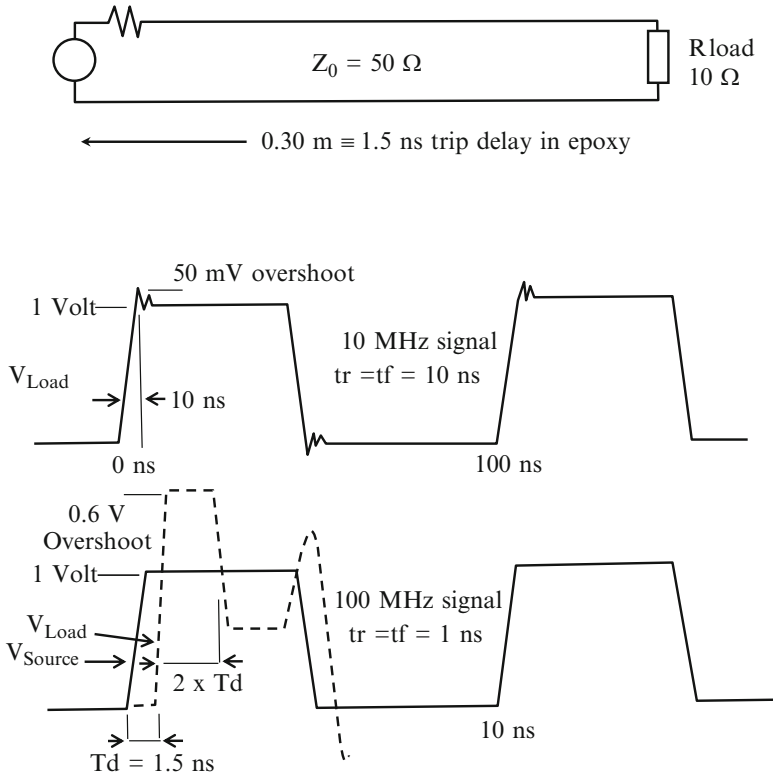


Fig. 6.35 Example of mismatch problems with fast rise times, shown for 20 cm line

Correct termination can consist in:

- A resistance equal to  $Z_0$  (with the drawback of wasting power during the DC plateau of digital pulses).
- A set of pull-up/pull-down resistor pairs, such that their parallel combination approximates  $Z_0$ , but only half the power is wasted since digital pulses will be either high or low.
- A series RC network across the line end, such that termination  $R$  is only seen during the propagation delay,  $T_d$  (the only time where matching is needed). Compact sets of such RC networks in single in-line (SIP) packages are available, with values of  $C$  ranging from 10 to 500 pF.
- A series resistor on the source side. This solution allows one reflection to occur, but the reflected wave terminates on a matched end and does not bounce back. It has the drawback of affecting the drive capability of the source device and can only be used with point-to-point links.
- As an alternate to the above, a small, few 100 nH ferrites can fill up the need for matching, by smoothing the rise front. The time constant (63% crossing point)



is  $\approx$  unchanged, but the 90% rise time is doubled, so the new rise time might no longer compete with  $T_d$ .

- A clamping diode at gate input. Several vendors incorporate this diode to limit signal overshoot.

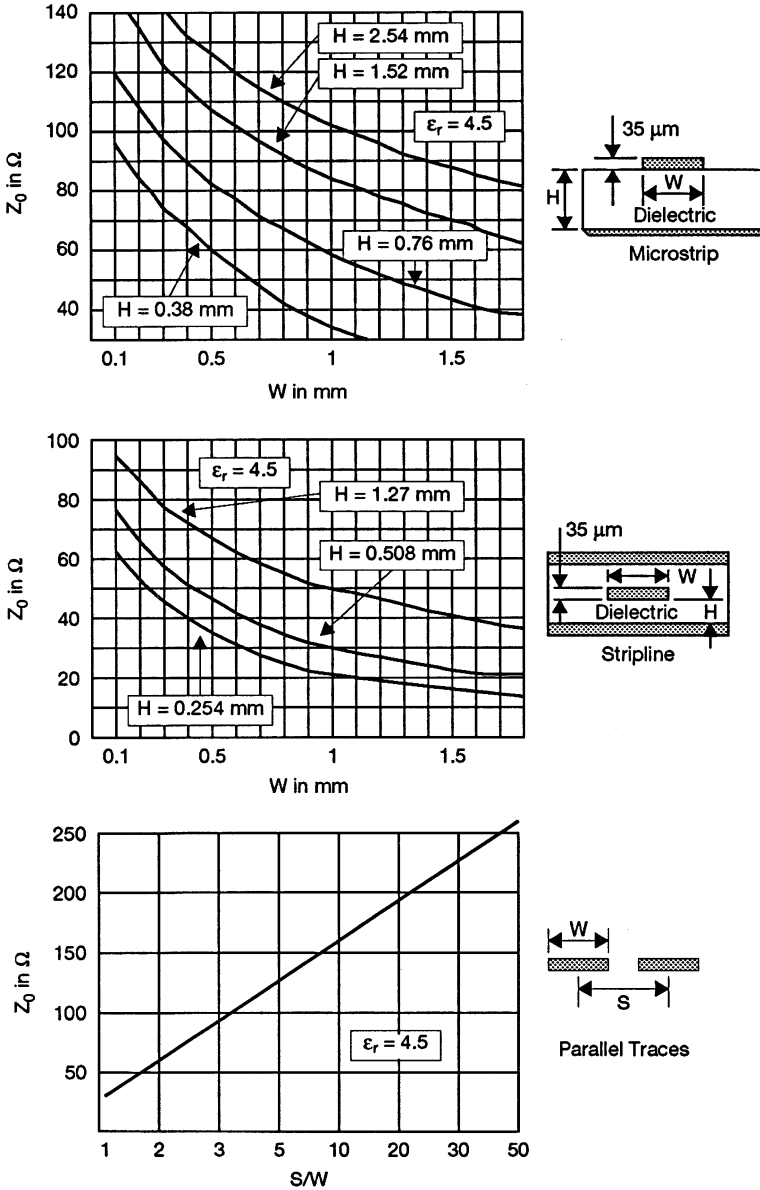


Fig. 6.36 Characteristic impedances ( $Z_0$ ) of several trace geometries

### 6.6.2 EMI Concerns with Impedance Mismatch at PCB Vias Transitions

With the exception of RF  $\mu$ waves circuits, signal or return vias were not regarded as critical EMC issues, as long as the functional frequencies did not exceed a hundred MHz. A via is a vertical, 1-1.6 mm-long cylinder allowing signals to jump from one PCB layer to another. They represent an infinitely small portion of the wavelength at 100 MHz in epoxy, where  $\lambda = 1.50$  m. When logic speeds exceed 1 GHz, rise times  $< 100$  ps are commonplace. Let us consider a 50 ps rise time: given the 7 ps/mm time delay in FR4 epoxy, a 1.6 mm via represents an 11 ps delay that is a sizeable fraction of the rise time [1, 2]. When two traces are carrying differential signals or signals that must be perfectly synchronized (Fig. 6.37), it is important that either

- They remain on a same layer, with no vertical jumps between planes
- If they change layers, they use vias that are very close, not staggered (Fig. 6.37)

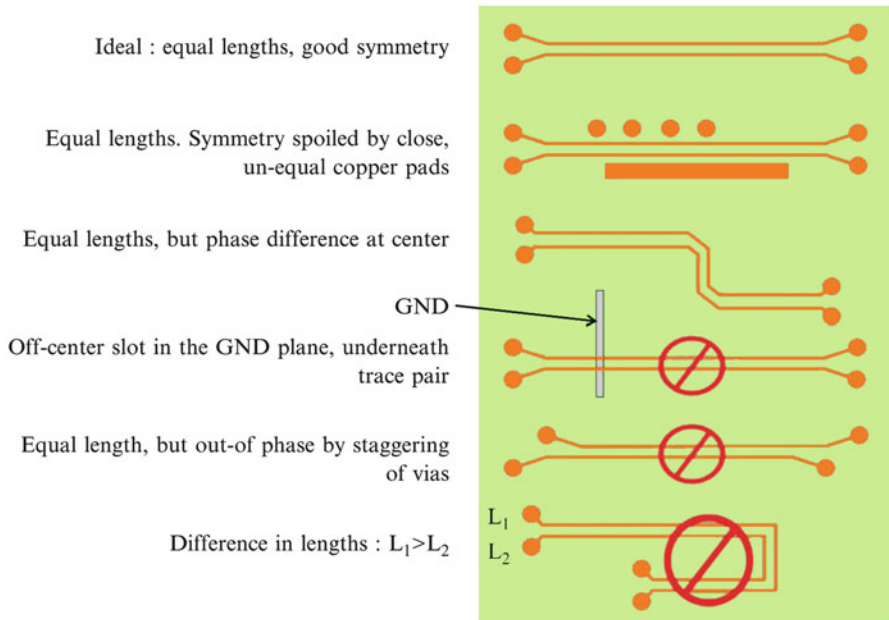


Fig. 6.37 Example of differential traces routing impairments, causing mismatch and CM noise

## 6.7 PCB CONNECTOR PIN ASSIGNMENT

As far as EMI emissions are concerned, the board-level connector parameters of concern are:

- Crosstalk
- Characteristic impedance
- Contact impedance

Board connectors may become limiting factors in circuits operating at high frequencies.

### 6.7.1 Crosstalk in Connectors

Although the coupling length may seem minuscule in a connector, the proximity of contacts embedded in a dielectric material can easily cause a contamination of I/O lines (our continuous concern) via internal high-frequency signals. For a 2.54 mm contact spacing, the 25 mm coupling length (typical of a male + female team) typically creates -40 dB of capacitive crosstalk between adjacent pins at 100 MHz (Fig. 6.38). For digital signals, this is already more than eating up our entire allocation for such coupling (see Sect. 6.5).

If the culprit pins carry more power, such as an RF signal that should not leak outside the box, an even more substantial isolation may be needed. For instance, if a video signal of several watts is leaving the board (before being driven into a coaxial line) by the same connector as an ordinary, low-speed I/O line, 60 or 80 dB isolation is required.

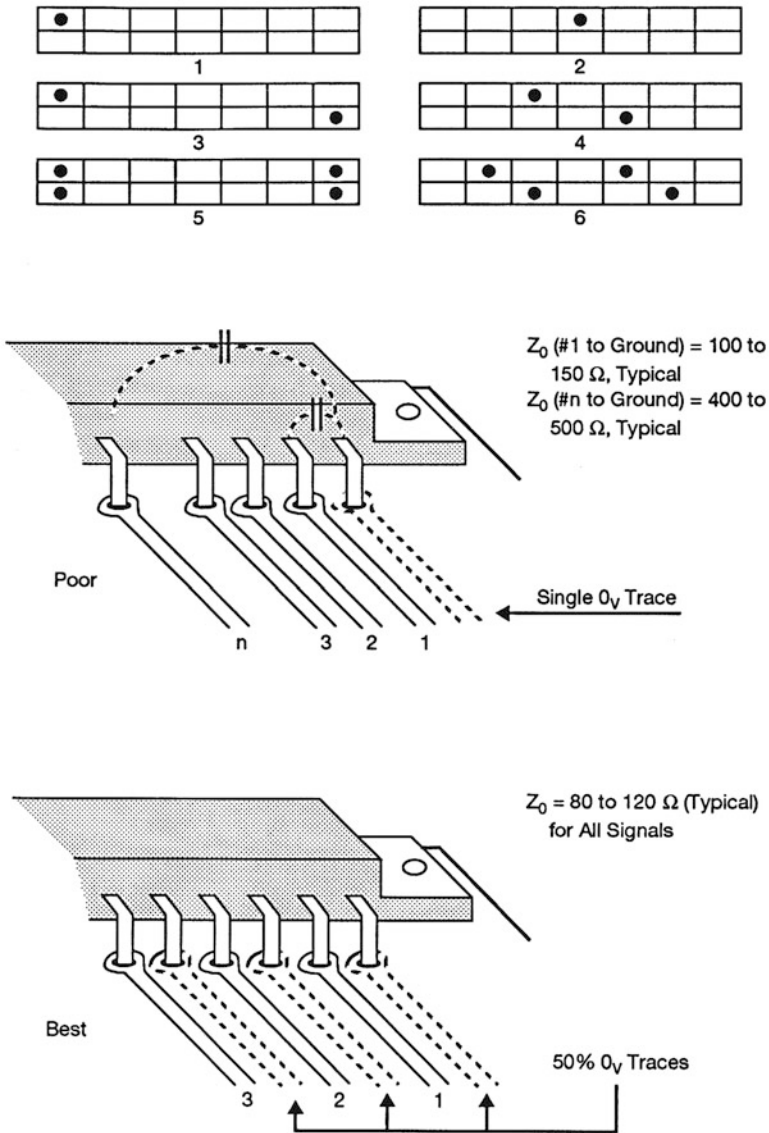
Crosstalk in connectors can be reduced by:

- Careful segregation of culprit and victim pins (simply by continuing the segregation that was done at the trace level)
- Interposition of ground pins (Figs. 6.38 and 6.39)

### 6.7.2 Connector Characteristic Impedance and Mismatch

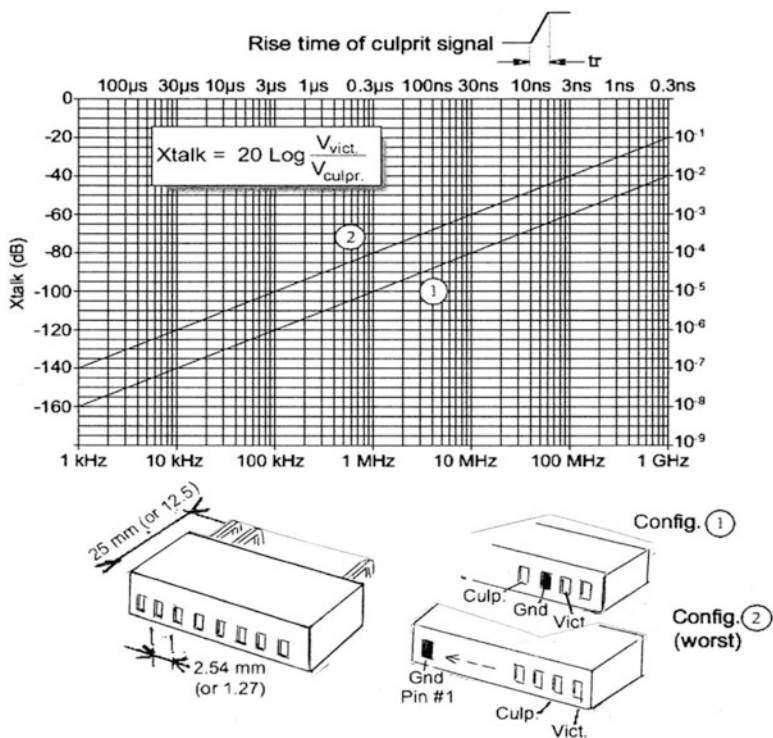
When a line enters or leaves the PCB, the mating connector should, ideally, have the same characteristic impedance  $Z_0$  to avoid mismatch. Up to about 100 MHz, this is of little importance, but when the connector length starts representing a non-negligible fraction of the signal wavelength, mismatch can cause reflections and ringing. Taking a connector pair whose total pin and body length represents about 3 cm and given a velocity in insulation of 15 cm/ns, the connector trip represents a 0.2 ns delay. Using as a rule-of-thumb  $\approx 1/10$ th of the trip delay for an indiscernible mismatch, this connector must be matched when signal rise times get shorter than 2 ns (or frequencies above 150 MHz).

Part of the mismatch problem is the fact that different distances to the ground pin, as in Fig. 6.38, not only create a different  $Z_0$  but also different propagation delays for each contact (speed and  $Z_0$  are both related through the distributed  $L/C$  in the connector). Just like for crosstalk, a good precaution is the regular insertion of ground pins or, even better, alternating pins in a signal-0 V-signal configuration for



**Fig. 6.38** Reducing crosstalk and impedance mismatch at connector crossing. At the top, performance improves from #1 to #6. The single 0 V assignment labeled “poor” creates more crosstalk between the remote pins (#n), and the odd spread of *L* and *C* parameters creates different  $Z_0$  and propagation delays

bandwidths exceeding 30 MHz. Some modern PCB connectors have a ground plane built in the connector such that, except at the soldering pin level, contact rows are below an edged ground plane (Fig. 6.41).



**Fig. 6.39** Crosstalk in typical miniature connectors with 2.54 mm (or 1.27) contact pitch, for  $Z_{vict}$  (total) = 100 Ω. If  $Z_{vict} \neq 100 \Omega$ , apply correction  $20 \log(Z_{vict}/100)$ . Capacitive  $X_{talk}$  dominates, unless culprit pin carries a significant current (that is  $Z_{culp} \leq 50 \Omega$ )

### 6.7.3 Contacts Impedance

When daughterboards communicate via backplanes or several PCBs are linked by a ribbon cable or flexprint, with the designer using ground planes for all of these circuits, unexplained EMI problems may still occur [15]. They are usually traceable to the card’s deck. The cause is an insufficient number of  $V_{cc}$  or Gnd pins being allocated at the edge connectors. This creates an inductive bottleneck at each current transition, especially with high current returns from I/O drivers sharing a single Gnd pin (Fig. 6.40). As a result, in terms of high frequencies, the board becomes “hot” with respect to the backplane. Here again, the answer is to allocate more, evenly spaced ground pins.

**Example 6.5** Assume eight simultaneous drivers at 50 mA each, with 5 ns rise time, sharing only one connector Gnd pin. Taking 2.5 cm of average length for the edge connector pins plus the lead-in trace, we get

$$\Delta V = L \sum di/dt = 2.5 \text{ cm} \times 10 \text{ nH/cm} \cdot (8 \times 50 \text{ mA})/5 \times 10^{-9} \text{ s} = 2 \text{ V}$$

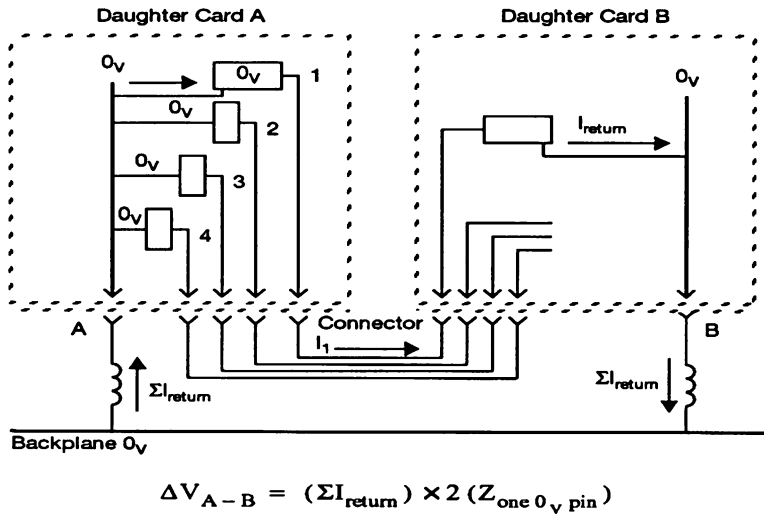
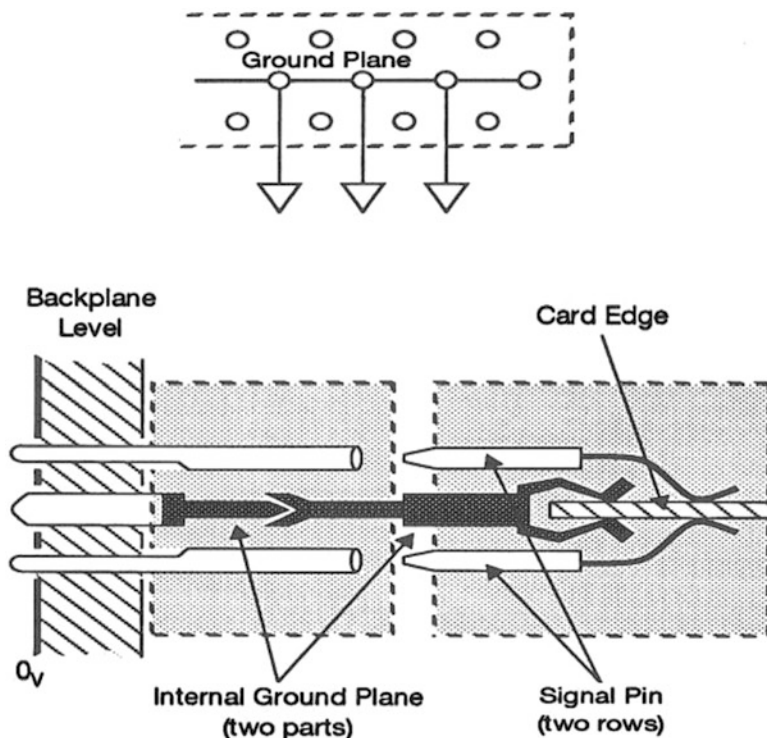


Fig. 6.40 Common impedance noise at connector crossings

The connectors’ problems described in previous sections become critical above a few tens of MHz. Therefore, with boards exchanging signals below this frequency range, the assignment scheme of Fig. 6.15 is generally sufficient. Notice, however, that this 10% of Gnd pins are evenly spread over the connector width. This spread is as important as the number of pins: a same number of Gnd pins packed on a same end would reduce DC resistance but would not reduce contact inductance to any practical extent. For higher speeds, the “one signal, one Gnd” scheme becomes mandatory, or one should use the connectors with internal Gnd plane of Fig. 6.41.

## 6.8 GROUNDING OF 0 V REFERENCE TO CHASSIS

The decision of whether to connect the PCB 0 V to the chassis must be a part of the general grounding strategy in the equipment and, furthermore, in the entire system, including its installation. Traditional low-frequency analog and audio practices have long dictated that signal reference should be isolated from chassis (then from earthed structures) everywhere but at one connection point: the center of the star grounding or SPG (single-point ground). Toward the opposite end of the frequency spectrum, RF designers, especially in the VHF/UHF and microwave domains, have always practiced multipoint grounding, where the signal reference and box skin are connected as many times as possible. Although with a single PCB one could conceivably handle signal speeds from DC to daylight, within the scope of this book, radiated EMI generally implies a high-frequency context.



**Fig. 6.41** Example of special high-speed board connector with internal ground plane. The knife-edged part on the *left* engages in a double-spring contact mating part

Therefore, even if the equipment of concern handles both low-frequency analog and high-frequency RF or digital signals, the grounding strategy should be the following:

- For the low-frequency analog circuits, keep the Gnd isolated from the chassis to avoid ground loops, except at one point, which is generally the DC power supply 0 V terminal.
- For the high-frequency circuits, connect the signal Gnd to chassis at the PCB level, as close as possible to the I/O cable entry points. This works because floating signal references become meaningless above a few MHz; the PCB to chassis capacitance (typically a few tens to hundreds of picofarads) would tend to close the loop anyway and also create parasitic resonances between the whole PCB and chassis.

Therefore, we may have several possible packaging situations:

- (a) All the electronics are mounted on a single PCB, and there is no backplane or motherboard. In this situation, the logic ground is connected to the chassis within the I/O connector zone. This should be made via a short and wide strap (no wire), a set of spring contacts, or several screws. There is an interaction here with the grounding of the power supply module, as will be addressed in Chap. 9.

- (b) The active PCBs are pluggable daughter-type, mounted on a motherboard. Because of the need to remove the cards easily, no permanent ground-to-chassis bond can be made at the daughterboards. In this case, daughterboard's Gnd plane should be continued by the motherboard Gnd plane through as many connector ground pins as possible. Motherboard ground plane is, in turn, grounded to chassis as in situation (a). Another option exists if card guides are used: ground the daughterboards via metallic guides, using spring contacts pressing on board edge traces.
- (c) For various reasons, the end user or the purchasing authority explicitly requires that the signal reference be totally floated from the chassis. In such a case, the main board should still have a chassis ground copper land, isolated from the 0 V, to serve as common area for the HF decoupling capacitors (see Chap. 9, I/O Connector Area).

## 6.9 EMC SOFTWARE TOOLS FOR PCB DESIGNS

With the endless trend for reducing the time-to-market, product engineers need a final version of their PCB which is both functionally perfect and EMC compliant within shorter time and less and less delays for prototyping and iterations. Ordinary design habits like placement and spacing rules, experience, and flair may not be sufficient. We have shown that a deterministic approach for predicting radiated EMI is achievable. When a PCB reaches a certain complexity, with several hundred nets of which more than a small percent are critical ones, a hand calculation becomes monumental. Computer simulation may be needed, and to avoid a fastidious entry of all the layout dimensions and component parameters, it is best to have the simulation software teamed with the PCB routing software. As early as 1983, a CAD program (#5300 by Don White Consultants) was commercially available. Using friendly, interactive entries and coarse trade-offs for averaging trace lengths, number of clock traces, etc., this precursor was displaying the emission spectrum from a complete PCB. Since the year 2000, software tools are available that can interface with PCB auto-routers like Mentor Graphics, Orcad, Visula, Cadence, etc. Several philosophies are used:

- (a) The EMC program is a rules checker which verifies, after the layout is made, that a precise set of rules for traces separation, guard traces, line resonances and mismatch overshoot, delays, X-Y tracking,  $V_{cc}$  decoupling, isolated copper lands, etc. are not violated (e.g., "Design Adviser" by Zuken-Redac).
- (b) The EMC program is a field equations solver, calculating the radiated field for each trace, combining them into a global field at the prescribed test distance.
- (c) Instead of using typical waveforms derived from the specific logic technologies, the EMC program may extract the results from a signal analysis software which calculates first the exact signal waveforms, including the influence of  $X_{talk}$ , mismatch, etc. Then these actual signal characteristics are used to calculate the radiated field (e.g., "Presto" by HDT or "Quantic EMC").



In all cases, the program provides a display of rules violation (a) or radiated field spectrum (b), with a list of the nets which are responsible.

As of the time of this writing, the major critique regarding these software tools is that they are essentially post-layout analyzers, not interactive expert systems. Once the culprit traces have been spotted, one has to re-route them differently, which means a new run of the auto-router will have to move dozens of other traces to accommodate the relocation. A new PCB layout will result, which may solve the original problem but uncover a few new culprit traces, etc. The process is usually a converging one, but is extremely hungry in CPU time. For instance, a typical field solver was taking 1 h on a Pentium dual-core processor to plot the radiation from a circuit with one single IC, at one frequency. Therefore, the next step toward a truly helpful software would be an EMC package that automatically guides the auto-router into a successful “virtual PCB prototype,” at the first pass. For their 3-day class on EMI radiation control, D.L.S. Electronic Systems, Inc. has generated software that performs many of the calculations presented here [16].

## 6.10 SUMMARY OF RADIATION CONTROL AT PCB LEVEL

Reducing emissions really starts at the board level. Briefly, the proper approaches are the following:

Common rules for ALL boards:

1. Decouple  $V_{cc}$  for every module (or every two modules) with 10 nF to 100 nF capacitors. Use ceramic and, if possible, leadless components. For RAM, micro-processors, and pin grid arrays, use 220-470 nF. Decouple again  $V_{cc}$  at the edge connector with 1-10  $\mu$ F capacitor.
2. Keep critical traces (master clocks, divided clocks with the same fast rise, etc.) away from board edges. For clocks  $>10$ MHz, border them with ground traces alongside.
3. At edge connectors, allocate at least every tenth pin to Gnd. Increase to every four or every other pin if impedance matching is required.
4. Check for crosstalk on long parallel runs. If I/O traces get more than 1-3 mV per discrete harmonic, increase trace spacing or add a guard trace.
5. Locate I/O driver/receivers away from the highest frequency sources, closest to their respective I/O connector pins.
6. Provide a guard ring around the board edge, tied frequently to the ground net or plane.
7. Where HC or AC logic is used and unless load-end matching is required, add a small resistor (47-100  $\Omega$ ) at the ordinary gates' output (not for buffers/drivers).
8. Force necessary changes in auto-router layout, to clear EMC rules violations.

Addition for single-layer (one- or two-sided) boards:

1. Apply one of the following practices (listed from “fair” to “best”):
  - (a) Distribute  $V_{cc}$  and Gnd by large traces  $>1$  mm, running side by side or one atop the other. Install ICs above  $V_{cc}$ /Gnd pairs, with their longest dimension in the trace direction.
  - (b) Landfill open areas with ground. Viewed in transparency, the board should look as opaque as possible.
  - (c) Implement a grid pattern of  $V_{cc}$  and Gnd traces.
  - (d) Consider adding leadless ceramic caps  $V_{cc}$  to Gnd underneath the current-hungry ICs.
  - (e) Devote one side of the board to ground plane.

Addition for multilayer boards:

1. Multilayers reduce emissions by reducing signal-to-return loop size. Do not ruin the concept by allowing slots or overlapping holes.
2. Beware of crosstalk when using inside signal layers: stagger them, or force perpendicular routings.
3. Decouple modules power distribution as for single-layer boards.
4. Do not neglect the “guard ring and guard traces rule,” even though there is a ground plane. When guard traces are run along a hot trace, which is changing level (e.g., jumping from layer 1 to layer 4), provide a ground via hole for the guard trace, close to the signal through hole.

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# Chapter 7

## Emission Control in Motherboards and Backplanes

Unless the equipment is of small dimensions, with all components housed on a single board, the design will probably include a motherboard. Although some motherboards contain active devices (bulky discrete components, power supplies, etc.), their major function is to provide interconnections between the daughter boards and the I/O lines.

One problem with motherboards is that dimensions are fairly large; therefore, all noise mechanisms are aggravated by one order of magnitude. For instance:

1. Because long parallel runs (highways) exist from one card location to another, they enhance crosstalk, which is a lesser problem with smaller PCBs.
2. Lines become electrically long and more prone to require impedance matching and other EMI reduction techniques.
3. Because backplanes may carry hundreds of interconnect lines that are in a switching state during any given strobe gate, the propensity for radiation is severe.

A good place to start, before all PCB layouts are frozen, is to complete the connector pin assignment and trace routes at the motherboard. By doing this first, undesirable proximities will be avoided, and the stage will be naturally set for a good layout of the daughter boards. For example, the designer should organize the runs by families:

- Internal-only digital runs (daughter to daughter)
- Digital I/O runs
- Analog (low level)
- Analog (high level) and power or analog video, etc.

Each family is separated from the next ones by ground traces or lands or run on different layers with a Gnd or  $V_{cc}$  plane in between.

Completing these rules,

1. No high-speed traces (e.g., clock, LSB, video) should run close to sensitive traces (analog, sense, reset) or to wires heading to I/O connectors, that is, interfacing to the outside world. This will prevent a single clock wire to contaminate many other wires via crosstalk.
2. No high-speed clocks or data wires should run without a ground trace alongside (Fig. 7.1).
3. At the very least, every tenth connector pin should be a ground pin. For lines which must respect impedance matching, this rule is reinforced to one ground pin every four signal pins, or ultimately one for each signal pin (i.e for parallel bus with rise times  $\leq 3$  ns).
4. The  $+V_{cc}$  distribution must run close to the ground traces or plane.

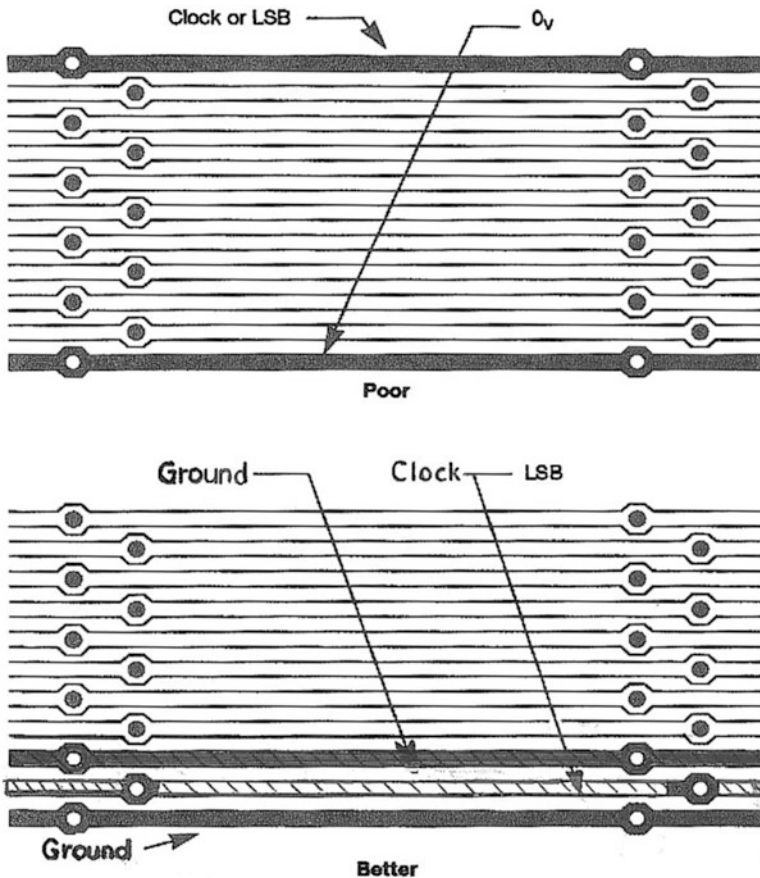


Fig. 7.1 Reducing high-speed lines loop areas in motherboards

## 7.1 WIRE-WRAPPED BACKPLANES

Although wire-wrapped designs are being phased out, particularly for active PC boards, it is still used for backplanes in such cases as (1) limited production runs and (2) equipment that must be frequently custom tailored to the buyer's requirements. We disregard here the cases of prototypes and breadboarding because such equipment does not require compliance with EMI radiation limits.

Wire wrapping is evidently more prone to HF radiation because of the larger size of the wire-to-ground loops.

To minimize this problem, the following procedures are recommended:

- Organize the wiring list so that the longer wires are mounted first. This way, they have a good chance to be close to the ground plane. (We assume that there is a ground plane.)
- Connect the shorter wires last.
- Do not try to lay the wires in an  $X$ - $Y$  pattern; rather, run them via the shortest path. These random directions will reduce radiation and crosstalk.
- Over the signal wires' wrapping, install an  $X$ - $Y$  grid of Gnd wires, interconnecting the 0 V pins of the backplane/daughter card connectors. (As explained in Chap. 6, these should include one Gnd wire for every tenth pin).

## 7.2 SINGLE OR MULTILAYER MOTHERBOARDS WITH $V_{CC}$ /GROUND PLANES

In backplanes, the general flow of signal traces being parallel, it is generally easy to provide full copper planes without obstructing signal routing. In this case, accessibility to traces is not crucial, so it is feasible to have the  $V_{CC}$  and Gnd planes on the exterior and the signal layers in between, thereby reducing radiation. The constraint mentioned with regard to multilayer PCBs remains, i.e., signal layers should not be stacked on top of each other without a ground or power plane in between. If this is not feasible, the signal traces in two stacked layers should be staggered such as they never run atop of each other.

## 7.3 CROSSTALK AND IMPEDANCE MATCHING

One reason for advising the designer to make connector pin assignments at the motherboard first was that crosstalk, radiation, and other EMI aspects are exacerbated by the "highway" nature of the signal flow. If this is done properly, the clean distribution of motherboard traces will naturally continue via the connectors at the daughter card entries. The designer must consider crosstalk and impedance matching at both levels, as described below.

### 7.3.1 Crosstalk

Crosstalk is a higher risk due to the long parallel runs. All the crosstalk aspects discussed in Sect. 6.5 are aggravated here, so the crosstalk budget must incorporate the noise picked up by I/O lines during their trip to and from the motherboard. However, chances are good that the wavelength limitation will be reached and, therefore, that the full trace length need not be entered in crosstalk estimation. With a 2 ns rise time, for instance, maximum crosstalk is reached after about 30–35 cm of trace length, and this must also incorporate the corresponding daughter card and connector length.

When the culprit or victim is a differential signal (using two traces), an interesting remedy to crosstalk in the backplane would be to twist the traces (culprit or victim, but not both). Provided that an even number of loops are created, it takes only a few twists to create a significant reduction in crosstalk and radiation. Twisting requires the traces to cross and a jumper/via-hole at each crossing, so it complicates board fabrication and is seldom used. The solution is valid, and efficient.

The remark made in Chap. 6 regarding capacitive crosstalk being the dominant mode in PCB may not stand here. Backplanes are often forcing low characteristic impedances (see next section), causing significant current loops, hence magnetic crosstalk which is adding to the capacitive crosstalk. Inductive and capacitive crosstalks are additive at the near-end side (the end that is near the culprit signal source) and subtractive at the far end. Thus, the near-end crosstalk, sometimes termed “backward,” can be twice what would be due to capacitive or magnetic couplings taken separately.

### 7.3.2 Impedance Matching

Impedance matching also is a more frequent requirement for backplanes than for daughter cards, due to the longer line length. An additional problem exists in motherboards, caused by the addition of several, periodic lumped capacitances (see Fig. 7.2) corresponding to:

- The trace enlargement at the connector via holes, where the trace enlarges into a circle
- The signal-to-ground capacitance at each connector level

The result is a decrease in the actual value of  $Z_0$  as well as the signal speed. It is not rare in multilayer backplanes to see the calculated  $Z_0$ , typically 50–70  $\Omega$ , actually dropping to 25 or 40  $\Omega$ . This means more current, hence more radiation.

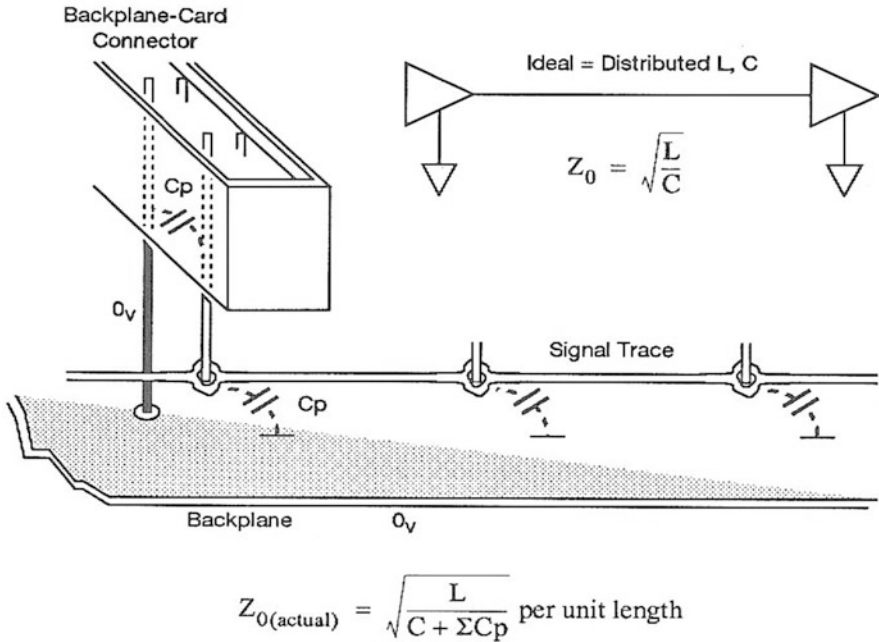


Fig. 7.2 Actual vs. ideal characteristic impedance in motherboards

## 7.4 CONNECTOR AREAS AT BACKPLANE INTERFACES

In a large equipment, the motherboard is typically fitted with end connectors for interfacing with other motherboards or the rest of the equipment. This is accomplished via flat ribbon cables or other means. The I/O connector area must continue the PCB to motherboard, noise-free concept. If high speeds are involved, the connector areas should respect impedance matching, as do the printed traces and cables. This means that alternate signal/Gnd pins may have to be provided at the end connector to avoid discontinuities in characteristic impedance.

In any case, an extension of the board ground traces or plane underneath the connector area is recommended (see Fig. 7.3). This allows the most direct connection of all the I/O signal ground returns and makes it easier to decouple directly the noisy lines at the connector level, using discrete or planar capacitors.



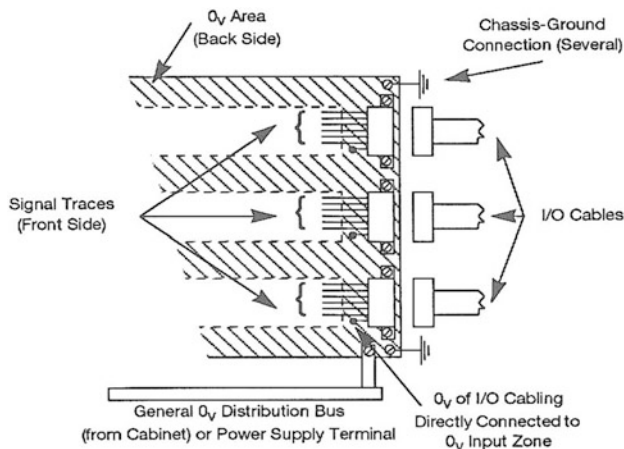


Fig. 7.3 Connector area at the motherboard (or single board) interface with external cables

## 7.5 INCREASED RADIATION IN CONNECTOR AREAS

With high-density daughter card connectors, like the DIN #41612 with four or five rows of contacts, Fig. 7.4 shows the risk of increased radiation simply caused by the connector unmasked loops. For the signal going out on pos. #5 and returning via pos. #1, the radiating loop A–B–C–D can represent easily an area of  $4 \text{ cm}^2$ , which requires only 3 mA of loop current, at 100 MHz, to exceed Class B limit. Such loop exists regardless the fact that both the daughter and motherboards may have a ground plane. The only way to reduce it is to use a male–female connector system incorporating an internal ground plane (see Chap. 6), or add more ground pins close to each signal pin.

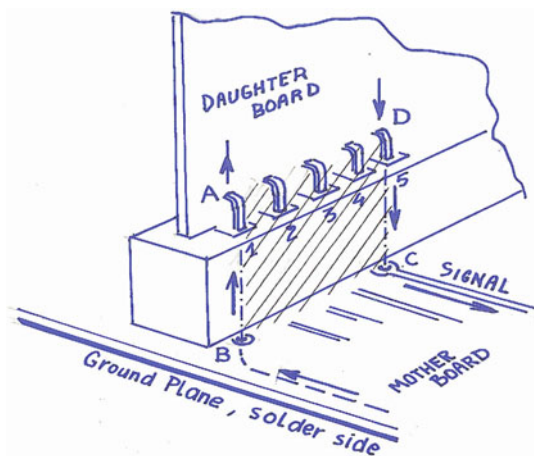


Fig. 7.4 Unmasked radiating loops caused by backplane connectors

# Chapter 8

## Controlling Radiated Fields from Switch-Mode Power Supplies

Since their introduction at the end of the 1960s, switch-mode power supplies (SMPSs) have become progressively popular, such as the vast majority of today's electronic equipment are using this type of regulator. With regard to EMI, SMPSs have always been a serious concern, primarily because of their conducted emissions but also, to a lesser extent, radiated emissions. The first aspect has been covered extensively in [2], by J. Fluke. Therefore, we will concentrate on radiated field generation and suppression.

There is no official regulation addressing power supply-radiated EMI, assuming that the device is not sold as a stand-alone item. However, more and more power supply vendors incorporate filtering and shielding in their product to lighten the burden at the host machine level. In addition to the issue of specification compliance, SMPSs can be a source of internal EMI if some sensitive circuitry is located nearby. So, depending on the design strategy, an equipment designer will have to deal with a noncompliant, homemade power supply or a compliant, commercially built one. Assuming the worst, this chapter will address radiation control from the earliest level.

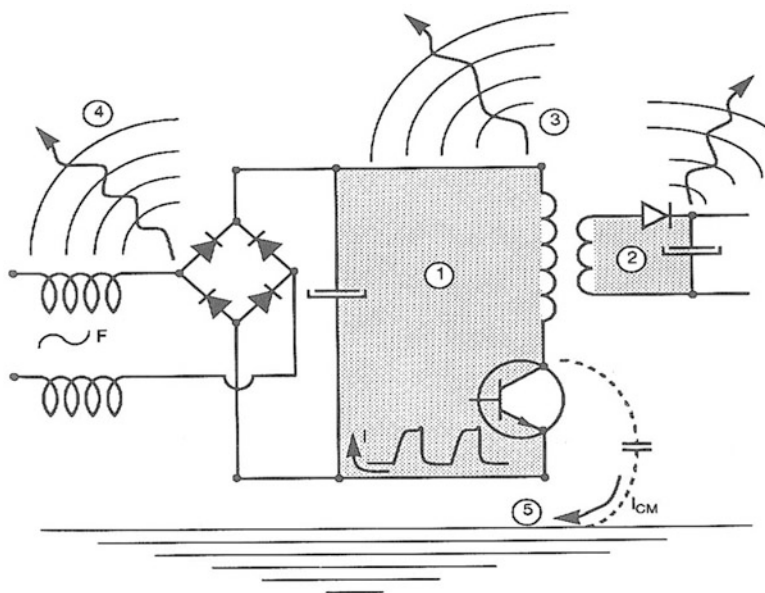
### 8.1 BASIC RADIATING SOURCES

Figure 8.1 shows the basic radiating sources or circuits in a simplified, one transistor SMPS:

1. The primary loop comprises the transformer (or the storage inductor in a non-isolated SMPS), the switching transistor(s), and the primary capacitor. This loop carries pulsed HF current and is generally the major radiator [1]. Its radiated field can be computed quite accurately from its current spectrum and the formulas in Chap. 2 for differential-mode loops.

2. The secondary loop comprises the transformer secondary, the rectifiers, and the filter capacitors (and, preferably, inductors). This loop carries the rectified (but not yet smoothed) current that is generally higher. Radiation can be calculated in the same manner as for the primary loop.
3. The transformer (or switched inductor) itself tends to radiate during the current peaks where it is brought to saturation. The leakage field can be significant in close proximity to the transformer.
4. The filter inductors, which ironically have the mission of suppressing conducted EMI, in turn tend to convert some of the reactive power into radiated EMI unless packaged carefully.

To a lesser extent, the CM loop due to the stray capacitance to ground of switching transistors, IGBTs, and diodes is also a candidate radiator. Such a loop can carry CM currents in large areas of the SMPS and host machine. However, this circuit is so strongly filtered to control conducted EMI up to 30 MHz (civilian) up to 100 MHz (some military or aerospace) that its radiated field generally is not a problem, with exceptions acknowledged.



**Fig. 8.1** Principal radiating elements in a switch-mode power supply (SMPS)

**Example 8.1** (*Radiation from an elementary one-transistor SMPS*) For the simplified 1 kW/40 kHz SMPS of Fig. 8.2, calculate the radiated  $H$  field at a 7 cm distance against MIL-STD-461 (E or F) RE101, most severe Navy limit.

**Solution** The peak current in the primary switching loop can be estimated per the following formula:

$$I_p = \frac{P_{\text{sec}} \left(\frac{T}{\tau}\right)}{V_{\text{prim}} K \sqrt{2}} \tag{8.1}$$

where  $T$  is the switching period,  $\tau$  the current pulse duration,  $P_{\text{sec}}$  the secondary power (watt)s,  $V_{\text{prim}}$  the primary rms voltage, and  $K$  the efficiency ratio (typ. 0.8).

Here, for  $V_{\text{prim}} = 115 \text{ V}$ ,  $T = 25 \text{ }\mu\text{s}$ , and  $\tau = 11.2 \text{ }\mu\text{s}$ ,  $I_p = 17 \text{ A}$ .

Then, calculate the characteristic frequencies of the Fourier envelope:

$$F_1 = 1/\pi\tau = 28.5 \text{ kHz}$$

$$F_2 = 1/\pi t_r = 2 \text{ MHz}$$

The fundamental's amplitude (40 kHz) will be

$$2A/\pi = 0.64 \times 17 \text{ A} \approx 11 \text{ A peak}$$

At 7 cm distance, the near-far transition frequency is

$$F_{\text{N-F}} = 48/0.07 = 685 \text{ MHz}$$

Therefore, the entire spectrum of interest is in the near field. From this point, the radiated  $H$  field is calculated by Equ. 2.19 or Fig. 2.7, for a 1 A-cm<sup>2</sup> magnetic moment. The following table shows the calculated values for the RE101 range of frequencies. The RE101 limit in dBpT has been converted in equivalent dBμA/m: 0 dBpT = -2 dBμA/m (in air).

Notice that this is a NB type of measurement, since the 10 kHz receiver bandwidth is smaller than the 40 kHz SMPS frequency. So, the actual harmonic readout will be in rms value, i.e.,  $\sqrt{2}$  (3 dB) less than the peak values.

For the MIL-STD-461-RE101 test, the distance being 7 cm. Equation 2.19 gives

$$\begin{aligned} H (\mu\text{A/m}) &= 7.96 \times I_{\text{amp}} \times A (\text{cm}^2)/D^3 = 23.10^3 \mu\text{A/m} \\ &= 88 \text{ dB}\mu\text{A/m for } 1 \text{ A cm}^2 \end{aligned}$$

where  $D$  is the distance in meters.

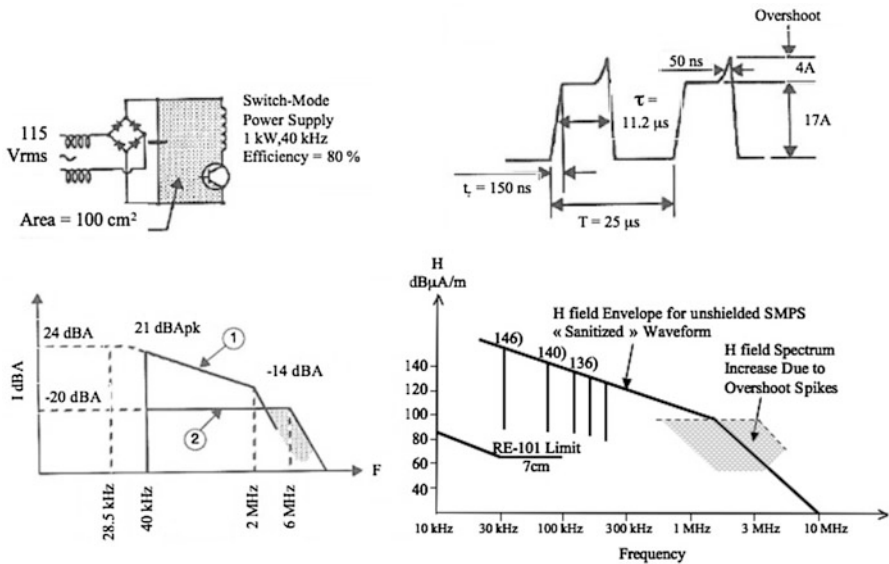
The calculated values are summarized in the following table:

Frequency	40 kHz	80 kHz
$I$ (dBA), peak	21	15
$I$ (dBA) rms	18	12
$H_0$ (dBμA/m) for 1 A-cm <sup>2</sup> at 7 cm distance	88	88
Area correction (dBcm <sup>2</sup> )	+40	+40
$H$ total (dBμA/m)	146	140
RE101-2 limit (dBμA/m)	74	74
$\Delta$ off-spec (dB)	72	66

RE101 compliance is required only in specific cases of low magnetic ambient requirements, e.g., antisubmarine warfare environments. This power supply (or the equipment using it) will be off-spec by 72 dB if no shielding or radiation control is effected. A loop size reduction >4,000 times would be needed to be within specs, with no margin. That is, the effective radiating area of the primary switching loop should be brought down to  $\ll 1 \text{ cm}^2$ , which is totally unrealistic. A serious modification of the circuit layout, repackaging the PC board, could bring the loop down to a few square centimeters, i.e., about 30 dB reduction. The remaining 42 dB + 6 dB margin has to be provided by a thick shield over the SMPS module, plus some additional shielding of the host machine.

Notice that the MIL-STD does not require  $H$  field measurement above 100 kHz, because the frequency domain of the submarine warfare detection equipment is using low frequencies. Yet, the  $H$  field radiation of this module could still be a threat to nearby (<10 cm) sensitive analog circuitry in the host equipment. This needs to be checked as an internal EMI (self-jamming) concern.

With power converters, if some sacrifice in efficiency is acceptable, pulse shaping and corner rounding can strongly limit the EMI spectrum above the megahertz region. A good example of this is evident in the resonant converter, where the basic switched waveform approaches a sine wave, with a much more limited spectrum (Fig. 8.3). Applications using a buck converter are also generating less magnetic field, because the primary current has an isosceles triangular shape, whose spectrum decreases like  $1/F^2$ .



**Fig. 8.2** Power supply radiation of Example 8.1 extended to few MHz. Current spectrum (1) corresponds to straight trapezoidal waveform, without overshoot. Superimposed, shaded spectrum (2) corresponds to the overshoot

### 8.2 EFFECT OF ACTUAL CURRENT WAVEFORMS

In general, SMPSs use square waves with steep slopes to minimize transistor power dissipation, thus increasing efficiency. This may not be an optimized choice overall: if maximum efficiency is the only driving parameter in the design, it will result in a proliferation of harmonics that require additional EMI-suppression components. It is not rare to see SMPSs whose active size is shrunk by “hot rod” design, but whose overall size and weight increase due to the filtering components (especially magnetics) that must be added to make up for the additional noise.

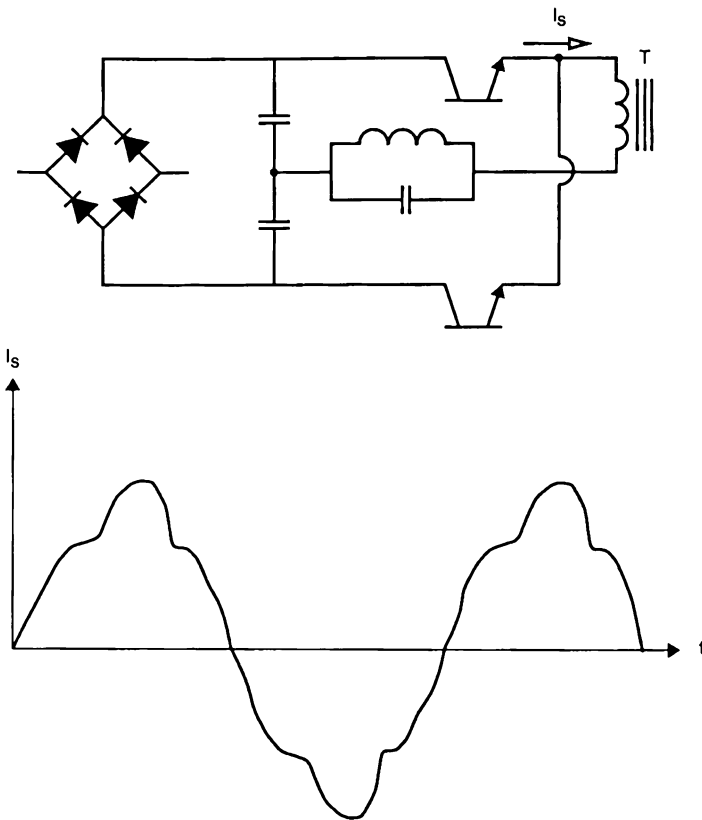


Fig. 8.3 One type of resonant-mode converter, causing less high-frequency harmonics

### 8.3 PACKAGING AND CIRCUIT LAYOUT

Up to about 100 W of secondary power, SMPSs are generally small enough to be packaged on a PC board or a small, compact module. Above this range, the SMPS is generally a hybrid of printed and hardwired assemblies, housed in an open or six-sided metal frame. The general principles discussed in Chap. 2 apply here. One of the driving ideas is to reduce, by all practical means, the magnetic moments (current  $\times$  area). The following methodology is recommended while still at the design phase:

1. On a schematic or wiring diagram, highlight in color all the connecting wires that carry changing (not necessarily alternating) currents (see Fig. 8.4).
2. When visualizing loop areas, consider them both in the horizontal and vertical planes (3D).
3. Identify the high  $dI/dt$  paths in order to minimize their inductance.
4. Watch for “hidden” radiating loops such as snubbers (small areas, but high peak currents and wide spectrum).
5. On all identified loops, keep the area to a minimum, and always try to “pair” a trace or wire with its return; this will decrease:
  - (a) Emissions from high  $dI/dt$  circuitry
  - (b) The susceptibility of sensing circuitry

The best way to accomplish this is by using strip-line style PCB wiring.

6. For connecting transformers and bulky components to the PCB, use flat conductors. The best approach is to have transformer leads (Fig. 8.5) coming out as flat straps for direct PCB mounting.
7. When two components or circuits are carrying equal currents at the same time, orient them such that their magnetic fields are in mutual opposition. This reduces (ideally, nullifies) their net magnetic moment (see Fig. 8.6).

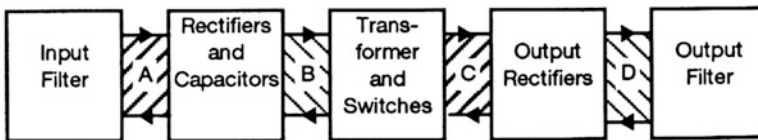


Fig. 8.4 Example of SMPS wiring diagram used to identify and control magnetic moments

### 8.3.1 Magnetic Leakages from Transformers and Chokes

Magnetic components are optimized for best efficiency and minimum heat, not for minimum EMI. The designer tries to achieve the best usage factor of his magnetic core by working close to (but not in) saturation. Leakage inductance is often a functional parameter and cannot be controlled just for the sake of EMC. However, trade-offs do exist:

- Try to use magnetic materials that show a hysteresis cycle with a soft knee, instead of a square cycle.
- For low-voltage, high-current windings, use flat conductors instead of round ones.
- Prefer closed or semi-closed shapes for magnetics (Fig. 8.7).
- If magnetic leakages are still too high, a transformer shield may be needed. A transformer whose full load leakage exceeds 1 mG at 10 cm distance (equivalent to 0.08 A/m or 98 dB $\mu$ A/m) on the first harmonics in the 20-50 kHz range has no chance to meet the  $H$  field limits of MIL-STD-461 or similar. A transformer whose leakage is simply ten times larger (10 mG at 50 kHz and 10 cm distance) will start to cause internal EMI problems if there is nearby sensitive analog wiring. At this frequency, such a field induces 0.3 mV/cm<sup>2</sup> of exposed circuitry.

The simplest kind of magnetic shield (the “poor man’s shield”) is the shading ring. This is a closed copper band, centered mid-height on the bobbin. The optimum width has been found empirically to be about half the bobbin height. Its operating principle is that the induced current in the short-circuit ring creates a canceling field, working against the leakage field. The copper must be thick enough and well soldered to withstand the Joule effect. In the predominant leakage directions, the field is reduced by a 2-3 factor. If more attenuation is needed, the ultimate solution is a closed box made of iron or ferrous material. It is important to note that the inductors used for conducted EMI suppression may require a similar treatment around their E-style magnetic cores. Otherwise, the designer will have traded his conducted noise for a radiated emission problem! (Fig. 8.8)

### 8.3.2 The Power Supply PC Board

On power supply boards, it is a good practice to leave copper on all unused areas instead of etching it away. These copper lands will be used for the positive and negative dc voltage on the rectified primary side and for the heavy current outputs. If a double-layer board can be afforded, the radiating loop sizes can be reduced by running opposite current traces on top of each other rather than side by side.



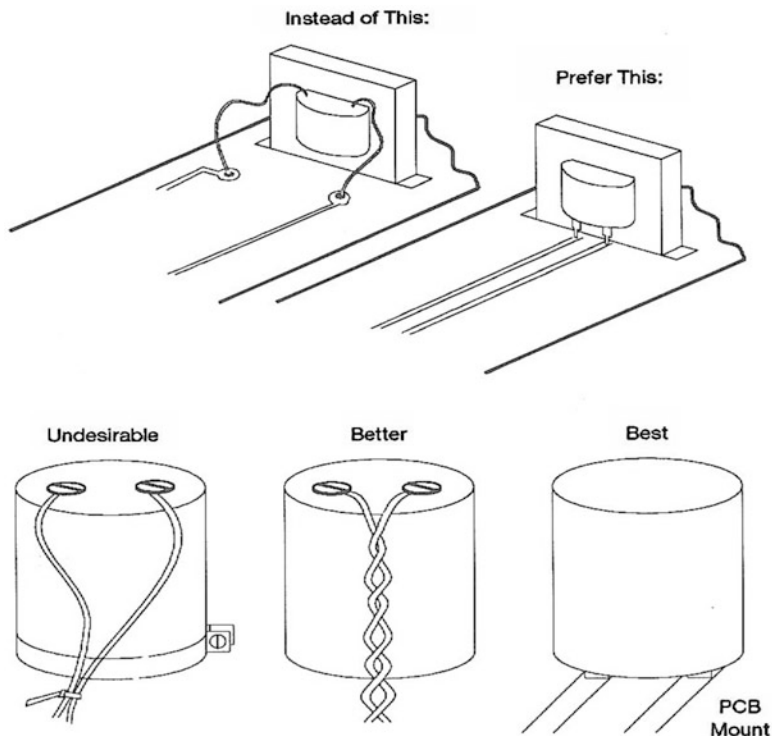


Fig. 8.5 Minimizing component leads loop areas

### 8.3.3 Secondary Loops

The secondary loop carries a pulsed current whose shape can be extremely distorted, especially with rugged designs like the one in Fig. 8.9. Such a current shape bears a high harmonic content. To reduce radiation from this loop, one must control its area, as mentioned previously. In addition, the current waveform should be spread and smoothed. Full-wave rectification already reduces the problem by decreasing  $I_{\text{peak}}$  and increasing  $\tau/T$ . But more is gained by adding an inductor between the rectifier and the capacitor. This causes the current spectrum to roll off at a  $1/F^2$  rate (40 dB per decade), instead of  $1/F$ .

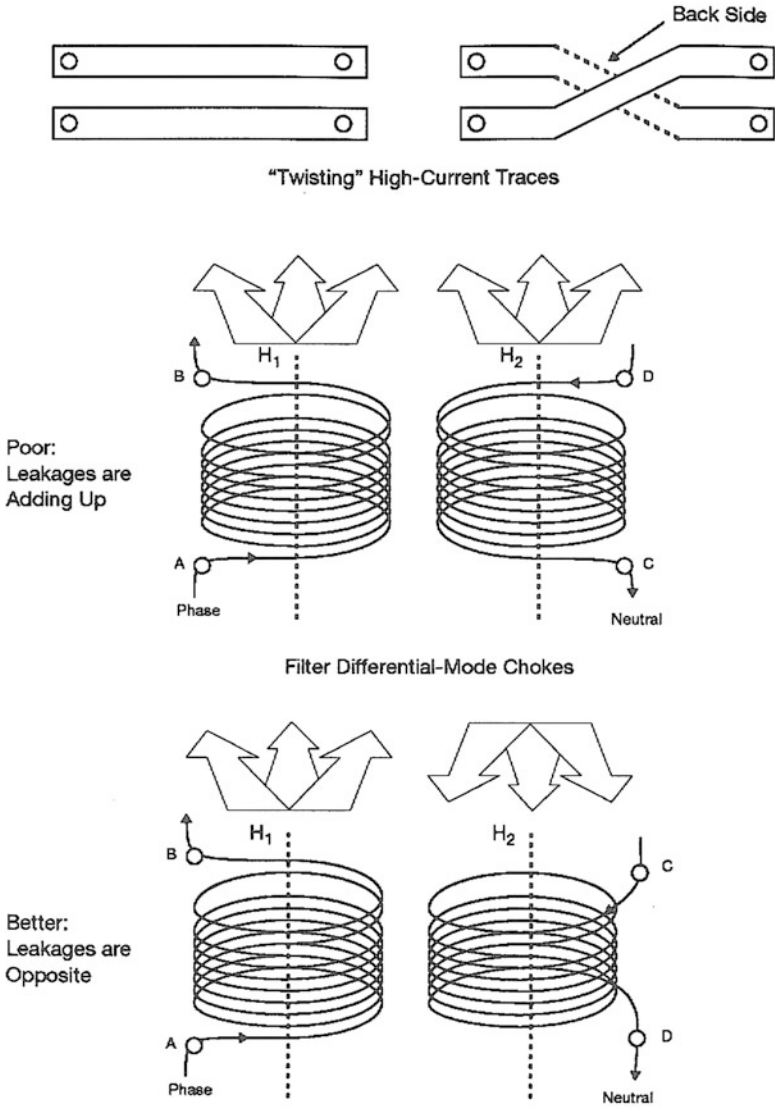
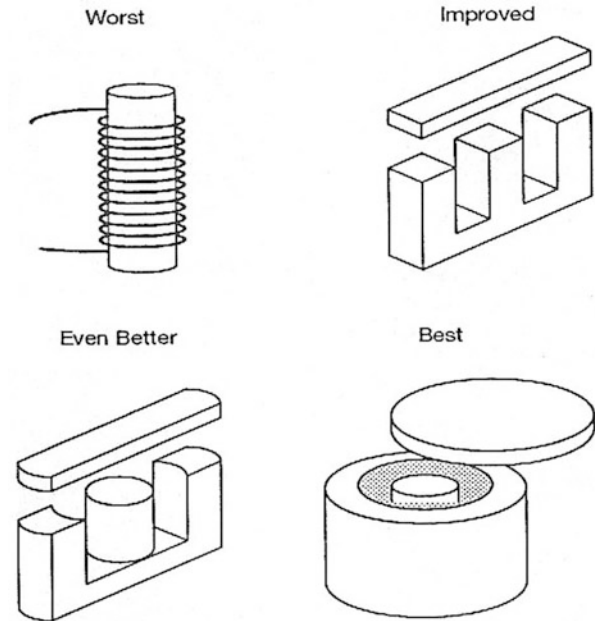
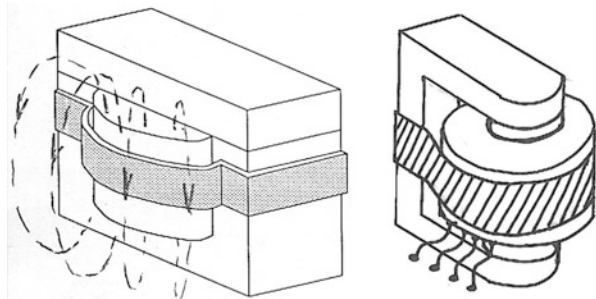


Fig. 8.6 Neutralizing identical magnetic moments. By 180° reversing the “neutral” filter choke, its leakage field now opposes that of the “phase” choke

**Fig. 8.7** Reducing transformer leakage field



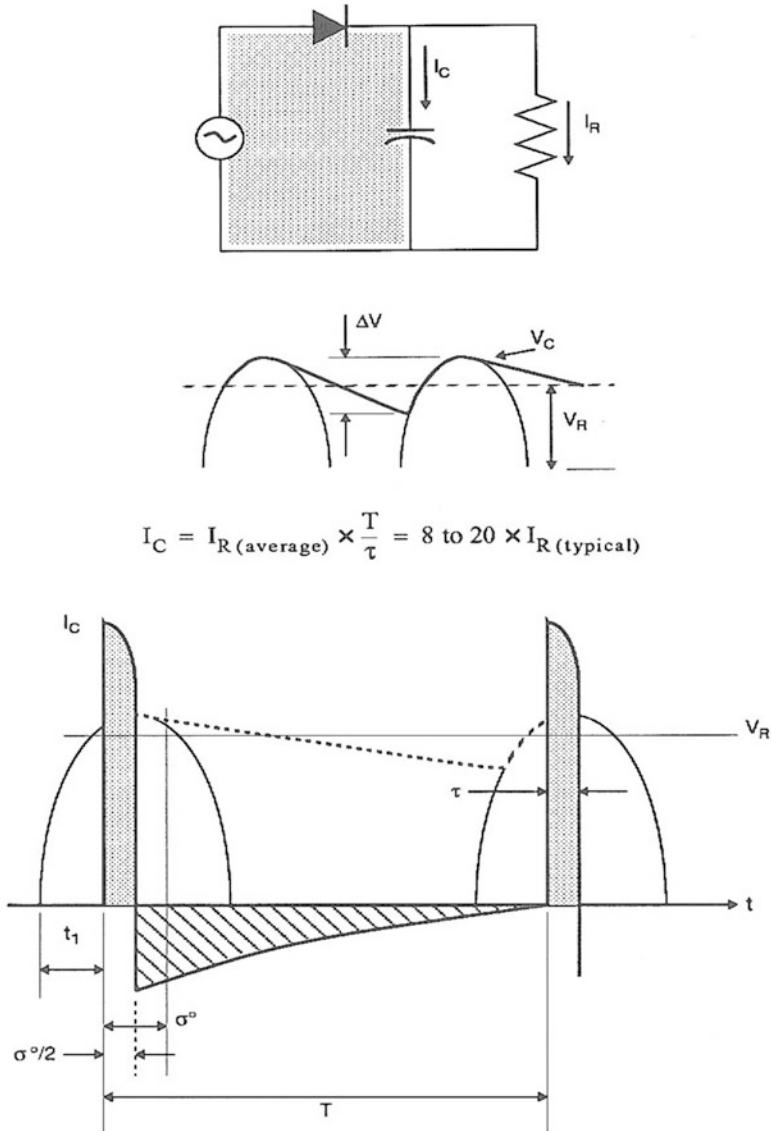
**Fig. 8.8** Use of shading ring for reducing transformer leakage field



### 8.3.4 Electromechanical Packaging

All the guidelines prescribed so far need to be translated into a compact electro-mechanical design that minimizes radiating loop surfaces in three dimensions. Figure 8.10a, shows a mediocre, hardwired SMPS layout:

- The unfiltered AC input radiates in the entire host machine before being filtered by G, causing internal and external EMI.
- The primary diode bridge (labeled A) and electrolytic capacitor (labeled B) form a radiating loop carrying 50/60 or 400 Hz, pulsed, nonsinusoidal current.
- Capacitor B, transformer T, and switching transistor S form a large and mostly detrimental radiating loop.
- Output filter Section F will pick up switching harmonics, by near-field radiation.

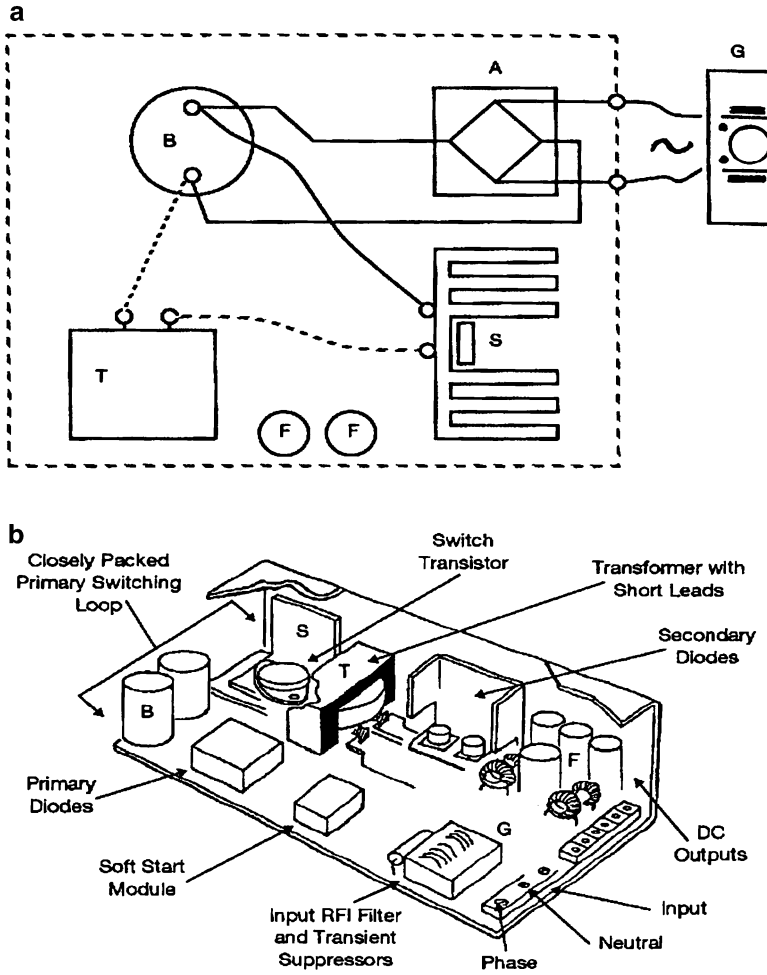


**Fig. 8.9** Secondary loop current into filtering capacitor

In comparison, Fig. 8.10b, shows a better layout:

- The AC input is cleaned up by filter G at the SMPS barrier, with no input-to-output recoupling.
- B, T, and S are now closely packed, rendering the HF loop minimal. DC output diodes and ripple filter F are distant from the primary switching loop. A large copper plane under B, T, and S is used for the bulk DC (rectified ac) return.

It also helps decoupling the heat sink (collector) noise from the emitter common before it goes to the chassis. Wider traces are used for transformer output.



**Fig. 8.10** Poor and good SMPS layouts. (a) Example of a poor layout, (b) example of a good layout

Whenever possible, there is an advantage to keeping input and output terminals on the same face. Provided that the primary section is correctly decoupled internally from the output, all terminals on the same side will reduce the HF current flow across the entire power supply chassis, where it would have more opportunities to radiate through slots and discontinuities. (This does not apply to integrally shielded SMPS.)

## 8.4 SHIELDING THE POWER SUPPLY MODULE

A detailed discussion of shielding materials and practices will be found in Chap. 10. However, we will summarize here some shielding guidelines that are unique to power supplies.

Below about 100 W and 100 kHz switch frequency, an SMPS generally does not need to be enclosed in a shield, provided that the packaging precautions described earlier have been incorporated. Unless stringent intra-unit EMC requirements exist (e.g., the proximity of analog circuits, magnetic heads amplifiers, etc.), a PCB with open-frame power supply packaging is usually sufficient. Notice, though, that even an open-frame design can be a fairly useful Faraday shield, preventing CM currents from an “HF-hot” heat sink from circulating into the entire equipment chassis (see Fig. 8.11). In Fig. 8.11a, the heat sink is a voltage-driven antenna with respect to ground. Notice that “earthing” the heat sink would decrease the  $E$  field but increase the CM current leakage back to the power mains, aggravating conducted EMI. In Fig. 8.11b, the  $I_{CM}$  path is contained within the frame, even if the box is not 100% closed. With a continuous metal sheet, there is virtually no voltage drop along the B-to-G path, and the frame does not reradiate.

At higher power and/or frequencies, the SMPS radiation becomes a greater concern, and real shielding has to be considered. On the first harmonics of the switching frequency, fields with a predominantly magnetic term (i.e., low impedance fields, at a distance  $< \lambda/2\pi$  from the source) are very difficult to shield. Against very low frequency ( $< 10$  kHz) magnetic fields, it is necessary to use thick iron (at least 1 mm thick) or permeable materials like Co-NETIC<sup>®</sup>, having a  $\mu_r$  larger than 1,000. Above a few hundred kilohertz, any metal like copper, aluminum, or iron, with at least 0.8 mm (30 mil) thickness is intrinsically an excellent shield. At 100 kHz, a 0.8 mm-thick aluminum plate provides 55 dB of attenuation against an  $H$  field source at 5 cm.

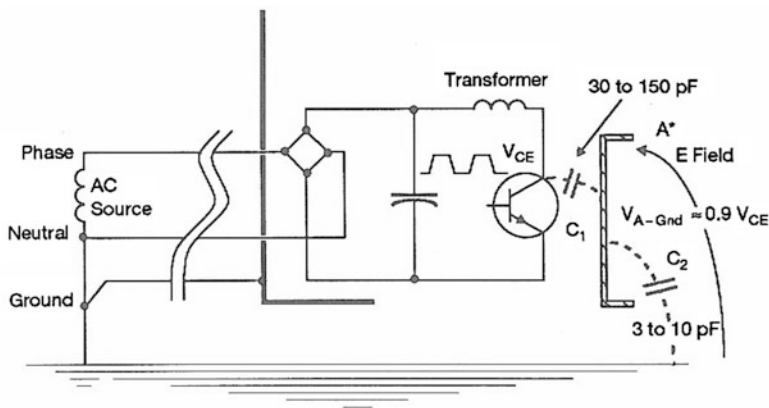
In the 10–100 kHz region, a good trade-off for performance and weight consists of:

- A layer of good conductive material (copper, zinc, or tin) facing toward the  $H$  field source, providing reflection loss
- A barrier of ferrous material providing good absorption loss

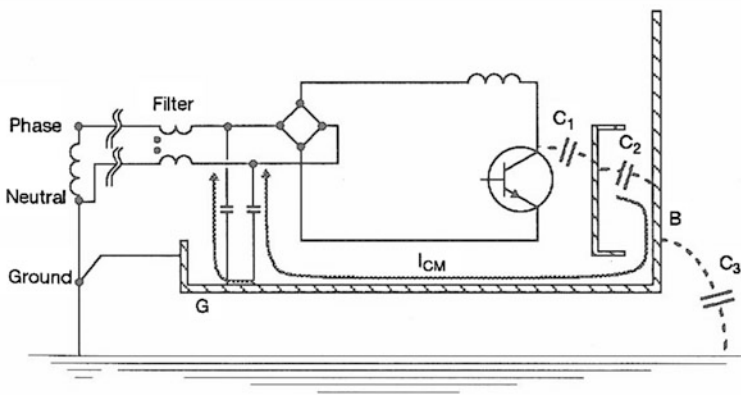
This combination is realized by copper-clad, tinned, or zinc-coated iron.

Next in importance to the choice of the shielding material is the realization of the shielded box itself. If the SMPS stands entirely on a PCB, a ground plane on the external face of the board can act as one face of the shield, and the metal housing needs to be only a five-sided one. Avoid large perforations, especially near the high  $dV/dt$  or  $dI/dt$  sources. Eliminate long slots and seams. Cooling apertures should be arrays of round holes instead of long slots. Do not mount magnetic components near openings. Ideally, to preserve the normal field attenuation through an opening, the radiating source should be at a distance,  $D$ , greater than three times the largest opening dimension,  $\ell$ . To assemble shield edges, prefer a continuous

weld to spot welding. For screw-mounted covers, keep the screw spacing small, consider the space between screws as a leaky slot, and respect the  $D/\ell > 3$  criteria, as explained above.



**a. Open-Frame Power Supply**  
 \*Electrically "hot" heat sink becomes a voltage-driven antenna.



**b. Partially or Fully-closed power supply**

Fig. 8.11 Properly designed open-frame power supply can act as a Faraday shield

## 8.5 EFFECT OF THE POWER SUPPLY FILTER ON RADIATED EMI

Whether the power supply filter is specific to a power module only (i.e., inside the machine) or acts also as a mains filter for the whole unit, there is a definite interaction between the filter performance and the radiating profile of the equipment. There is a tendency to envision EMI as a two-sided coin, conducted and

radiated, presuming that the two can be handled separately. Therefore, a power supply filter that has successfully helped in not exceeding conducted limits is labeled “good” and exempted from any further suspicion. In fact, mounting deficiencies or disregard for parasitic effects in PCB layout (Fig. 8.12) may cause the filter attenuation to drop in the range above 20–30 MHz [3, 4]. Beyond these frequencies, conducted specifications generally stop. Thus, filter leakages could go undetected by the conducted test, yet still cause the equipment to radiate strongly by its power cord. One major, incidental radiating contributor in SMPS filter is the filter inductor (DM and CM), because of its unavoidable magnetic leakage. In that respect, the technology used for planar inductors [4], made of printed circuits concentric windings, can be an interesting alternative: because of their good efficiency and interleaving patterns, they can provide more  $\mu$ Henry per turn and therefore will radiate less magnetic field at the SMPS harmonic frequencies.

To avoid this, filter performance and mounting techniques should be scrutinized across the entire frequency range of clock harmonics (not just SMPS harmonics), typically up to 10–30 times the highest clock rate or at least 100 MHz, whichever comes first (see Fig. 8.13).

Quite typically, an unfiltered SMPS generates conducted EMI 40–60 dB above FCC/CISPR or MIL-STD limits. To attenuate<sup>1</sup> this noise before it radiates into the entire equipment and beyond, it is advisable to mount the filter components as closely as possible to the power supply input terminals and separate noise-conducting leads from regulated DC and sense leads. The best way to achieve this is to use filters (either purchased or homemade) that are packaged in a feed-through style. In this manner, any undesired recoupling of output and input conductors is avoided. The following example will show how compliance with conducted limits does not necessarily guarantee radiation compliance.

**Example 8.2** A tabletop commercial equipment, with plastic housing, satisfies the conducted FCC Class A limit at around 25–30 MHz with a 4 dB margin. Knowing that the conducted narrowband spectrum stays at approximately the same amplitude from 25 to 35 MHz, does the equipment meet the Class A radiated limit with its unshielded 1.50 m power cord at about 0.80 m above ground? Repeat this exercise for MIL-STD-461-CE103 vs. RE102 (cable at 5 cm above ground). The test data from these examples are illustrated in Fig. 8.14.

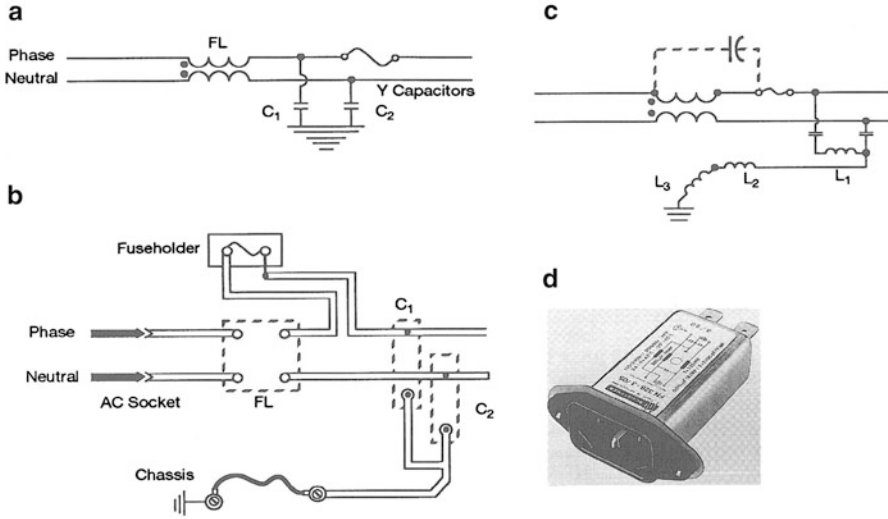
#### a. FCC Class A Solution

For the FCC tabletop test setup, we have an undefinable loop, so we will use the worst-case assumption of an open-ended cable and apply Equ. 2.27. At 35 MHz, the conditions are far field (test distance = 10 m) with an electrically short cable

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<sup>1</sup> Although commonly used, including by this author, the terms “attenuate” and “suppress noise” are generally misnomers. Except for the small amount of energy that is dissipated into heat, the filter in fact reroutes the EMI currents away from the equipment and power mains loops and forces them to remain confined within the power supply compartment.





**Fig. 8.12** Filter mounting problems. The feed-through mounting (bottom) avoids recoupling. Photo courtesy of Schaffner, Inc. (a) How schematic showed it (b) How manufacturing made it (c) How it looks electrically (d) a correctly made finished product

( $\ell < \lambda/4$ ). We first determine the CM current from the  $50 \Omega$  LISN (artificial mains) impedance:

$$I \text{ (dB}\mu\text{A)} = (V_{\text{limit-margin}})/Z_{\text{LISN}} = (70 \text{ dB}\mu\text{V} - 4 \text{ dB}) - 34 \text{ dB}\Omega$$

$$= 32 \text{ dB}\mu\text{A} \text{ or } 40 \mu\text{A}$$

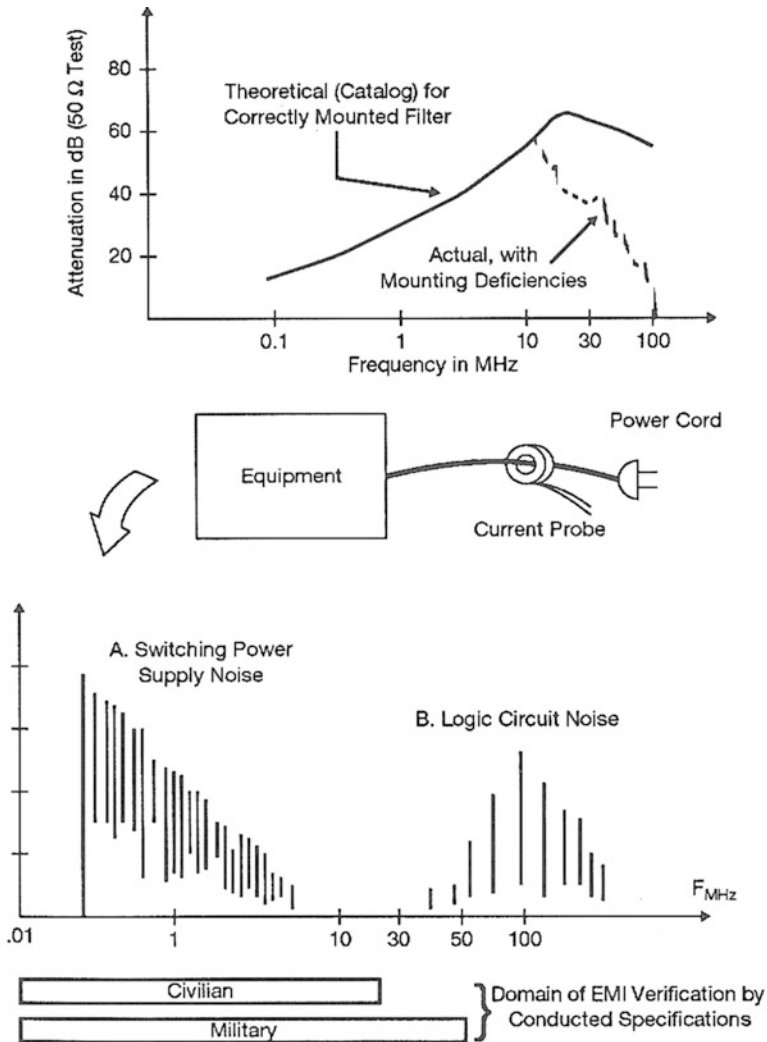
for each LISN, that is,  $80 \mu\text{A}$  for the two wires (phase + N) together

$$E \text{ (}\mu\text{V/m)} = \frac{0.63 \times 80 \mu\text{A} \times 1.50 \times 35 \text{ MHz}}{10 \text{ m}} = 260 \mu\text{V/m} \text{ or } 48 \text{ dB}\mu\text{V/m}$$

Even without accounting for the ground reflection in the FCC test method, the radiated Class A limit of  $40 \text{ dB}\mu\text{V/m}$  at  $10 \text{ m}$  is exceeded by  $8 \text{ dB}$ . In other words, compliance with conducted emission around  $30 \text{ MHz}$  may give a false feeling of security for radiated emission at same frequency.

**b. MIL-STD Solution**

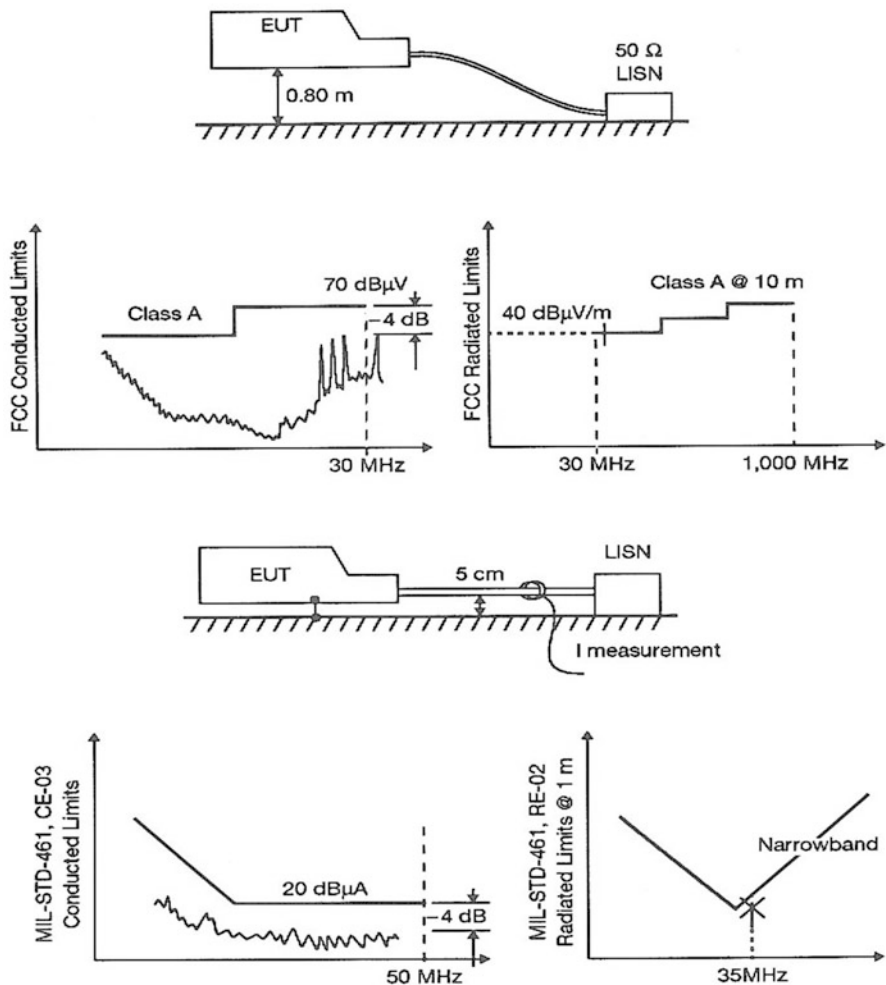
For MIL-STD-461, we will first use the former Mil-461-C, CE03 criteria, because its  $20 \text{ dB}\mu\text{A}$  limit extends up to  $50 \text{ MHz}$ . If the product is within specifications by a margin of  $4 \text{ dB}$ , this means a  $(20 - 4) = 16 \text{ dB}\mu\text{A}$  or  $6 \mu\text{A}$  CM current exists between  $25$  and  $35 \text{ MHz}$  on each power lead. However, at a  $1 \text{ m}$  test distance, we are in the near field ( $D < 48/F$ ). Also, no more than  $\ell = D$  can be entered for effective radiating cable length (see Chap. 2, Sect. 2.5.3). The radiating loop dimensions are  $\ell = 1 \text{ m}$ ,  $h = 0.05 \text{ m}$ . In such conditions, the  $E$  field is calculated by



**Fig. 8.13** Power line filter performances vs. EMI spectrum on power cord. If the filter does not have good attenuation above 30–50 MHz, the A portion of the spectrum is correctly suppressed for conducted spec. compliance, but the B portion contributes to radiated EMI

$$\begin{aligned}
 E(\mu\text{V/m}) &= \frac{0.63 \times I(\mu\text{A}) \times A(\text{m}^2) \cdot F(\text{MHz})}{D^2} \\
 &= \frac{0.63(2 \times 6\mu\text{A}) \times (1 \times 0.05) \times 35(\text{MHz})}{1^2} = 13 \mu\text{V/m} \text{ or } 22 \text{ dB}\mu\text{V/m}
 \end{aligned}$$

The MIL-461 RE02 limit is 22 dB $\mu$ V/m. Thus, we are just at limit, without any margin. Incidentally, we retrieve our criteria for CM currents as set forth in Chap. 2, Sect. 2.5.2, Example 2.7.



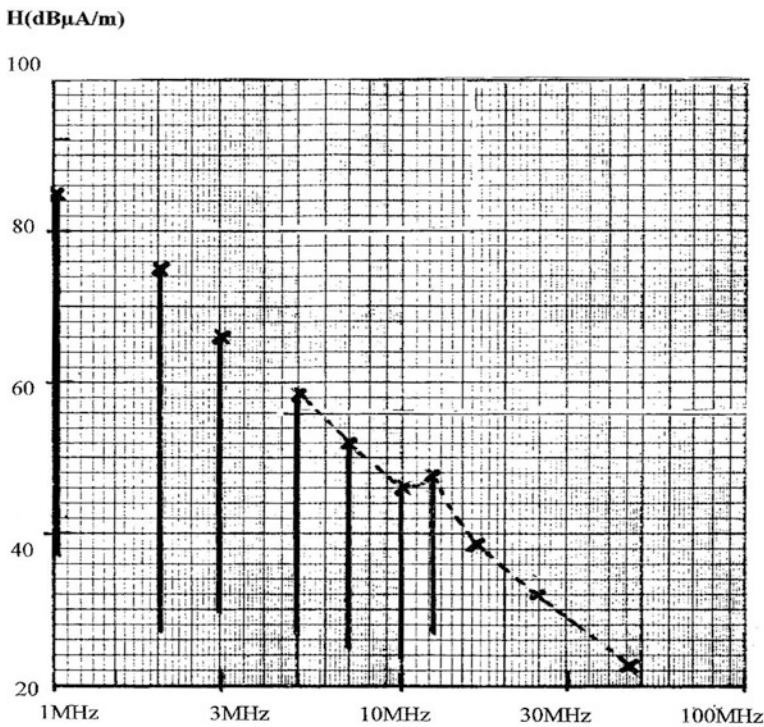
**Fig. 8.14** Test data of Example 8.2, conducted vs. radiated compliance (Military part refers to MIL-461-C limits)

If, instead we use the Mil-461 E or F version, the conducted CE102 limit, expressed in voltage is  $60 \text{ dB}\mu\text{V}$ , that can we translate, like we did above for FCC-Class A, into a corresponding current of  $12.5 \mu\text{A}$  on each wire, that is  $25 \mu\text{A}$  of CM current for the Ph. + Neutral wires. Using the same equation as above, the corresponding E field at 1 m is  $27.5 \mu\text{V/m}$ , or  $29 \text{ dB}\mu\text{V/m}$ . Mil-461 E or F RE102 limit at 35 MHz is  $24 \text{ dB}\mu\text{V/m}$ . Therefore the product exceeds the limit by 5 dB.

## 8.6 EMI RADIATION FROM SMALL DC-DC MODULES

An increasing number of applications are using small, just few watt DC-DC converters scattered on the PCB for delivering the various low voltages (1, 1.8, 3.3 V, etc.) required by dense, fast ICs. Although small in size, typically few cm<sup>2</sup>, they operate at frequencies in the few hundred kHz to few MHz range. Therefore, although their magnetic radiation is rather modest, the relatively high switching frequency can turn them into potential offenders to nearby sensitive circuits sharing the same PCB. One must keep in mind that a 0.1 A/m *H* field at 1 MHz is just as threatening as a 1 A/m field at 100 kHz: they both can induce 40 μV/cm<sup>2</sup> of printed circuit capture area.

Figure 8.15 shows the *H* field at 5 cm above a 3 W DC-DC module, operating at 1 MHz. The module has a built-in shield and an internal filter on its 15 V input. Assuming at least 20 dB of shielding effectiveness, the unshielded version is deemed to radiate ≈100 to 110 dBμA/m at 1 MHz.



**Fig. 8.15** *H* field in the *Z*-axis at 5 cm above a 3.3 V/1 A DC-DC module LTM 8031. The package is a 15 × 9 × 2.8 mm, leadless low profile (measured by the author)

## REFERENCES

1. F. Costa, Radiated emission from Buck chopper, in *IEEE/EMC Transactions*, May 2008
2. J. Fluke, *Controlling Conducted Emissions by Design* (Van Nostrand, New York, 1991)
3. M. Nave, *Power line filter design for SMPS*, Van Nostrand, 1991, 2nd edn. (Springer, New York, 2010)
4. T. Neugebauer, D. Perreault, Filters with inductance cancellation using printed transformers, in *IEEE/EMC Transactions*, Oct 2013

# Chapter 9

## Reducing Radiated EMI Via Internal Cabling and Packaging

Once the major building blocks have been designed for minimum EMI radiation, it must be ensured that the internal equipment harnessings between subassemblies do not radiate excessive noise. Such wirings will be found to radiate as a function of the intentional signals they carry, plus the spurious signals gathered and insufficiently filtered at each subassembly's interface. This chapter is addressing only the internal aspect of precautions for reducing EMI radiation of the equipment alone. The very important aspect of I/O ports treatment and associated external cables EMI control will be fully covered in Chap. 11.

### 9.1 CARD-TO-CARD AND BACKPLANE INTERCONNECTS

PCB-to-PCB connections inside or between modules are usually made with ribbon cables or flexprint. To accommodate the largest possible number of conductors, designers tend to use only a single return wire and assign all other positions to signal wires. This is a poor practice, because the signal wires at the far edge from the return wire make a wide DM loop that:

- Radiates efficiently
- Exhibits strong crosstalk with the next conductors (see Fig. 9.1)
- Is susceptible to ambient interference

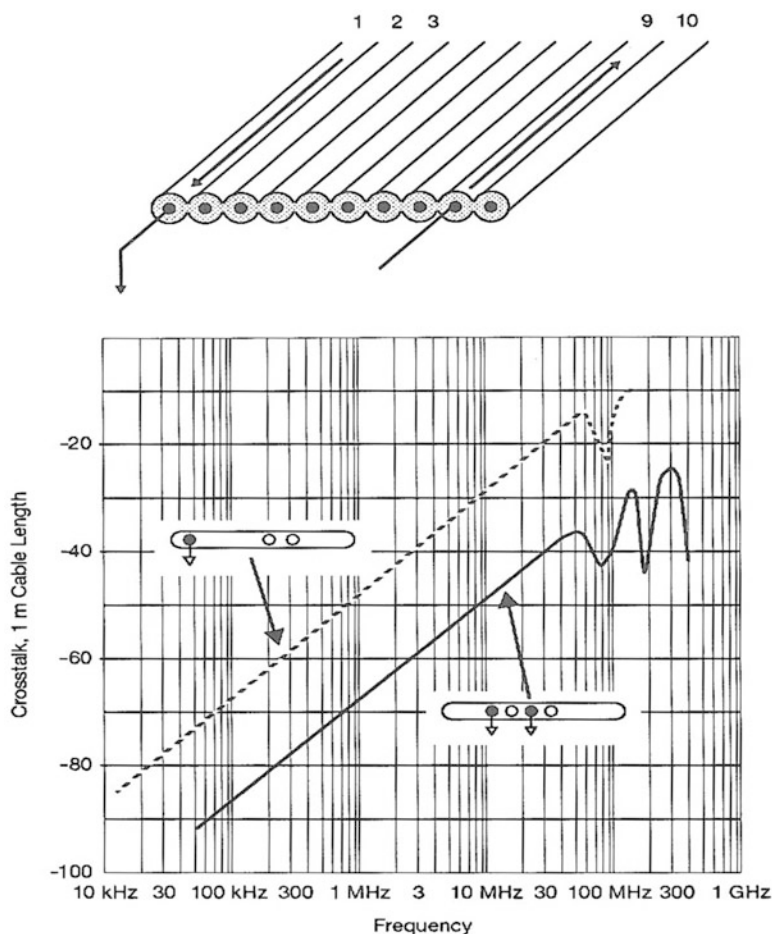
For a typical ribbon cable 1 or 2 in. in width, such a loop is an efficient radiator (see Chap. 2).

The alternating 0 V-signal-0 V arrangement should be used systematically for rise times shorter than about 12 ns and clock frequencies or bit rates above 1 or 2 MHz. (This calculation is based on satisfying FCC/CISPR Class B limits with a

1.50 m flat cable and the worst possible wire spacing of 5 cm.) Therefore, all signals with faster rates and rise times should use either:

- One ground for each signal wire, or at least one ground wire running along each high-frequency signal, at 1.27 or 2.54 mm spacing (see criterion above)
- A ribbon cable with ground plane
- A flexprint with ground plane

Some vendors offer twisted ribbon cables. Twisted ribbons are efficient in reducing crosstalk and near-field radiated problems (emissions or susceptibility), yet their benefit with regard to radiated EMI is rather limited, compared to the major improvement achieved by simply reducing wire spacing down to 1.2 or 2.5 mm. This is true for two reasons:



**Fig. 9.1** Radiation and crosstalk with flat cables. All wires terminated in  $100\ \Omega$  to the single ground wire. Wire #9 or #10 forms a large radiating loop with the 0 V return. The worst capacitive crosstalk (*top curve*) is for two wires, 2.5 mm apart with their 0 V return at a 25 mm distance

- The reduction in DM radiation by simply reducing wire spacing is so large that CM radiation generally takes over, masking any twisting improvement (twisting has no effect on CM current radiation).
- The vendor often leaves an approximately 4-10 cm-long untwisted segment every half meter or so, to allow for easy mounting of self-stripping connectors. This seriously limits the twisting-derived attenuation.

Another risk of crosstalk with flat cables occurs with stacking. In this case, high-speed flat cables that do not exit the equipment can very efficiently contaminate I/O cables. Alternate grounds won't help very much; a better solution is to interpose a shield, use shielded flat cables, or insert a spacer of a few millimeter thickness to increase separation.

Flexprint interconnects with copper planes on two sides give an even better shielding, especially if the two planes are connected regularly every few centimeters through holes. This approaches the performance of conventional shielded cables.

Occasionally, the designer may use short jumper segments of flat cables to connect one card that lies above a larger one (see “terrace” arrangement in Fig. 9.2, top) or two daughter cards on their front ends, in addition to their normal backplane interconnection. In this case, a potential radiating loop is formed; since the ground references of the two boards are now connected by two possible paths, each signal current going from one card to the other can return not only by the expected path, but also by the alternate one. In addition, ground noise current can flow between the two top connectors. Radiation from such loops is difficult to combat, so they should be avoided whenever possible (otherwise, the flat jumper cable should have a ground plane). In all cases, all the unused wires should be connected to the ground at both ends. A floating wire just invites more radiation and crosstalk. In extreme cases of internal flat cable radiation, ferrite suppressors can be installed over the cables. Such ferrites work by creating a high mutual inductance and resistive losses. Above a few megahertz, they increase the CM loop impedance, artificially balancing the pairs in the flat cable (more about ferrites is found in Chap. 11, Sect. 11.4, I/O filtering section).

## 9.2 INTERNAL WIRING RULES BETWEEN SUBUNITS

### 9.2.1 General Rules for Ordinary, Unshielded Cables

1. Try to route internal cables close to internal frame members, metal compartments, and conductive equipment covers, not across large slots, louvers, and seams.
2. Avoid crosstalk between high-frequency carriers that may be filtered or shielded when they exit the equipment and other (harmless) wiring that will not. Keep a minimum separation “s” (center to center) between the culprit and victim conductors, function of their height “h” above the closest chassis. An  $s/h$  ratio  $>5$  will guarantee a maximum crosstalk  $<3\%$  in the worst possible scenario (high-impedance victim circuits, parallel length  $>\lambda/4$  of the culprit signal, etc.).



For instance, if culprit and victim bundles are kept at no more than 0.5 cm above the chassis, a separation  $\geq 2.5$  cm will guarantee less than  $-30$  dB of crosstalk.

3. Avoid creating large loops between hot wires carrying high  $dV/dt$  (more than a few volts/nanosecond) or high  $dI/dt$  (a few hundreds of milliamps/nanosecond) and their normal, or unintentional, return conductors. When attempting to track down and reduce them, always picture these loops in three dimensions to figure out the loop contour.

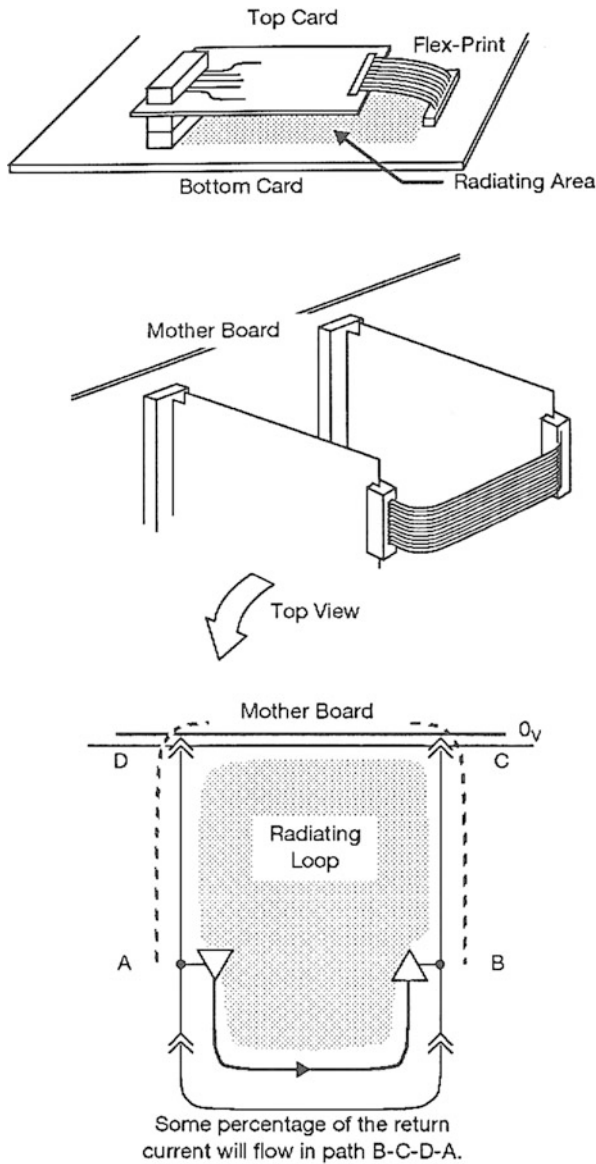


Fig. 9.2 Some hidden radiating loops with card-to-card wired interconnections

## 9.2.2 Coaxial Cables

A coaxial cable is simply a two-conductor line in which one conductor happens to be concentric to the other. Therefore, there is no question that the shields be connected at both ends to the ground reference. As of the year 2010, more than 80 years after the invention of coaxial cable, the author in his role of EMC consultant still (not so rarely) encounters coaxial shields that have been kept floated at one end “to avoid making ground loops.” Missing the shield connection, the HF current from the center conductor will have to worm its way back to the source, generally using every possible return route through chassis and bonding wires. In this process, the radiation is multiplied by several orders of magnitude, and the shield becomes useless.

Interfacing coaxial cables with PCBs should always be accomplished via a coaxial connector before the signal can be transferred into the strip or microstrip configurations of the PCB. Multicontact edge connectors used for PCB and motherboards are available with all or some of their contacts being the coaxial type. If space or cost dictates, cheaper substitutes like coaxial ferrules (see Fig. 9.3) can be used, but radiation and crosstalk will be generated in these areas. A rather regrettable practice is shown in Fig. 9.3c, where a large portion of each shield is stripped away, then daisy chained to a single ground pin. As demonstrated in the following example, this type of termination can be quite detrimental.

**Example 9.1** A coaxial cable carrying a video signal terminates on a PCB as shown in Fig. 9.3c. The stripped center wire and the shield-to-ground connection form a  $4 \times 2.5$  cm loop. The video signal has the following characteristics:

- Time-domain peak voltage: 10 V
- Fundamental: 6 V at 25 MHz
- Harmonic #3: 2 V at 75 MHz
- Load resistance: 50  $\Omega$

What is the radiated field at 3 m distance at 25 and 75 MHz?

From Equ. (2.22) or Fig. 2.6, for far-field conditions:

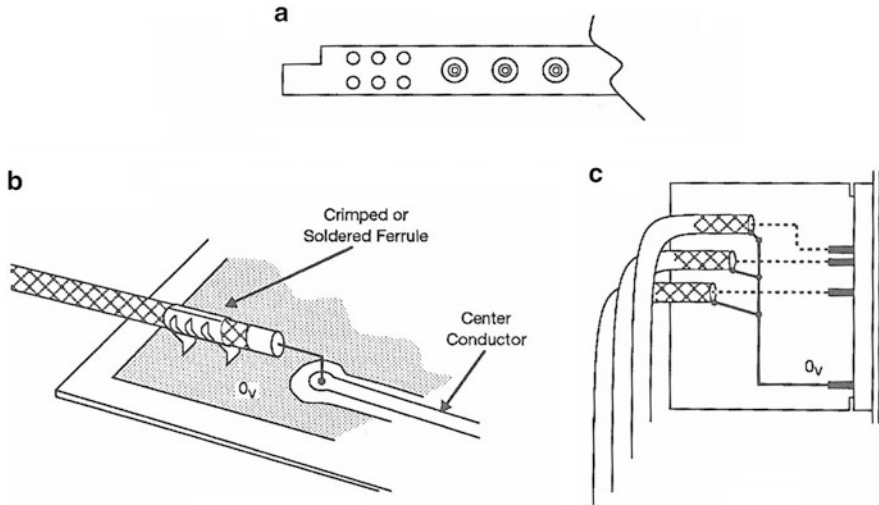
$$\begin{aligned} E(\mu\text{V}/\text{m}) &= 1.3(\text{V} \cdot 10 \text{ cm}^2 \cdot F^2)/(3 \text{ m} \cdot 50 \Omega) \\ &= 300 \mu\text{V}/\text{m} \quad \text{or} \quad 50 \text{ dB}\mu\text{V}/\text{m} \quad \text{at} \quad 25 \text{ MHz} \\ &= 1,000 \mu\text{V}/\text{m} \quad \text{or} \quad 60 \text{ dB}\mu\text{V}/\text{m} \quad \text{at} \quad 75 \text{ MHz} \end{aligned}$$

The second value exceeds FCC/CISPR Class B requirement by about 20 dB. (There is no requirement at 25 MHz for commercial equipment.) The MIL-STD-461-RE102 limit, if we translate it at 3 m, is exceeded by at least 40 dB (assuming that the circuitry inside the tested box is no less than 25 cm above the test ground plane). To make this loop a negligible contributor to the radiated field (taking a 6 dB margin), the loop surface must be brought down to

$<0.5 \text{ cm}^2$  for FCC Class B

$<0.05 \text{ cm}^2$  for MIL-STD-461-RE102

This virtually eliminates any such mounting.



**Fig. 9.3** Connecting coaxial cables to PC boards. (a) Best: Combination edge connector, with coaxial and regular contacts, (b) acceptable, (c) poor

### 9.2.3 Internal Shielded Cables, Other Than Coaxial

For internal shielded pairs or shielded harnesses, the shield is not an active return so there is no functional reason to connect it to the signal ground ( $0\text{ V}$ ). Because its role is to prevent some cables from radiating or picking up internal radiation, the best connection for such protective shields is at the chassis, at both ends. Each end of a cable shield should be at the same potential as the chassis or box that it enters or exits.

The following rules apply to internal cable shields other than coax:

1. If the chassis (or a sheet metal component box, conductive plastic enclosure, etc., i.e., bonded to the chassis) is available near the cable ends, connect both ends of the shield to this part, via the metallic connector housing/receptacle, or use a short, wide strap. (Do not use “pigtail” wire.)
2. If rule 1 cannot be met, stay away from nonsense: do not run long wire leads to a remote chassis ground. A copper land connected to the chassis should have been provided on the motherboard edge (see Chap. 7), which is an acceptable place for a short, low-inductance shield connection.
3. If neither rule 1 nor rule 2 can be met, connect the shield ends to the ground reference plane or copper land of the corresponding PCBs or subassemblies. Do not use a thin trace for this. A shield is basically a “noise collector.” Driving current from a noise collector into a copper plane is of less consequence, because impedance of a ground plane makes only tens of milliohms up to 300 MHz. Driving the same current into a ground trace can contaminate a signal reference.

There are few exceptions to rule 3 with regard to grounding shields at both ends “for lack of any better” method:

- If the cable carries low-level analog signals, tying the two ends of the shield to different ground references may inject noise into the enclosed wires, destroying a high CM rejection obtained via coupling transformers, optoisolators, or differential amplifiers. In this case, the input of the analog amplifier should be decoupled against HF. The cable shield will be grounded (a) on the amplifier side only, if the sensor can be floated or (b) on sensor side only, if the sensor, magnetic head, or other reference is already grounded. If the amplifier has a floated “guard” shield, the cable screen will be connected to it as well.
- If the cable carries mixed analog/digital signals, with an analog ground reference on one end and a digital ground on the other, it is presumed that the designer has provided some kind of interface isolation device or translator. Tying the two ground references together via the shield may create an objectionable loop. In this case, a shield aimed at protecting sensitive wire from radiation should be tied to the analog ground only. Conversely, a shield meant to prevent digital wires from inducing capacitive crosstalk into other wiring should be grounded to its digital ground only.

Notice that the two above exceptions are aimed more at internal EMC than to outside radiation concerns. Shields connected in such ways are primarily electrostatic shields, with no effect in reducing radiated emissions above 30 MHz, let alone CM loop reduction. However, this book is trying to provide emission reduction guidelines that are not counterproductive to noise immunity considerations.

### 9.3 SOME HIDDEN RADIATING ANTENNAS

Some equipments may include internal radiating loops that are not easy for a nonspecialist to catch. They usually involve the interconnect cabling between sub-assemblies, where the signal wiring and the ground returns are cabled in many directions. Looking simply at the schematic reveals nothing wrong, and it takes a closer look at the point-to-point wiring and layout to visualize the parasitic “antennas.” A few examples of such radiating cable loops are shown in Figs. 9.4 and 9.5.

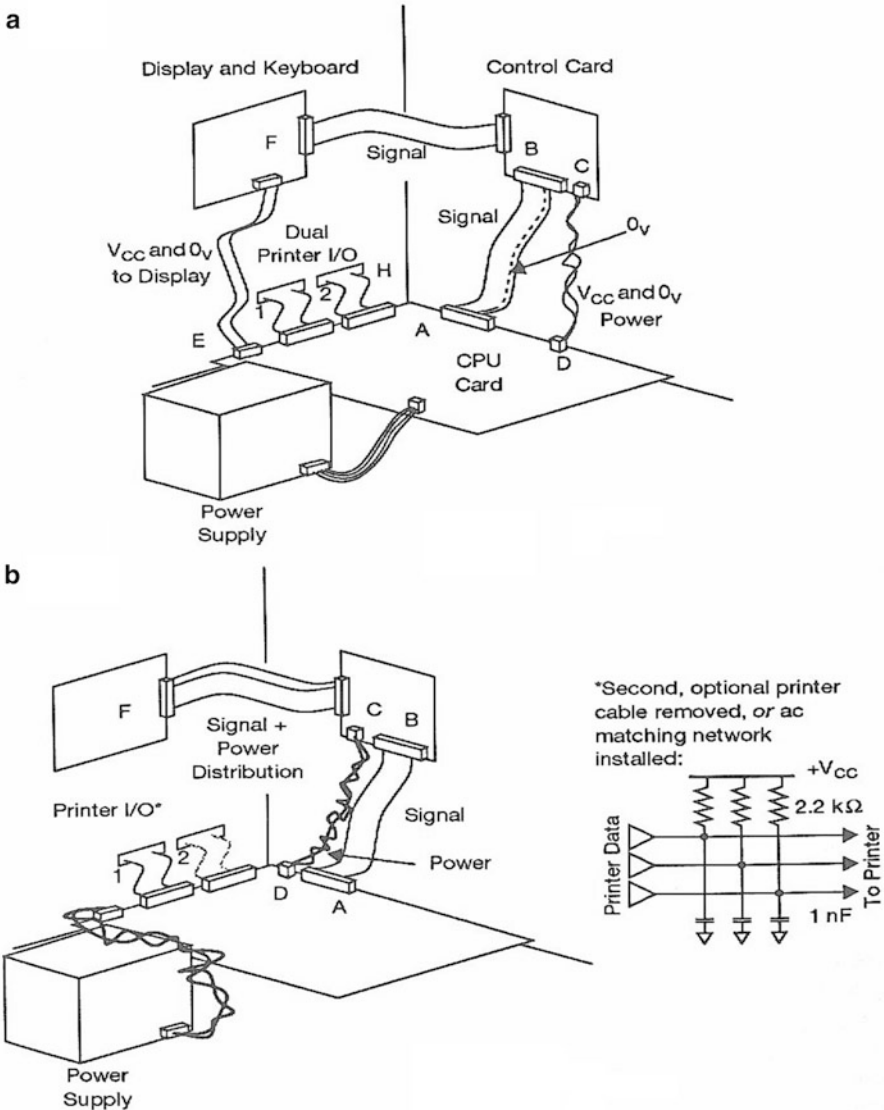
In Fig. 9.4a (top), we see the central processing unit (CPU) board being connected to a control card by a flat cable A-B. The same control card also gets its regulated supply from a pair of signal-ground  $V_{cc}$  and 0 V wires on separate connectors C-D. Although there is one signal-ground wire in the ribbon cable A-B, some percentage of the logic signal currents will return by the alternate path C-D, causing the loop A-B-C-D to radiate. The author has seen a few cases where the situation was even worse: the A-B ribbon cable had no ground wire at all, because the designer feared that two ground wires “would create a ground loop.”

In the same figure, the display/keyboard card is interconnected to the control card and the CPU card by different flat cables. Here again, a small percentage of the digital pulsed currents in the link F-B will return by the ground conductor of the cable F-E, and vice versa, causing the entire loop A-B-F-E to radiate.

Finally, in the same figure, a flat cable goes to the I/O port H, reserved for an optional second printer that is not installed. No loop exists here, but we have an unterminated line that can still receive some signals from the CPU card.

The open end will cause reflection and voltage standing waves, with a peak amplitude twice that of the normal signal. This is a radiating monopole.

Figure 9.4b, shows solutions to this problem, which must be considered early enough in the design stage. The A-B and C-D cables are run very close to reduce loop area. The C-D cable carries enough current to also supply power to the display/keyboard card through the control card. Connector E has been relocated so that the CPU card will interface with the display card through the control card PCB.



**Fig. 9.4** Some large radiating loops in packaging. Notice that most loops are not obvious at first glance. (a) Poor, (b) better

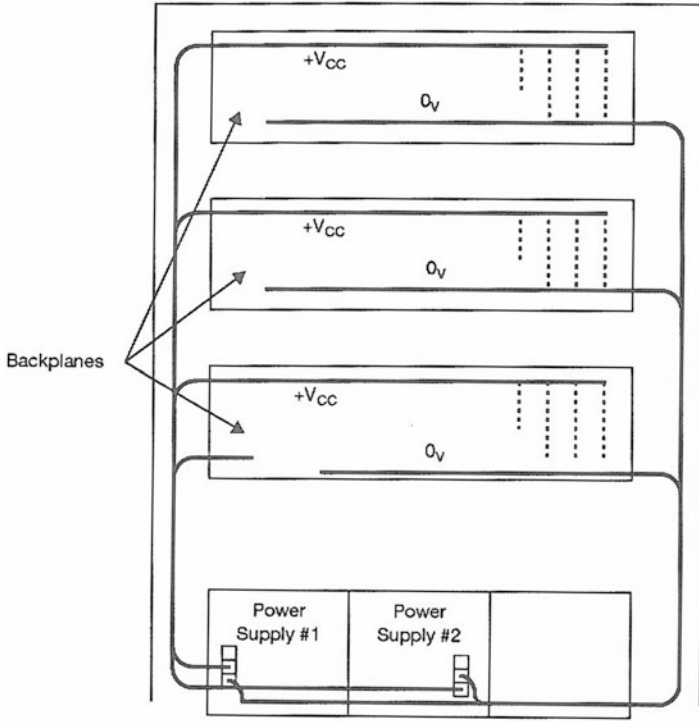


Fig. 9.5 Other large loops on a cabinet's rear wiring

This adds extra printed traces on the latter but eliminates another cable loop. Another fix, quicker but less efficient, would have been to make the original cable E-F longer and reroute it, closely following the A-B-F path. Finally, the cable to the second I/O port can be removed, to be installed only when the option is ordered, or the I/O lines may be terminated near the cable end by an RC network that achieves an approximate AC matching.

Figure 9.5 shows a huge loop, although not always considered to be one (because people do not expect DC currents to radiate). All the HF currents superimposed to the DC supply wires are flowing in loops that can be as large as the entire frame perimeter. These loops will radiate efficiently, especially if the cabinet is not entirely metallic, with proper seams leakage control. Such large DC distributions should be fed from one side of the frame, preferably with flat bus bars, stacking the  $+V_{CC}$  and  $0_V$  bars to form a low-impedance stripline. Then, they should immediately be connected to the backplanes'  $V_{CC}$  and  $0_V$  planes.

## 9.4 INTERNAL CONNECTION OF 0 V REFERENCE AND CORRESPONDING GROUND LOOPS

The two subjects of 0 V-to-chassis connection and ground loops cannot be dissociated. We have already shown (Chap. 2, Sect. 2.5) that floating a 0 V reference from the chassis can be a useful solution for opening low-frequency ground loops, but becomes useless and sometimes actually worse than grounding, above a few MHz. Grounding practices are as likely to create havoc as to solve EMI problems if they are inspired purely by traditions or hearsay.

Considering these facts, it is mandatory that an overall, comprehensive grounding scheme for the system be determined to optimize between (a) LF immunity of low-level electronics (slow analog, audio), which would require a floating reference, and (b) HF immunity and emissions of digital, RF, and video circuits. A given equipment is just one element of a system, and it must adhere to the best grounding scheme devised for this system.

When the equipment incorporates only the type (a), low-level circuits, keeping 0 V floated from chassis and installing efficient HF decoupling on all analog inputs and outputs is the best compromise. In any event, this type of circuit is never a cause of radiated RFI emissions. When the equipment incorporates only type (b), HF circuits, the best results are obtained by tying the 0 V reference to the chassis, at least near the I/O cable entry points and preferably at several places near the edges of the main PCBs.

Conflicts arise when, as is often the case, an equipment incorporates both (a) and (b) circuit types, plus a certain number of internal EMI sources (e.g., relays, motors, cooling fans, transformers, discharge tubes, lasers). As long as wiring lengths are less than  $\lambda/20$ , i.e.,  $\ell(\text{m}) \leq 15/F(\text{MHz})$ ,<sup>1</sup> single-point or star grounding is often most achievable and compatible with other constraints. The rationale for this magic  $\lambda/20$  rule (variations such as  $\lambda/10$  or  $\lambda/50$  are used) is as follows: the value  $\ell = \lambda/20$  is the electrical length where any piece of round wire will represent approximately 100  $\Omega$  of inductive (series) impedance and 1,000  $\Omega$  of capacitive (shunt) impedance. Therefore, this is the frontier up to which any conductor is still a wire (even though no longer a short circuit) and is still far from parasitic resonance.

Internally to an equipment, the star grounding prevents the potential 0 V-to-frame loops from either radiating or receiving, since in principle no current can flow. Star grounding also prevents the signal return current from one building block from flowing through another building block's ground wire, which would create CM impedance problems.

Therefore, each subassembly has its 0 V floated from its compartment, and the compartment is hardwired, or preferably bonded, to the host equipment frame. There is no need and it is generally counterproductive to waste copper and work time by making a star grounding of the subassemblies' housings within the mainframe.

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<sup>1</sup>“ $F$ ” here means the highest frequency of EMI concern that is not necessarily the highest signal repetition rate but the equivalent frequency calculated by  $1/\pi\tau_r$ .

Such practices, in general, occur due to a poor understanding of the single-point ground concept: signal and 0 V ground loops to chassis are potential problems. Chassis-to-chassis, or green-wire to green-wire, loops pose no threat. An equipment that appears to display lessened noise problems when the housings of its internal boxes are star grounded is really just revealing that the bonding of all its mechanical parts is poor or nonexistent.

When a good electrical bonding of all internal parts is restored, by scraping off the paint and tin plating all metallic mating surfaces under screws and bolts, and when the several frames or racks in a bay are made equipotential by several bolts or wide straps, noise problems are reduced more efficiently and across a higher-frequency domain than with hardwired “stars.”

The only exception to this would be subassemblies containing very high voltages (above tens of kilovolts) or very high LF currents (above a 1 kA level, at 50/60 or 400 Hz). Such large items need to have their chassis star grounded with heavy-gauge cables or flat braids because in the case of HV arcing or by mere induction, too much undesirable current would flow in the mainframe.

When the highest frequency of concern reaches tens of megahertz, the single-point concept becomes more or less an unrealistic concept because:

- Grounding conductors exhibit too much impedance.
- Floated circuits become randomly “grounded” through their stray capacitance to the chassis.

For instance, at 100 MHz, corresponding to a rise time of 3.2 ns, our  $\lambda/20$  rule would dictate that the branches of the star do not exceed 15 cm, which is generally impractical. Since this situation occurs more and more frequently as logic speeds increase, the following is recommended:

1. If for some reason there is an absolute requirement to keep all 0 V references floated (this still happens frequently, as some procurement specifications are based on the state of the art of the 1960s):
  - (a) Decouple each logic 0 V-to-frame ground at the motherboard level using a capacitor rated at a few nanofarads and installed with minimum lead inductance (leadless components are best). This still preserves low-frequency isolation (more than 10 k $\Omega$  at 10 kHz) but achieves HF grounding at a controlled location.
  - (b) If the above is insufficient, complement it with a CM ferrite block slipped over the power supply and internal wiring to add series insertion loss above a few megahertz.
2. If floating is not mandatory, ground the logic 0 V to chassis with a low-impedance strap or, preferably, with several screws.

It does not matter if the 0 V-to-chassis connection is permanent or only a high-frequency bypass; the name of the game is to short out to the low-impedance chassis all spurious currents that otherwise would tend to use external cables to return to their sources. This works from the inside out, to control emissions, but it works just



as well for the reciprocal, i.e., preventing outside EMI currents from getting into the PCB.

This brings up an additional question involved in the grounding of the 0 V reference: *the issue is not simply whether to make the connection of the 0 V to chassis but also where to make it.* Focusing on emissions, the dilemma is depicted in Fig. 9.6. In Fig. 9.6a, the 0 V is connected to chassis at the regulated DC supply terminal. This seems to satisfy the general idea of a star connection. However, the far end of the PCB (labeled A) tends to be “hot” with respect to the chassis due to the HF impedance of ground traces and perforated ground planes. If cable ports exist in this area, I/O cables become common-mode-driven antennas. Decoupling capacitors on the I/O port can help in cleaning up the external cable, but their return current, flowing back to the power supply, has to run across the chassis via the path C-B. If the frame and covers have seams and slots, these will radiate (see Chap. 10, Sect. 10.4, Shielding).

In Fig. 9.6b, the reverse approach is used. The “A” side of the PCB is no longer “hot” near the I/O ports, but all SMPS switching noise (mostly CM) flows through the PCB to return to the chassis. As long as the SMPS switching spectrum does not extend above 10-30 MHz, this creates little outside radiation. But it does create a very noisy 0 V distribution, leading to internal EMI or at least reducing the allowable noise margin.

Figure 9.6c, shows an optimum trade-off: the power supply, its power cord entry, and all I/O cables have been grouped on the same face of the equipment frame. The A side of the PCB in the I/O area sees minimal CM voltage to chassis as it is the grounded end, with a maximum current but virtually no voltage. This is why we have repeatedly insisted that this connection be as short and direct as possible.

## 9.5 PACKAGING PRECAUTIONS AT I/O CONNECTOR AREAS

Having stated that all I/O connector and cable entries should preferably be grouped on the same side of the equipment, this face will be the “hot plate” where many RF currents associated with I/O decoupling will flow. But it is easier to make one face particularly RF tight, than to treat this way all six faces of the cubicle.

For radiation control (and immunity as well), all internal leads (wires, printed traces, etc.) arriving at the equipment skin should be decoupled as closely as possible to the point at which they cross the barrier.

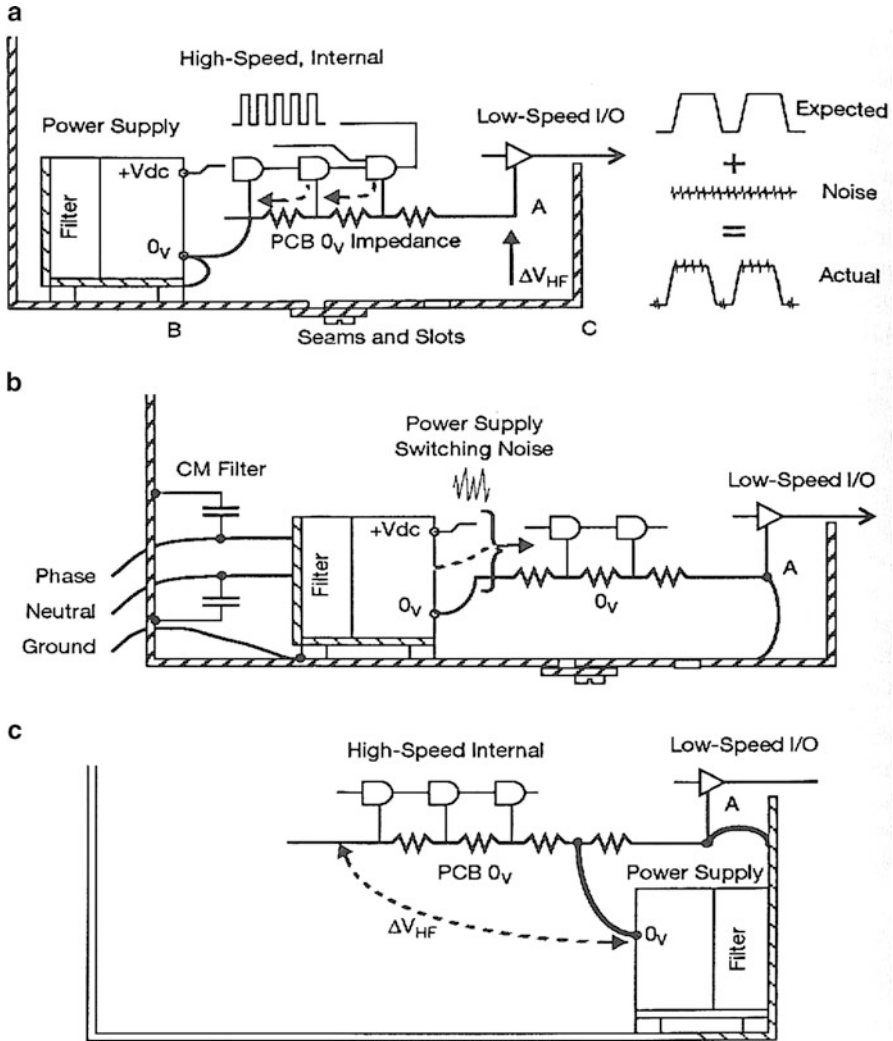
When there is a significant<sup>2</sup> length of internal cabling from the PCB to the connector area, this decoupling has to be made at the connector, because if it is done

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<sup>2</sup> What is “significant” depends, of course, on the frequency of concern. Let’s say that for the VHF range (30-300 MHz), which is a prime concern in radiated EMI, a cable length in excess of 5-10 cm becomes a significant coupling length (see our former  $\lambda/20$  criteria).

just at the PCB/motherboard, it is likely that the cleaned-up segment of cable will pick up HF noise after it has been filtered and then reradiates it outside. A good way to visualize this, although extreme, is in the way shielded EMC test rooms are built: absolutely no cable can get in or out unless it is perfectly shielded or filtered at the very point of penetration.

Decoupling at the I/O port level can be done using either of two approaches:



**Fig. 9.6** Common-mode pollution of PCB and I/O by internal sources. (a) CM pollution of low-speed I/O lines by the hot side of PCB 0 V, (b) CM pollution of PCB by SMPS noise, 0 V grounded at far end, (c) best trade-off between (a) and (b)

1. Apply discrete filtering to each individual conductor, especially where there is a permanent connection rather than pluggable contacts. This can be done with purchased signal filters for high performance or homemade filtering with discrete capacitors if a maximum attenuation of 20-30 dB, up to about 150 MHz, is sufficient. Specific selection or design of EMI filters for I/O ports clean-up suppression will be covered in Chap. 11.
2. Use filtered connectors where each contact is filtered by miniature ferrites and multilayer capacitor arrays. The price of such connectors was prohibitive in the 1990s, when applications were mostly military and quantities were low. As of 2010, a 15-position sub-D socket, with metallic shell and filtering on all contacts, costs no more than \$15 in medium quantities. This compares favorably with the parts cost and labor required to prepare, solder, and check the mounting of 15 discrete element “pi” filters or ceramic capacitors and ferrite beads.

Very often, on smaller equipments, no hardwired interface exists between PCBs and I/O connectors, and the receptacles of those components are directly mounted on the card edges. In some cases, the piece of internal cable is so short that there is no room (or justification) to install filter components anywhere other than on the PCB. Printed circuit board permits some economical and efficient mounting of filter components, and if one-pole filtering (20 dB/decade) is deemed sufficient, simple ceramic capacitors are enough. SMT components allow for economical and non-inductive mounting. The preferred method is to have these capacitors connected to a “chassis ground” copper land on the PCB edge. If such a provision has not been made, the capacitors can be connected to the ground plane, which itself should be connected to chassis, nearest to the I/O ports. In this case, all traces leading to I/O connectors should be decoupled to avoid spurious RF leaks, especially common mode, on the I/O cabling. Specific selection or design of EMI filters for I/O ports clean-up suppression will be covered in Chap. 11.

If filtered connectors of the PCB-mount style are used, one must make sure that the metallic receptacle, which is the capacitor common, is positively grounded to the chassis (or, by default, to the PCB ground plane). The author has seen occasions where a filter connector housing was simply riveted to an epoxy glass board, with no contact to the ground at all. Not only was the filter useless (as discovered by the technician), but the floating common plate of the filter capacitors created crosstalk between the different lines.

In any case, make sure that all I/O lines have been decoupled in the same zone. One single line, even a dormant one, left unfiltered can couple capacitively or magnetically with the others. In Fig. 9.7 the high-speed data line has been filtered close to the equipment case. But an apparently harmless, low-speed line that has just been casually filtered at the output of its PCB can pick up some RF noise from the high-speed line, then radiates it outside.

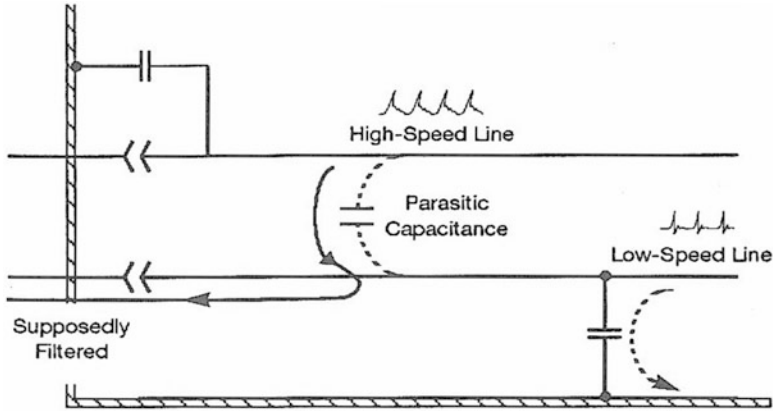


Fig. 9.7 Backdoor reentry of noise when decouplings are not grouped in the same area

## 9.6 A FEW OTHER RADIATED EMI SOURCES

So far, we have been concentrating on SMPS, RF oscillators, and digital circuits as major EMI sources. A few other devices can cause steady intrasystem- or intersystem-radiated interference. The following is a less than exhaustive list of such sources:

- CRTs or LCD displays
- Electroluminescent displays
- Fluorescent tubes or xenon lamps (used inside certain categories of equipment)
- Electric motors (DC and AC)
- Printer head solenoids
- Laser emitters
- Ultrasonic generators
- Plasma and controlled arc generators
- X-ray generators (in addition to their ionizing radiation)

It is difficult to provide characteristic values of the radiated levels for these components, as they depend strongly on the type and manufacturer of these OEM devices. When an equipment incorporates such devices, it is recommended that the designer obtain from the vendor a radiated field profile of the product-the vendor normally will have performed some appropriate test. If no such data is available, a radiated EMI test should be conducted as soon as possible by an independent lab or the prime user. This will serve to identify if (a) the device will cause the host machine to exceed its relevant specification level and (b) the device could cause internal EMI. In either circumstance, proper shielding must be provided.

# Chapter 10

## Box Shielding

All the efforts described in the previous chapters being completed, a conductive box may constitute the ultimate barrier against radiated emissions. However, more often than not, electronic cabinets or equipment housings are designed per one or a combination of the following approaches (which, in other circles, would be quoted as recipes for failure):

1. Make the enclosure similar to earlier versions that are known, or presumed, to be EMI-free. Then, to confirm expectations, test the box when a prototype is available.
2. Starting from the ground up, design and construct a box per mechanical, aesthetic, cost, and accessibility requirements and test it as above.
3. Do as above, but perform only the mandatory emission tests. Do not test for susceptibility unless a specific purchasing specification calls for it.

Such a strategy-or lack of strategy-allows the final test to govern the outcome of a design and results in one or more of the following regrettable situations:

1. Time and money are wasted during the hit-or-miss process.
2. Components or techniques which are not optimized become integral parts of the product.
3. EMC overdesign occurs, with its accumulation of cost, weight, and maintainability issues.
4. EMC underdesign occurs because tests sometimes give a less than complete simulation of all possible EMI situations.

This being said, the designer who prefers an analytical approach faces the following questions:

1. How much attenuation (if any) should the enclosure provide?
2. How can one design an enclosure to meet the attenuation requirements before any prototype exists?
3. If item 1 is not known (as is usually the case), how can it be quantified?

In light of the above, a deterministic approach to the EMC design of the equipment enclosure is needed. The two being related, we will address a

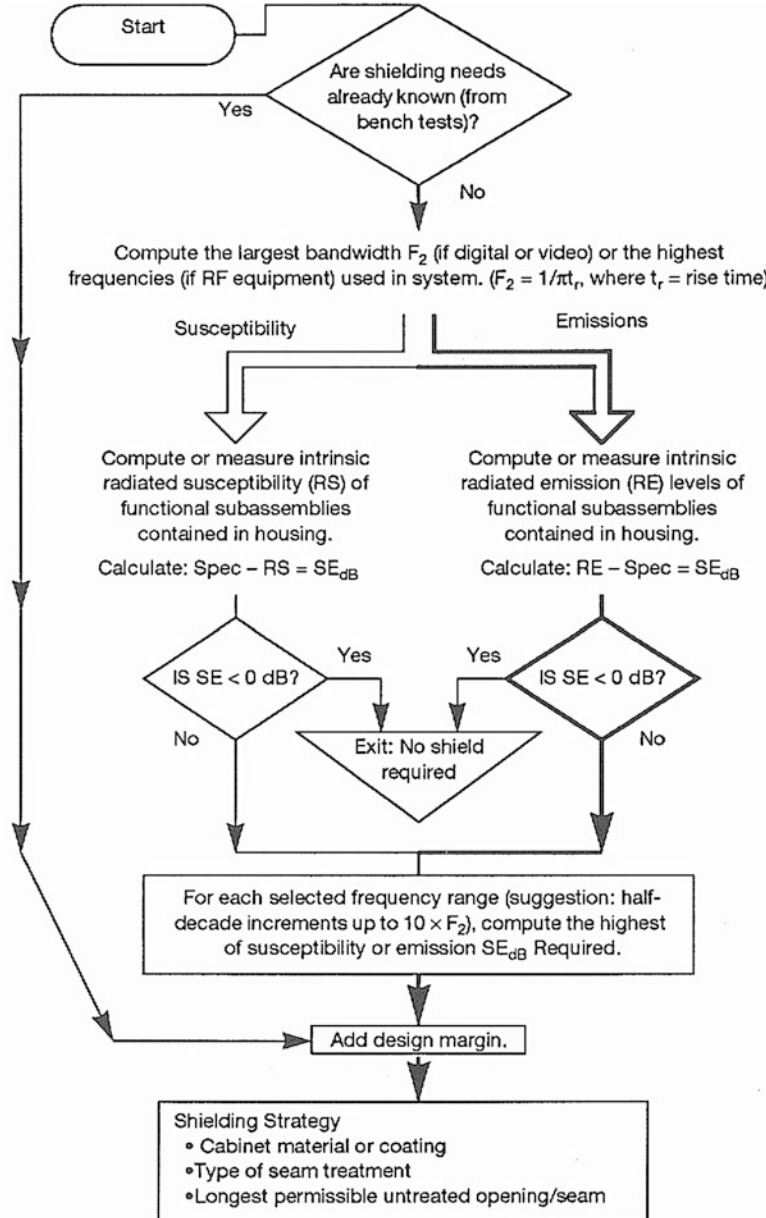
combined emission and susceptibility strategy, then concentrate on emissions for the application part. This strategy is derived from [9] which at the time offered a complete compilation of the knowledge on this subject.

## 10.1 HOW TO DETERMINE BOX ATTENUATION REQUIREMENTS

Using the flow diagram of Fig. 10.1, the designer first asks whether the required shielding effectiveness (SE) is already known across a defined spectrum. While SE requirements generally are not known, there are cases where procurement specifications or test data from a similar equipment dictate the amount of shielding needed. If the SE requirement is known, the routine is bypassed, except (eventually) for adding an appropriate safety margin (exit at the bottom of the figure). Since the needed SE is usually unknown, the flow diagram covers three cases:

1. Shielding for susceptibility hardening
  - (a) Determine the ambient threats (e.g., LF magnetic field, electric field), frequencies, and amplitudes. This is based on the product's intended application and location and provided by applicable immunity specifications. For a new application, if no adequate specifications exist, a site survey is required.
  - (b) Compute, or evaluate, using a prototype, the interference situation via the coupling of fields to internal cables and PCBs. This includes the in-band and out-of-band response of victim circuits.
  - (c) The desired SE is the difference in decibels between the imposed threat and the "bare-bones" susceptibility of the unshielded equipment.
2. Shielding for emission control
  - (a) Compute (see Chap. 2), or measure on development prototypes, the radiated emission levels for each major subassembly to be housed in the box, excluding I/O cables. (Their radiation needs to be addressed and resolved separately from box shielding.) For each frequency interval of at least one decade (half-decade intervals are strongly recommended), record the highest calculated or measured field level up to approximately  $10 \times F_2$ .  $F_2$  represents the highest significant frequency of the voltage or current spectrum, for instance,  $1/\pi t_r$  for pulsed signals (see Chap. 4 "General Strategy").
  - (b) If several amplitudes are in the same range, compute their combined effects. Once the radiated field envelope is drawn across the spectrum for the unshielded electronics, it is compared to the applicable civilian or military specification.
3. Optimized shielding for susceptibility and emission control
 

After items 1 and 2 have been determined, compare in each frequency interval the susceptibility SE (1) and emission SE (2) and retain the tougher of the two requirements. "Tougher" does not necessarily mean the higher figure in dB. For instance, 20 dB of SE against a near-field magnetic source may be harder to achieve than 60 dB against an  $E$  field or plane wave at the same frequency.



**Fig. 10.1** Flow diagram for shielding design. The *right-hand* branch emphasizes shielding against radiated emission (from [9])

The SE requirements having been established, what remains is to select or verify:

- The cabinet material
- The way apertures and seams will be treated
- The surface treatment/finish if specific corrosion and longevity requirements exist

Over the years, clock frequencies have increased constantly. For emission control, the present 1,000 MHz or higher spectrum span obliges the designer to consider possible leakages from any slot that exceeds a few centimeters of maximum dimension.

Decades ago, empirical methods often led to a “steamroller” approach where equipment housings resembled a vault. Such techniques, although effective, increase manufacturing and hardware costs and complicate maintenance and accessibility. In addition, aesthetic and weight considerations prohibit the use of certain shielding materials. Typically, then, the designer will look for shielding techniques that are economical and remain unaltered after intensive use across equipment lifespan. At the risk of overgeneralizing, emission SE requirements are usually less demanding than immunity SE requirements, particularly for military environments. Even with a mediocre design of the PCB and internal packaging (which means the shield will have to make up for internal deficiencies), SEs in the 10 to 40 dB range for civilian applications and in the 30 to 60 dB range for MIL-STD-461 typically will be required at the worst offending frequencies.

## 10.2 SOME SHIELDING BASICS: SHIELDING EFFECTIVENESS OF MATERIALS

Although a comprehensive coverage of shielding theory is far beyond the scope of this book, a few guidelines are provided on how and why shields work and examples are given of when they do not. The reader who wants to know more about the principles and applications of shields is invited to refer to the more complete sources, like Leferink, Mohr and Ott [2, 4, 5], two clear and concise summaries of basic theory. More complete theory can be found in [6, 7, 9, 10].

Shielding effectiveness (SE) is defined as the ratio of the impinging-radiated power to the residual-radiated power (the part that gets through):

For  $E$  fields:  $SE \text{ (dB)} = 20 \log E_{in}/E_{out}$

For  $H$  fields:  $SE \text{ (dB)} = 20 \log H_{in}/H_{out}$

If shields were perfect,  $E_{out}$ ,  $H_{out}$ , and therefore output power,  $P_{out}$  would be 0. In practice, a shield is merely an attenuator that performs on the basis of two principles: absorption and reflection (Fig. 10.2).

Absorption increases with:

- Thickness
- Conductivity

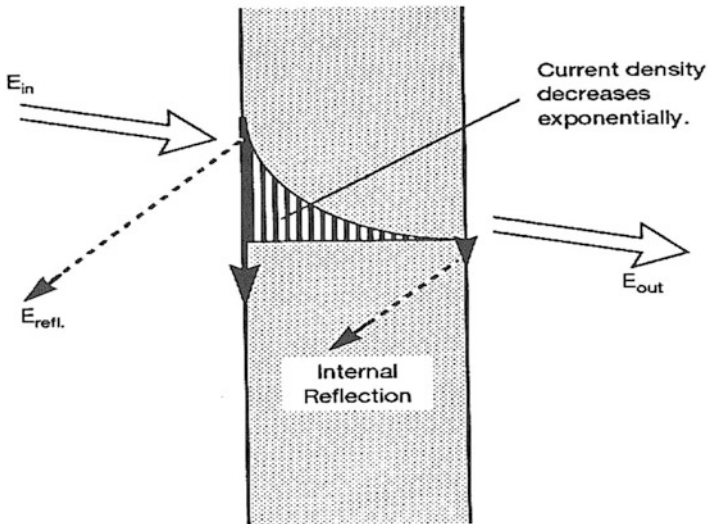


- Permeability
- Frequency

Reflection increases with:

- Surface conductivity
- Wave impedance

*Absorption:* To evaluate *absorption*, or penetration losses, one needs to know how many skin depths ( $\delta$ ) the metal barrier represents at the frequency of concern, knowing that the field intensity will decrease by 8.7 dB (or will lose 63% of its amplitude) each time it has to go through one skin depth.



**Fig. 10.2** Basic shielding mechanisms

Entering all the electrical constants, we come to a simple expression for absorption loss:

$$A_{dB} = 131t\sqrt{F\mu_r\sigma_r} \tag{10.1}$$

where:

$t$  is the thickness of conductive barrier in mm

$F$  is the frequency in MHz

$\mu_r$  is the permeability relative to copper = 1 for nonmagnetic materials (Fig. 10.3)

$\sigma_r$  is the conductivity (the inverse of resistivity) relative to copper = 1 for copper,  $\approx 0.6$  for aluminum, and  $\approx 0.17$  for common construction steel

For example, a 0.03 mm (1.2 mil) aluminum layer will offer an absorption loss at 100 MHz of

$$A(\text{dB}) = 131 \times 0.03 \sqrt{(100 \times 1 \times 0.6)} = 30.4 \text{ dB}$$

This is equivalent to a field strength reduction factor of  $(10)^{30.4/20} = 33$  times.

Looking at Equ. (10.1) leads to a few remarks:

1. *For nonmagnetic materials* ( $\mu_r = 1$ ), the penetration losses increase with conductivity,  $\sigma_r$ . Since no metal offers better conductivity than copper (except for silver, with  $\sigma_r = 1.05$ ), any nonmagnetic metal will show less absorption than copper. Zinc, for instance, with  $\sigma_r = 0.3$ , will exhibit, for a thickness of 0.03 mm (1 mil), an absorption loss at 100 MHz of

$$A(\text{dB}) = 131 \times 0.03 \sqrt{(100 \times 1 \times 0.3)} = 20 \text{ dB}$$

2. *For magnetic materials* ( $\mu_r > 1$ ), the penetration losses increase with  $\mu_r$ . On the other hand, their conductivity is less than copper. Since  $\mu_r$  for steel or iron is in the range of 300-1,000, while  $\sigma_r$  is about 0.17, a definite advantage exists for magnetic materials. However, above a few hundred kilohertz (ferrites excepted),  $\mu_r$  generally collapses to equal 1, while  $\sigma_r$  is still mediocre.

To evaluate *reflection*, one must know if the shield is in near- or far-field conditions.

*For far-field conditions*, the reflection loss is given by

$$R_{\text{dB}} = 20 \log \frac{(K + 1)^2}{4K}, \quad \text{where } K = \frac{120\pi}{Z_b} \quad (10.2)$$

which, for  $K > 3$ , simplifies as

$$R_{\text{dB}} = 20 \log \frac{120\pi}{4Z_b} \quad (10.2a)$$

where  $Z_b$  is the barrier impedance at the interface.

Although for easier comprehension reflection and absorption are presented as two independent factors, they are interacting. The reflection on the air-to-metal interface is combining with the internal absorption, followed by a reflection on the second metal-to-air interface, which in turn is altered by the multiple internal reflections. The Reflection formula Equ. (10.2) is taking into account these in-between mechanisms. However, for a thin barrier whose thickness ( $t$ ) is  $<$  skin depth ( $\delta$ ), no absorption exists, and the shielding attenuation is entirely due to the barrier reflection, without the multiple internal reflections described above. In this specific case, seldom emphasized in literature [1, 9] on shielding, reflection loss is given by

$$R_{\text{dB}} = 20 \log (120\pi/2Z_b) \approx 50 - 20 \log R_b \quad (10.2b)$$

where  $R_b$  is the surface resistance (dc) of the thin film, in  $\Omega/\text{sq}$ .

*Near-field conditions*, where the shield is closer than  $\lambda/2\pi$  to the source, are the most critical ones. For pure electric fields, because their wave impedance is high, it is relatively easy to get good reflection properties because the field-to-shield mismatch is large. For nearby magnetic fields, the wave impedance is low, and it is more difficult to get good reflection. For such *near-field* conditions, the reflection losses are equal to the following:

For  $E$  fields (high impedance),

$$R_{dB(E)} = 20 \log \underbrace{\left( \frac{120\pi}{4Z_b} \right)}_{\text{far-field reflection term}} \times \underbrace{\left( \frac{\lambda}{2\pi D} \right)}_{\text{near-to-far-field correction}} \quad (10.3)$$

where  $D$  is the distance from radiating source in meters.

The second term is the near-to-far-field correction, showing the fact that as frequency increases (decreasing  $\lambda$ ), the high impedance of the field decreases until far-field conditions are reached, for  $\lambda/2\pi D = 1$ .

For  $H$  fields (low impedance), the near-field correction factor is just the reverse:

$$R_{dB(H)} = 20 \log \underbrace{\left( \frac{120\pi}{4Z_b} \right)}_{\text{far-field reflection term}} \times \underbrace{\left( \frac{2\pi D}{\lambda} \right)}_{\text{near-to-far-field correction}} \quad (10.4)$$

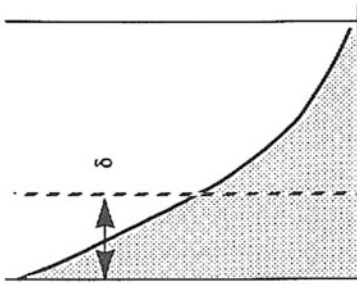
Here again, the second term is the near-to-far-field correction, but this time, as frequency increases (decreasing  $\lambda$ ), the low impedance of the field increases until far-field conditions are reached, for  $\lambda/2\pi D = 1$ . The equation simplifies as<sup>1</sup>:

$$= 20 \log \frac{2DF}{Z_b} \quad (10.4a)$$

where  $Z_b$  is the shield barrier impedance in ohms/square  
 $F$  is the frequency in megahertz

How does one know if at distance  $\ll \lambda$ , the field is more electric or magnetic in nature? By looking at the radiating source, one might gather an idea of the predominant mode: sources switching large currents such as power supplies, solenoid drivers, or large current drivers with more than 100 mA/V generate predominantly magnetic fields. Conversely, voltage-driven high-impedance or open-ended lines create electric fields. Figures 10.3 and 10.4 show shielding properties of some materials.

<sup>1</sup>Note:  $R(\text{dB})$  cannot be negative.  $R$  is a field *attenuation*, never a gain; thus, when  $(D/Z_b\lambda)$  becomes  $< 1$ ,  $R$  must be clamped to 0 dB.



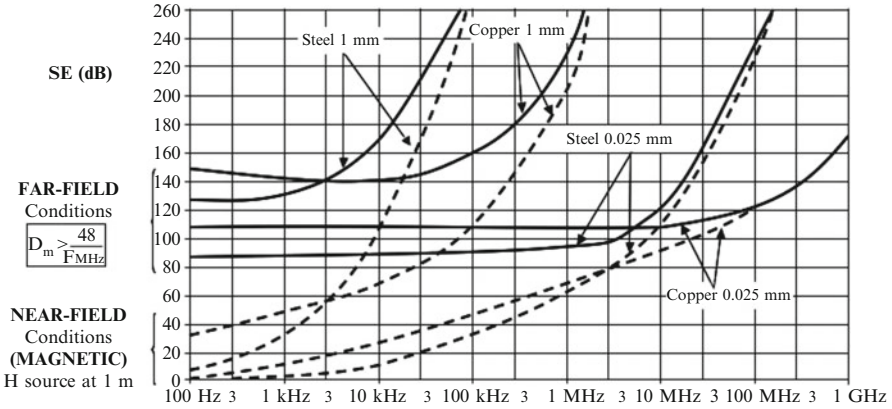
	$\sigma_r$	$\mu_r^*$	Skin Depth, $\delta$			
			60 Hz	10 kHz	1 MHz	100 MHz
Copper	1	1	8.5 mm	0.66 mm	0.066 mm	6.6 $\mu$ m
Aluminum	0.6	1	11 mm	0.85 mm	0.085 mm	8.5 $\mu$ m
Steel (ordinary cold-rolled)	0.16	200	1.4 mm	0.14 mm	0.1 mm	16 $\mu$ m
Steel (low-carbon)	0.1	1,000	0.85 mm	0.06 mm	0.04 mm	20 $\mu$ m
Conetic	0.032	20,000	0.33 mm	0.058 mm	0.058 mm	38 $\mu$ m
$\mu$ metal	0.028	20,000 to 60,000	0.34 mm	0.058 mm	0.058 mm	40 $\mu$ m

Thickness (mm)	Absorption Losses (dB)					
	Copper	Aluminum	Zinc	Steel*	Nickel* $\sigma_r = 0.2$	Copper Paint† $\sigma_r = 0.04$
30 MHz	0.01 0.1 1 70 700 >1,000	0.01 0.1 5.2 52 700 >1,000	0.01 0.1 4 40 400 >1,000	0.01 0.1 3 28 200 >1,000	0.01 1 3 31	0.05 mm (2 mil) 7
100 MHz	13 130 22 220 >1,000	9.5 95 170 >1,000	7 72 125 >1,000	5 50 88 880	6 58 10 98	13 22

\* Although steel and nickel are magnetic materials, their relative permeability  $\mu_r$  collapses to  $\approx 1$  above a few hundred kilohertz. This has been considered in calculating  $\delta$  and losses.

† Nonhomogeneous metal

Fig. 10.3 Skin depths and absorption losses for various materials (reminder: absorption does not depend on the near-electric, near-magnetic or plane wave nature of the field)



**Fig. 10.4** Total shielding effectiveness (absorption + reflection) of a few common metals. *Solid lines (top)*: far-field conditions. *Dotted lines (bottom)*: against *H* field sources at 1 m distance. The curves for 1 mm copper can be used for 1.25 mm (0.05") aluminum. Curves for 0.025 mm copper (1 mil) can be used for 0.03 mm aluminum

### 10.3 SHIELDING EFFECTIVENESS OF CONDUCTIVE PLASTICS

Plastic housings provide no shielding whatsoever. Therefore, unless the PCBs and internal wiring have been hardened sufficiently, the plastic must be made conductive. Several metallizing processes exist, as summarized in Table 10.1, along with their average 2009 costs. Since, as discussed in Sect. 10.2, thin coatings exhibit a poor absorption loss, their only chance to work is by reflection. Based on reflection loss only, Fig. 10.5 shows the shielding effectiveness of thin coatings. (A more detailed explanation can be found in [10]). If shielding effectiveness in the range of 40-50 dB is desired, especially against low-impedance sources, a conductive process with 1 Ω/sq or less must be selected.

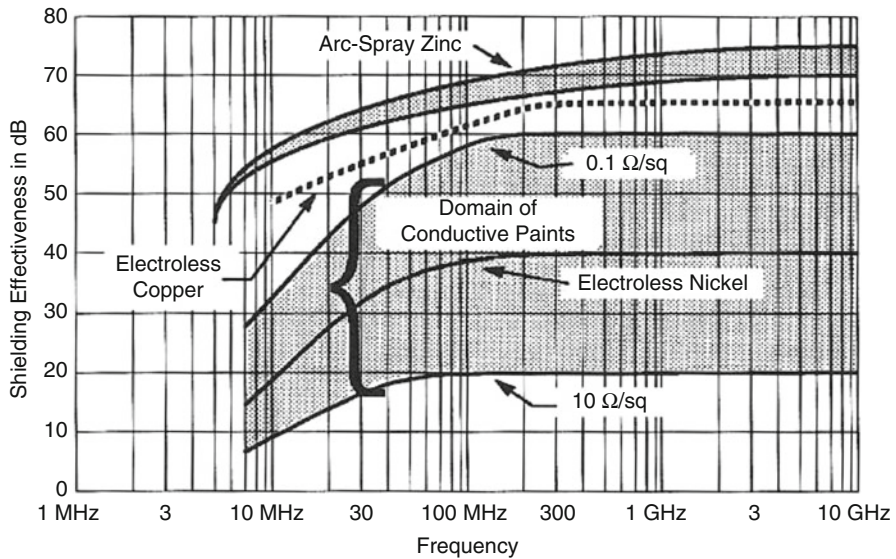
The case of emission shielding with metallized plastic is more critical. Since the sources are inside the box, the thin conductive surface very often will be in near-field conditions. At 10 cm from a source, one has to wait until 500 MHz is reached to be in a far-field situation. Because many of the radiating sources (e.g., current loops, capacitors discharges, bus drivers) exhibit less than 377 Ω impedances, the reflection performances of metallized plastics will be less than their far-field figures.

In addition, contrasting to the susceptibility case, the reflected wave does not vanish in the exterior but comes back after a two-way trip inside the box. If this re-reflected wave comes in phase (this occurs when the two-way trip reaches  $\lambda/2$ , i.e., box length reaches  $\lambda/4$ ), we have a resonant cavity, and effective SE will be less than calculated. This is why, ironically, a high-conductivity thin layer, giving

excellent reflectivity and no absorption, is not the best barrier against emissions. Lesser conductivity but a thicker coat can give better results provided that

$$t_{\text{new}}/t_{\text{old}} > \sigma_{r(\text{old})}/\sigma_{r(\text{new})}$$

In this expression,  $t_{\text{new}}$  is the thickness of the thicker, less conductive barrier, and  $t_{\text{old}}$  is that of the thinner barrier. In this respect, conductive plastics with volume conductivity provided by conductive particles are more efficient than thin conductive paints or films.



**Fig. 10.5** Shielding effectiveness of conductive plastic processes, at distance  $D = 0.30$  m. For frequencies below 100 MHz, the near-field source is magnetic. For SE at closer distance, *subtract*  $20 \log[30 \text{ cm}/D(\text{cm})]$

**Table 10.1** Average cost ranges of conductive treatments on plastics

	Cost in \$/m <sup>2</sup>	10	20	30	50	100	200
	Surface res. (Ω/sq)						
Copper paint: (50 μm thick)	0.2						
Nickel paint: (50 μm thick)	0.3-0.8		---				
Graphite paint: (50 μm thick)	10-300	----					
Silver coating: (13-25 μm thick)	0.06						----
Hot zinc spray	0.05					-----	
Electroplating	0.1			----			
Electroless plating: (1 μm thick)	0.1				-----		

Year 2009 figures compiled from several sources (Parker/Chomerics, MAP, Acheson). Graphite works only against high-impedance,  $E$ -field shielding

## 10.4 FIELD ATTENUATION THROUGH APERTURES

Housings, unfortunately, cannot be made like continuous metal cubicles. They have slots, seams, and other apertures that inevitably leak. Like for a chain, a shield is only as good as its weakest link; therefore, it is important to know the shield's weak points in order to match realistic objectives.

- At low frequencies, what counts is the nature of the metal and its thickness, conductivity, and permeability.
- At high frequencies, where any metal would provide hundreds of decibels of shielding, such figures are never seen because seams and discontinuities completely spoil the metal barrier (see Fig. 10.6).

### 10.4.1 Attenuation of One Single Aperture

From Babinet's theory, a slot in a shield can be compared to a slot antenna which, except for a  $90^\circ$  rotation, behaves like a dipole (see Fig. 10.7). When the slot length reaches  $\lambda/2$ , no matter how small the height ( $h$ ), this non-intentional antenna behaves as a perfectly tuned dipole, i.e., it re-radiates outside all the energy that excites the slot from inside. It may even exhibit a slight gain of about 3 dB. Below this resonance, the slot leaks less and less as frequency decreases.

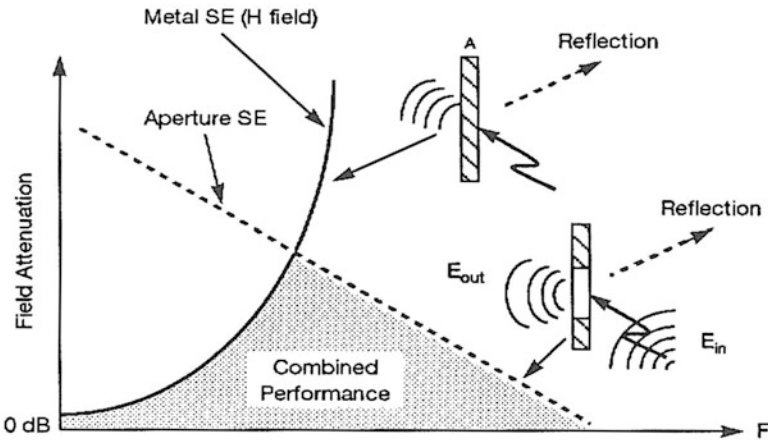


Fig. 10.6 Attenuation of field by an aperture compared to attenuation by a perfect metal barrier

A simplified expression gives aperture attenuation below  $\lambda/2$  resonance (from [9]). It is the worst-case far-field attenuation, for the worst possible polarization (in general, actual attenuation will be better):

$$\begin{aligned} A(\text{dB}) &= 100 - 20 \log \ell - 20 \log F(\text{MHz}) + 20 \log [1 + 2.3 \log(\ell/h)] + 30d/\ell \\ &= 0 \text{ dB} \quad \text{for } \ell \geq \lambda/2 \end{aligned} \tag{10.5}$$

where  $\ell$  is the length (largest dimension) of aperture in mm

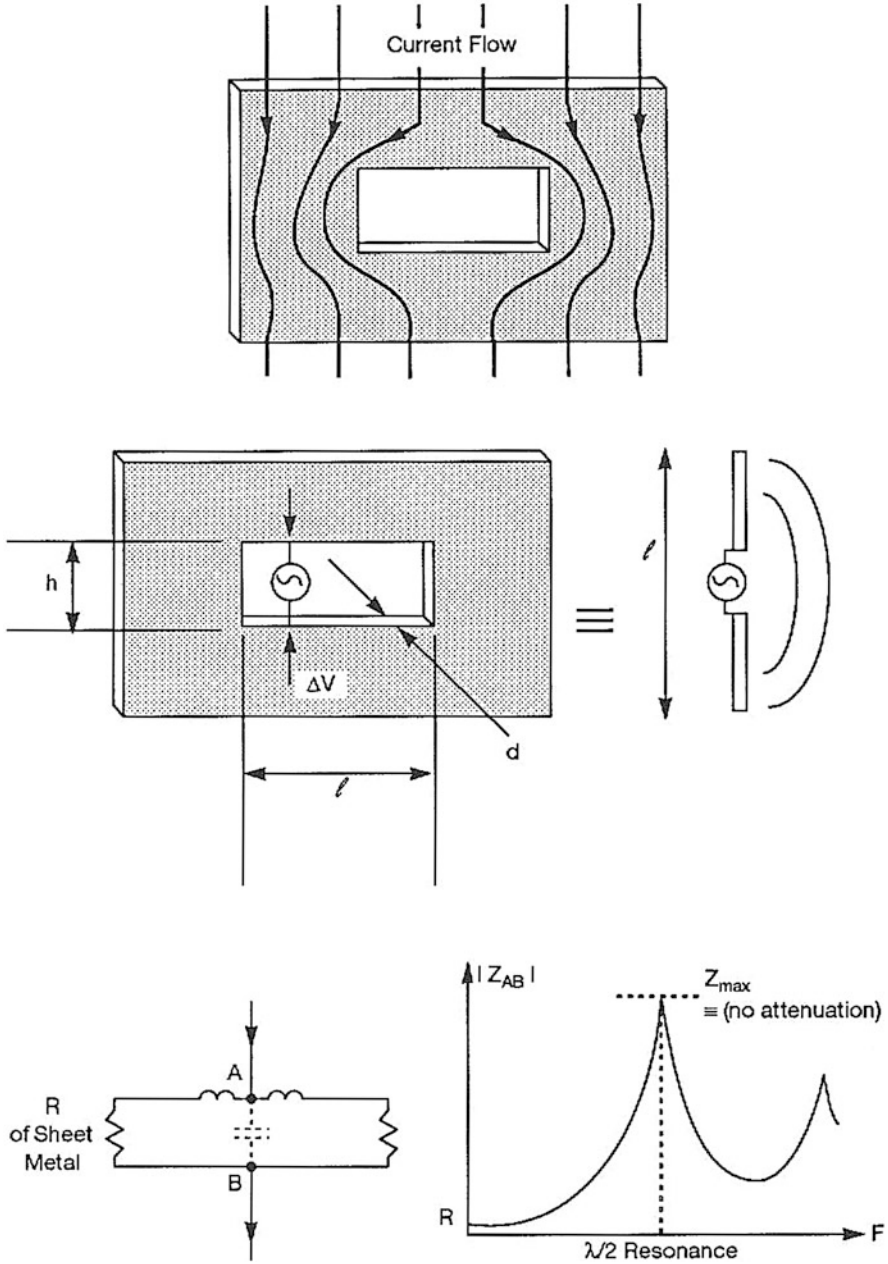
$h, d$  is the height and depth of the aperture (no unit given since it is the ratio  $\ell/h$  or  $d/\ell$  that counts)

The first three terms in Equ. (10.5) represent the reflection loss of a square aperture, due to the mismatch of the incident wave impedance ( $377 \Omega$  for far-field conditions) with the slot impedance. The 100 dB constant represents the  $\lambda/2/\ell$  attenuation ( $20 \log 150 \times 10^3/\ell$ ) of a square aperture, with an added  $\sqrt{2}$  margin for diagonal polarization. The equivalent circuit for a slot is an inductance (Fig. 10.7), until it resonates with the edge-to-edge capacitance. The fourth term is the “fatness factor” of the slot, taking into account the effect of  $h$ . Notice that  $h$  plays only a secondary role by the logarithm of  $\ell/h$ . A slot 100 times thinner will not radiate 100 times less than the equivalent square aperture, but only five times less. Some typical values of this factor are:

$$\begin{aligned} 0 \text{ dB} & \text{ for } \ell = h \text{ (square aperture)} \\ 10 \text{ dB} & \text{ } h/\ell = 0.1 \\ 15 \text{ dB} & \text{ } h/\ell = 0.01 \\ 18 \text{ dB} & \text{ } h/\ell = 0.001 \end{aligned}$$

The last term in Equ. (10.5),  $30 d/\ell$ , is the guided wave attenuation term, as it would happen in a real waveguide below its operating frequency. This term is directly given in decibels. It has only some influence if  $d$  is a significant fraction of  $\ell$ . For ordinary sheet-metal enclosures where  $d$  is equal to the metal thickness, this term is negligible. For small holes, or artificially lengthened holes (Fig. 10.8), the added attenuation is significant.





**Fig. 10.7** Effect of a discontinuity in a shield. At low frequency, slot impedance  $Z_{AB}$  is approximately a short circuit: reflection is significant

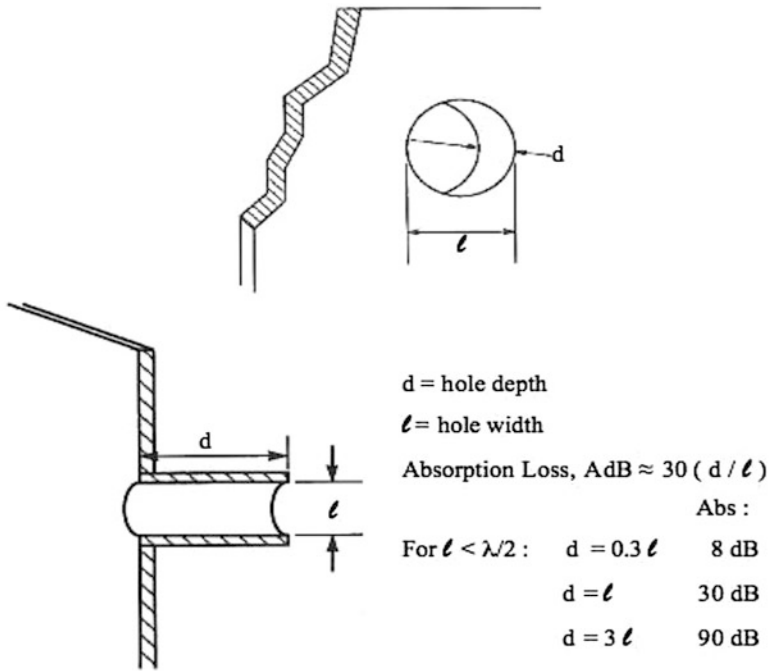


Fig. 10.8 Additional attenuation offered by lengthened holes (waveguide below resonance)

### 10.4.2 Effect of Multiple Apertures Leakages

A question often arises: how can we estimate the combined effect of several apertures, whether they are similar or not? The following are some guidelines for the most frequent cases:

(a) **Several apertures: scattered and not identical:**



Compute  $A(\text{dB})$  for each one and then using the antilog (expressing the leakage, i.e., the reverse of an attenuation), combine them to get the global leakage. For instance, assume that calculations using Equ. (10.5) has given the following:

- Aperture #1: 20 dB, that is, a relative leakage of 0.1 (meaning 10% of field gets through)
- Aperture #2: 14 dB, that is, a relative leakage of 0.2
- Aperture #3: 40 dB, that is, a relative leakage of 0.01

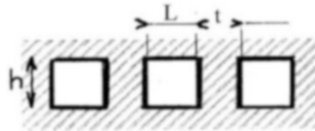
The total leak is  $0.1 + 0.2 + 0.01 = 0.31$ , that is, a total attenuation =  $-(20 \log 0.31)$  or 10.2 dB. As predictable, the total attenuation is less than  $A_{\#2}$ , the worst one. This will be the case for the next example.

**(b)  $N$  apertures: identical but scattered (*not adjacent*):**



Compute  $A(\text{dB})$  for one and *subtract*  $20 \log N$ . This is a worst-case approach, assuming that all openings are re-radiating in phase, which is not entirely true. Of course, if there are many apertures, such as the result is approaching 0 dB, the total SE must be clamped to 0 dB: slots cannot result in a negative loss and amplify the field (except for some limited gain due to a beamwidth effect).

**(c)  $N$  apertures: identical, not scattered, and *adjacent*:**



(Thickness of ribs  $t$  is  $< \ell$  or  $h$ , the opening dimension perpendicular to the rib.)

Compute  $A(\text{dB})$  for *only one* aperture. *Do not subtract*  $20 \log N$  or  $10 \log N$  (as mentioned in some literature). This is due to the fact that when identical holes are separated by thin ribs, mutual cancellation occurs by the edge currents (see Fig. 10.9, bottom).

Let us take a numerical example: Large square opening,  $100 \times 100$  mm, Frequency 100 MHz.

$$A(\text{dB}) = 100 - 20 \log(100 \text{ mm}) - 20 \log(100 \text{ MHz}) = 20 \text{ dB}, \text{ a serious leak}$$

Assume we screen it with a  $50 \times 50$  cells wire mesh, that is, an array of  $50 \times 50$  cells, each one is  $2 \times 2$  mm.

$$\begin{aligned} A(\text{dB}) \text{ (one cell)} &= 100 - 20 \log(2 \text{ mm}) - 20 \log(100 \text{ MHz}) \\ &= 54 \text{ dB@100 MHz} \end{aligned}$$

The largest dimension (length and width are the same here) has been divided into 50 small (2 mm) elements. Improvement is  $20 \log(50) = 34$  dB, that, added to the

20 dB of the naked aperture gives 54 dB, that is the same attenuation as one single 2 mm hole.<sup>2</sup>

**Example 10.1** Calculate, for 1-1,000 MHz, the far-field attenuation of the openings in the metal rack of Fig. 10.9:

1. Display aperture,  $60 \times 20$  mm.
2. Cooling fan aperture,  $100 \times 100$  mm.
3. Cover seams  $\ell = 300$  mm,  $h = 0.3$  mm.
4. Cooling slots  $\ell = 100$  mm,  $h = 3$  mm, thickness of metal ribs,  $t = 2$  mm.
5. Open slots on front panel edges  $\ell = 15$  mm,  $h = 5$  mm. The remaining open-ended slot of length  $\ell/2$  leaks as much as a closed slot of length  $2\ell$ : it has two times more inductance and sees twice more current because of the image of the missing half plane (right hand on Fig. 10.10).

**Solution** The metal thickness on all faces is 2 mm. It will be assumed that in this whole frequency domain, the metal SE is much higher than any slot SE (a quick estimate for 2 mm aluminum shows  $>200$  dB at 1 MHz up).

1. *Display*

$$\begin{aligned} \text{SE} &= 100 - 20 \log 60 \text{ mm} - 20 \log F(\text{MHz}) + 20 \log(1 + 2.3 \log 60/20) \\ &= 64 - 20 \log F + 6 \\ &= 70 \text{ dB} - 20 \log F \\ &= 0 \text{ dB above } \lambda/2 \text{ resonance, at } F = 150 \times 103/\ell = 2,500 \text{ MHz} \end{aligned}$$

2. *Cooling fan*

$$\begin{aligned} \text{SE} &= 100 - 20 \log 100 \text{ mm} - 20 \log F \text{ (no fatness term for square hole)} \\ &= 60 - 20 \log F \\ &= 0 \text{ dB above } \lambda/2 \text{ resonance, at } 1,500 \text{ MHz} \end{aligned}$$

3. *Cover seams*

$$\begin{aligned} \text{SE} &= 100 - 20 \log 300 \text{ mm} - 20 \log F + 20 \log(1 + 2.3 \log 300/0.3) \\ &= 50 - 20 \log F + 18 \text{ dB (fatness term)} \\ &= 68 - 20 \log F \\ &= 0 \text{ dB above } \lambda/2 \text{ resonance, at } 500 \text{ MHz} \end{aligned}$$

---

<sup>2</sup>It may look strange, and nonintuitive, that, for instance, a grid of  $10 \times 10$  holes, each one being 5 mm diameter does not leak 100 times more than one single 5 mm hole. However, let us consider this: if a grid of  $N$  holes was leaking  $N$  times more than one single hole, screen meshes would never work. In fact, *they do work*, and theory supported by experiments proves that when the holes are exactly similar and only separated by thin wires or ribs, a mutual cancelation takes place between adjacent holes. Note: if  $N$  holes are separated by a metal rib wider than  $\sqrt{(\ell h/2)}$ , no mutual cancelation occurs, and the  $N$  holes behave as  $N$  independent sources: they do leak  $N$  times more than a single one [2].

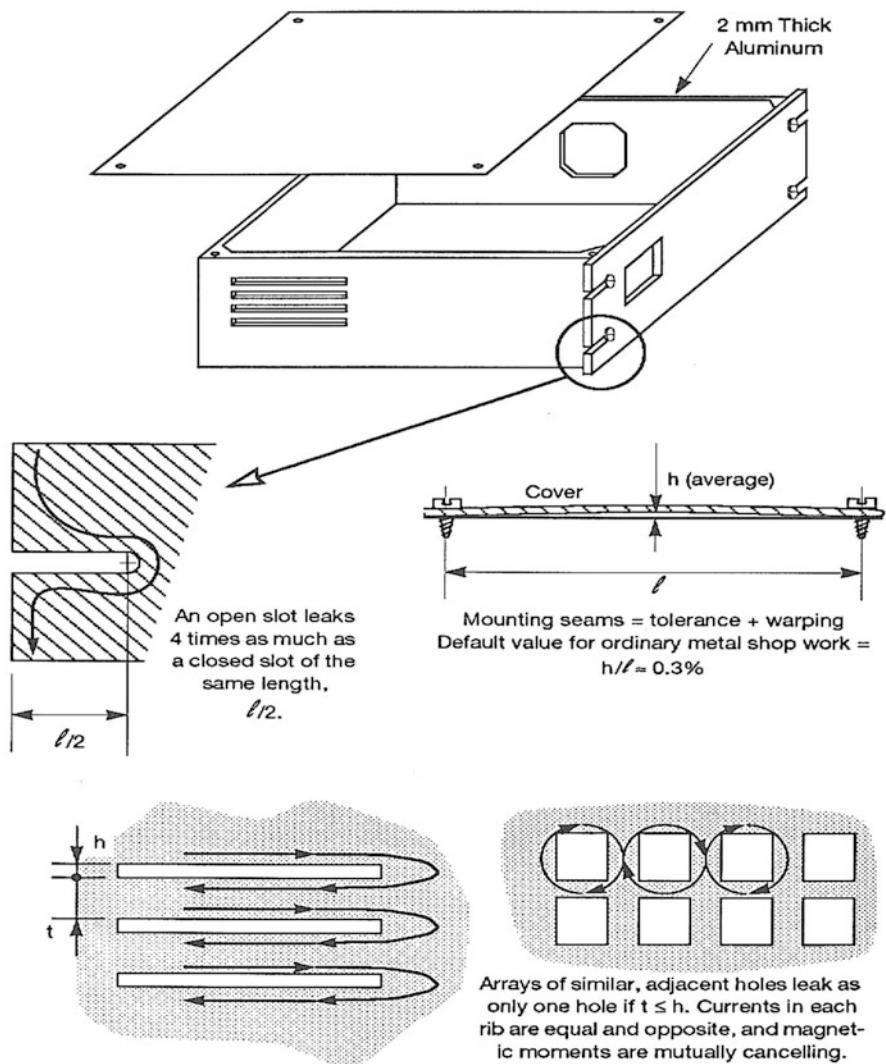


Fig. 10.9 Box from Example 10.1, with typical leakages

4. Cooling slots

$$\begin{aligned}
 SE &= 100 - 20 \log 100 \text{ mm} - 20 \log F + 20 \log(1 + 2.3 \log 100/3) \\
 &= 60 - 20 \log F + 13 \\
 &= 73 - 20 \log F (\text{only one slot is considered because } t \text{ is } < h) \\
 &= 0 \text{ dB above } \lambda/2 \text{ resonance, at } 1,500 \text{ MHz}
 \end{aligned}$$

### 5. open-sided slot

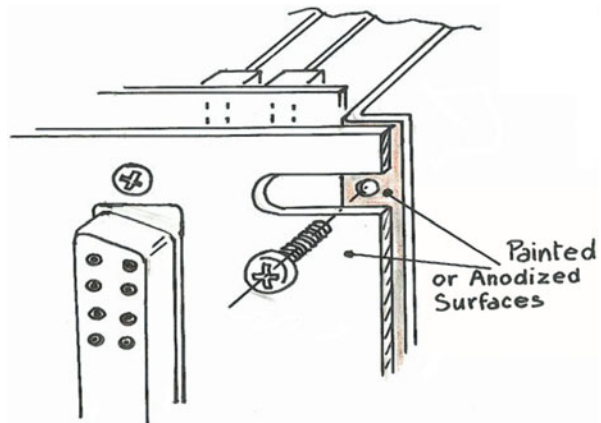
This will leak four times more than a 15 mm slot, because the screw head on the open end, and the front plate, being pressed on anodized surface, does not make a good electrical contact with box edge (Fig. 10.10):

$$\begin{aligned} SE &= 100 - 20 \log(4 \times 15) - 20 \log F + 20 \log(1 + 2.3 \log 60/5) \\ &= 64 - 20 \log F + 8 \text{ dB} \\ &= 72 - 20 \log F \\ &= 0 \text{ dB above } 2,500 \text{ MHz} \end{aligned}$$

Notice that this simple edge slot leaks practically as much as the display opening if it is excited by an internal, nearby source.

These five expressions will give us the attenuation of all these apertures at any frequency.

**Fig. 10.10** Detail of open-ended slot leakage. Such hidden slot could leak if the mounting hardware (screw and flanges) does not restore a good electrical bond of the end gap



## 10.5 ALTERATIONS OF THE IDEAL “HOLE-IN-A-WALL” MODEL

The above calculations for both metal SE and aperture SE are assuming a rather academic situation where:

- The metal wall has quasi-infinite dimensions or at least very large vs. the source-to-shield distance such as the current density in the plain shield (before any leakage exists) would be uniform.
- The reflected wave does not encounter any opposite wall, causing multiple reflections.

Reality is different:

- (a) Electronic cabinets have finite dimensions, causing current concentrations at the edges.
- (b) Radiating sources can be rather close from the box walls openings, such as a wide portion of the concerned frequency range is in a near-field condition.
- (c) The box will behave as a cavity excited by internal sources, if one or several of the circuit frequencies meet the natural box resonance frequencies.

Item (a) is of no great consequence, except that some apertures might be in zones of the box walls where there is practically no current, such as the aperture will not be excited. Calculated SE will be pessimistic, making our predictions conservative. Items (b) and (c) are addressed next.

### 10.5.1 Effect of Source Proximity on Aperture Leakage

As previously mentioned, aperture SE in the near field departs significantly from its plane wave expression of Equ. (10.5). Since the wave impedance will differ from  $377 \Omega$ , the reflection term will be affected, being higher (greater SE) with a predominantly electric field and lower with a predominantly magnetic field.

In Chap. 2, Sect. 2.3, we showed that wave impedance with actual radiators cannot possibly be higher than the “ideal” electric dipole nor lower than the “ideal” magnetic loop and in most cases is bound by the radiating circuit impedance  $Z_c$ . Setting aside the case of pure  $E$  field, which is academic for virtually all radiated EMI problems, it can be demonstrated that when the radiating source within a box is in near-field conditions (i.e., distance  $D_{(m)} < 48/F(\text{MHz})$ ), two conditions may apply:

1. If  $Z_c > 7.9/(D_{(m)}F(\text{MHz}))$ , Equ. (10.5) is modified for the attenuation against an ideal  $E$ -field source:

$$\begin{aligned} \text{SE (near } E\text{-field)} &= 48 + 20 \log Z_c - 20 \log \ell(\text{mm})F(\text{MHz}) \\ &\quad + 20 \log [1 + 2.3 \log(\ell/h)] + 30 d/\ell \quad (10.6) \\ &= 0 \text{ dB for } \ell \geq \lambda/2 \end{aligned}$$

2. If  $Z_c < 7.9/(D_{(m)}F(\text{MHz}))$ , Equ. (10.5) is modified for the attenuation of a slot against an ideal  $H$ -field loop:

$$\begin{aligned} \text{SE (near } H\text{-field)} &= 20 \log \pi D/\ell + 20 \log [1 + 2.3 \log(\ell/h)] + 30d/\ell \quad (10.7) \\ &= 0 \text{ dB for } \ell \geq \lambda/2 \end{aligned}$$

Notice that this last expression becomes independent of frequency, as long as the near-field criterion and condition 2 both exist. In most cases, condition 1 is true, which gives better SE than condition 2. Condition 2 can be considered as the worst conceivable lower boundary of aperture SE against pure  $H$ -field sources.

As a recap of the previous sections, Fig. 10.11 confronts skin attenuation vs. slot attenuation for typical emission conditions, with distance  $D = 10$  cm. It is clear that, very rapidly, as  $F$  increases, the SE of any box skin is bypassed by aperture leakages, which become the governing factors for overall box SE. However, a poor-quality conductive plastic with conductive coating resistance  $>2 \Omega/\text{sq}$  can be the limiting factor for the entire box SE up to a hundred MHz, compared to the attenuation of relatively small apertures.

## 10.5.2 Effect of Box Natural Resonances

For a rectangular metal box with dimensions  $\ell$ ,  $w$ , and  $h$ , the natural resonance frequencies of the waveguide TExx modes are given by:

$$F_{\text{res}} = 150 \sqrt{\left[ \left( \frac{m}{\ell} \right)^2 + \left( \frac{n}{w} \right)^2 + \left( \frac{p}{h} \right)^2 \right]} \quad (10.8)$$

where  $\ell$ ,  $w$ , and  $h$  in meters.

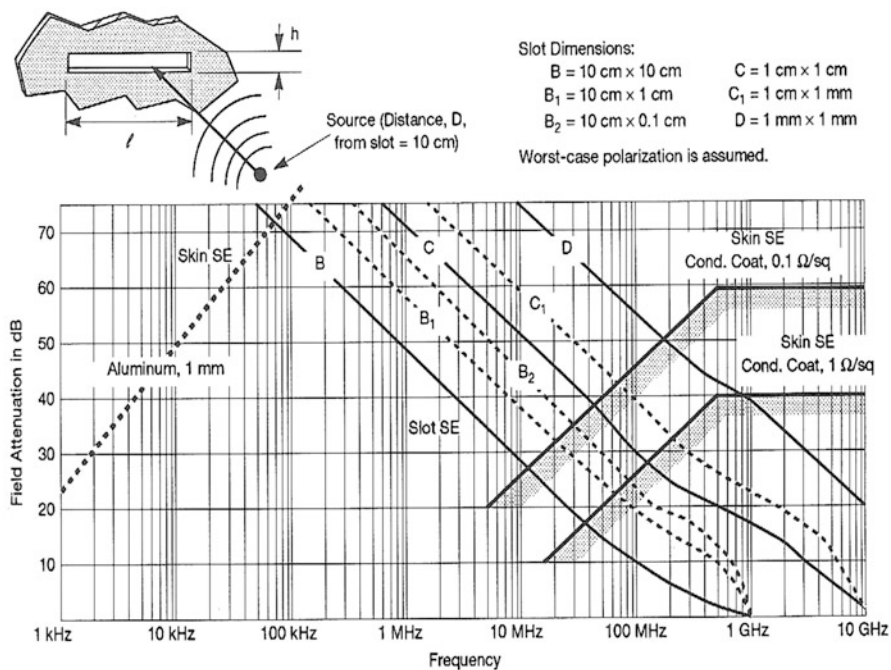
The terms  $m$ ,  $n$ , and  $p$  are integer numbers which can take any value, but no more than one at a time equal to 0. For instance, with the box example of Fig. 10.10, the first natural resonances exist at

$$F_1 = 707 \text{ MHz}, F_2 = 1,120 \text{ MHz}, \text{ etc.}$$

At these specific frequencies, an empty metal box could exhibit resonances with a  $Q$  factor as large as 10 (20 dB), which could result in a negative SE (an apparent “gain”). Hopefully, electronic equipment boxes are never empty but filled with PCBs, components, and cables which are behaving as scattered lossy elements, such as the measured  $Q$  stays within 0-10 dB, with typical values of 6 dB.

This doubling of the inside field results in an apparent 6 dB drop of the expected SE at every self-resonance frequency. If the box is large in dimension with relatively small apertures, this 6 dB notch of the first resonances occurs at rather low frequencies where SE is high enough to afford this loss. But when it comes to resonant frequencies that are less than one octave below the cutoff frequency for the largest opening, the box SE will drop to 0 dB faster than expected. Some manufacturers of shielding products are offering lossy composites with surface resistivity  $>10 \Omega/\text{sq}$  that can be used like an anechoic coating inside the enclosure.





**Fig. 10.11** Skin attenuations (aluminum and conductive paints) vs. apertures attenuations, facing a low-impedance source at 10 cm. A 100 Ω source impedance is assumed. If source is closer, SE will decrease proportionally

## 10.6 METHODS OF LEAKAGE REDUCTION AND APERTURE TREATMENT

A conductive housing already has the basic advantage of being a naturally efficient barrier. All the talent of the designer should be aimed at not spoiling this barrier with excessive leakages. Leakages (i.e., poor SE) are caused by:

1. Seams at mating panels, covers, etc. (a frequent cause of SE spoiling)
2. Cooling apertures
3. Viewing apertures for displays, meters, etc.
4. Component holes: fuses, switches, shafts
5. Cable or miscellaneous conduit penetrations

## 10.6.1 Mating Panels and Cover Seams

The general, simple rules are as follows:

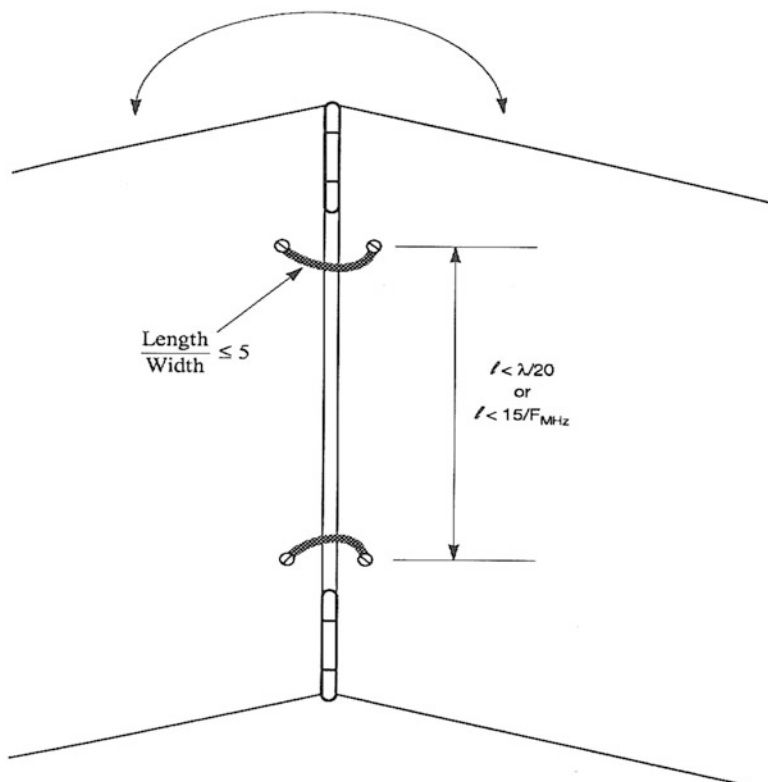
All metal parts should be bonded together.

A floated item is a candidate for re-radiation.

For cover seams, slots, and so forth, how frequently they should be bonded is a question of the design objective. Figure 10.11 shows that a 10 cm leakage is worth about 20 dB of shielding in the neighborhood of 150 MHz. If the goal is closer to 30 or 40 dB, seams or slots should be broken down to 3 or 1 cm. For permanent or semipermanent closures, this means many screws or welding points or an EMC conductive gasket. For covers, hatches, and such, this means flexible contacts or gaskets. In any case, it is always a safe practice to design fold-over shapes to the cover edges. With a sufficient overlapping, a sort of waveguide “labyrinth” is formed that adds some penetration loss. By doing this, one could complement the use of gasket or even avoid them.

The following is a sequential organization of these solutions. As efficiency increases, cost increases as well.

- If only minimal shielding effectiveness is needed, in the 0 to 20 dB range, the simplest technique is to have frequent bonding points and, for covers, short flexible straps made of flat braid or copper foil as shown in Fig. 10.12. This solution bonds only on the hinge side, but if no noisy cables or devices are located near the opposite side of the hinge, this can be sufficient. For this unbonded opposite side, a wise precaution is to use several grounded locks or fasteners. The  $\lambda/20$  criterion shown in Fig. 10.12 means that for a maximum emission frequency of 100 MHz, the distance between jumpers should stay within 15 cm for a 20 dB shielding objective, and up to 45 cm if a 10 dB reduction is sufficient. However, for emission shielding, this criteria would imply that the emission source inside is at a distance greater than 45 cm from the leaky seam, which may not be the case (see Sect. 10.5.1).
- If bonding only the hinged side leaves an excessive length of ungasketed seams, more bonding points are necessary. In this case, the techniques of Fig. 10.13 can be used. Fig. 10.3a shows an example of a soft spring, several of which being scattered along the cover edges. For durable performance, the spring contact riveting must be corrosion-free, which may render this solution more difficult to apply than it would seem.



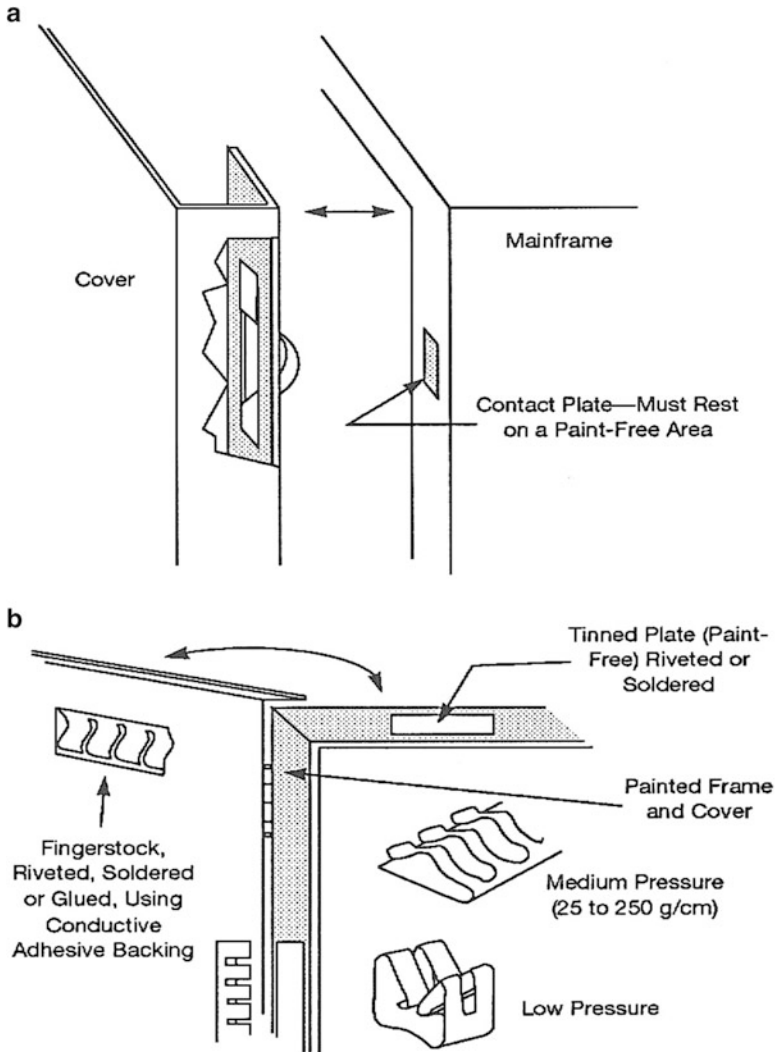
**Fig. 10.12** Leakage reduction by frequent seam bonding (for moderate shielding needs)

A variation of it, shown in Fig. 10.13b is to use sections of spring contacts called fingerstocks. Several types of fingerstocks are available, such as low-pressure, knife-edge, and medium-pressure styles. They require an adequate control of pressure through tight manufacturing tolerances, but they are extremely dependable. A third technique, shown in Fig. 10.14, is an interesting alternative that takes minimal surface preparation. The grounding “buttons,” which are fairly compliant to gap variations due to their loading, are mounted simply by press fit or a threaded stud.

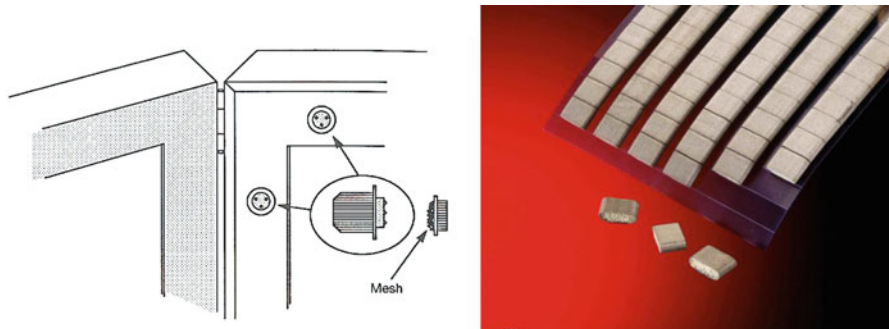
If a higher grade of shielding is required (20-60 dB), a continuous conductive bonding of seams is necessary, since an SE of 40 dB at 300 MHz ( $\lambda/2 = 50$  cm) would require screws or rivets spacing of less than 1 cm! These continuous conductive joints are available in several forms and stiffnesses (Fig. 10.15). Metal braid or mesh-type gaskets provide higher shielding, close to or beyond the upper side of the required SE range.

Hollow rubber gasket is less expensive to use because its wide elasticity compensates for large joint unevenness and warpage. The counterpart for this is a lesser contact pressure, hence higher resistivity; it is best used as a solution for the lower side of the SE range. Here again, a good quality mating surface can be made by applying conductive tape over the metal surface before painting. Then a piece of masking tape is pressed over the conductive foil, and the metal surfaces

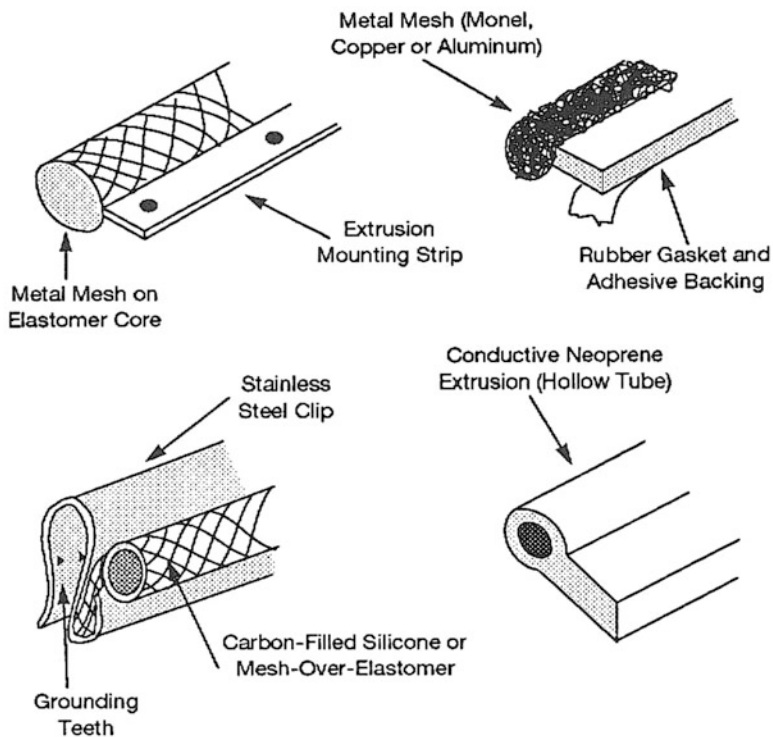
can be painted, after which the masking tape is carefully peeled off. The contact resistance of such conductive tapes after hard compression must not exceed few  $m\Omega/sq$ . For applications that require long-term exposure to harsh environments, one must take into account that the conductive adhesive backing of these tapes does not behave well with aging, with a tendency to polymerization of the glue after several years.



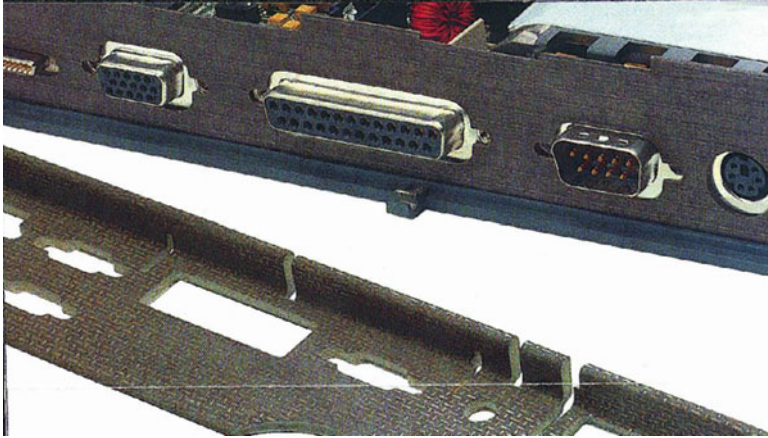
**Fig. 10.13** Maintaining shield integrity by evenly spaced, flexible bonding points. (a) Captive beryllium-copper springs are located along cover edges. When closed, they mate with abutting frame edge. Contact plates can be nickel or tin plated or made from adhesive conductive tape. (b) Partial bonding by knife-edge or regular fingerstock.



**Fig. 10.14** *Left:* Press-fit grounding buttons (LAIRD Co.). *Right:* soft grounding pads (Chomerics/Parker div.)



**Fig. 10.15** Compressible RF gaskets and mounting styles



**Fig. 10.16** Conductive textile gaskets with foam core (from Schlegel Co.)

Finally, if an even higher hardening level is necessary, the ultimate solution is shown in Fig. 10.17. This solution is the most efficient because 100% of seam becomes a very good conductive joint, and it is the one favored for shielded rooms. Besides its direct cost, it adds the need for a strong locking mechanism to ensure good, even pressure on all of the spring blades. This method is applicable to both rotating (hinged) and slide-mating surfaces.

Whatever the choice, conductive elastomer core, mesh, or spring fingers, all gaskets require an adequate design of covers and box or frame edges to provide:

- A smooth seating plane or groove, with well-conductive surface finish, for the gasket
- Proper mechanical tolerances to avoid gasket overpressure at some places (lower-tolerance gap), causing permanent gasket flattening, and underpressure at others (higher gap) resulting in insufficient contact

In all cases, when a continuous metal-to-metal contact is required, with or without an intermediary EMC gasket, surface conductivity is paramount to an effective bonding. Mating areas must be paint-free, but in any case, bare metal is generally treated against corrosion. These treatments are not all good conductors:

- Anodized aluminum is nonconductive.
- Bichromate olive green, and most aluminum treatment make poor, unstable contacts.
- Alodine provides a decent conductivity, but the process has been banned due to its toxicity. It has been replaced by neutral chromate treatments, like chromitAL/SurTec.
- Zinc or nickel, plating provides a good conductivity.

For metallized plastic housings, the seam treatment needs only to be proportionate to the box skin SE, which is generally more modest (typically less than 50 dB below 100-200 MHz). If the conductive coating is resistant to abrasion, mating edges can be designed to provide an electrical continuity, without the need for gasket. This is done by using tongue-and-groove or other molded profiles for assembly (Fig. 10.18). The relative compliance of plastic provides the necessary contact pressure of the conductive surfaces.

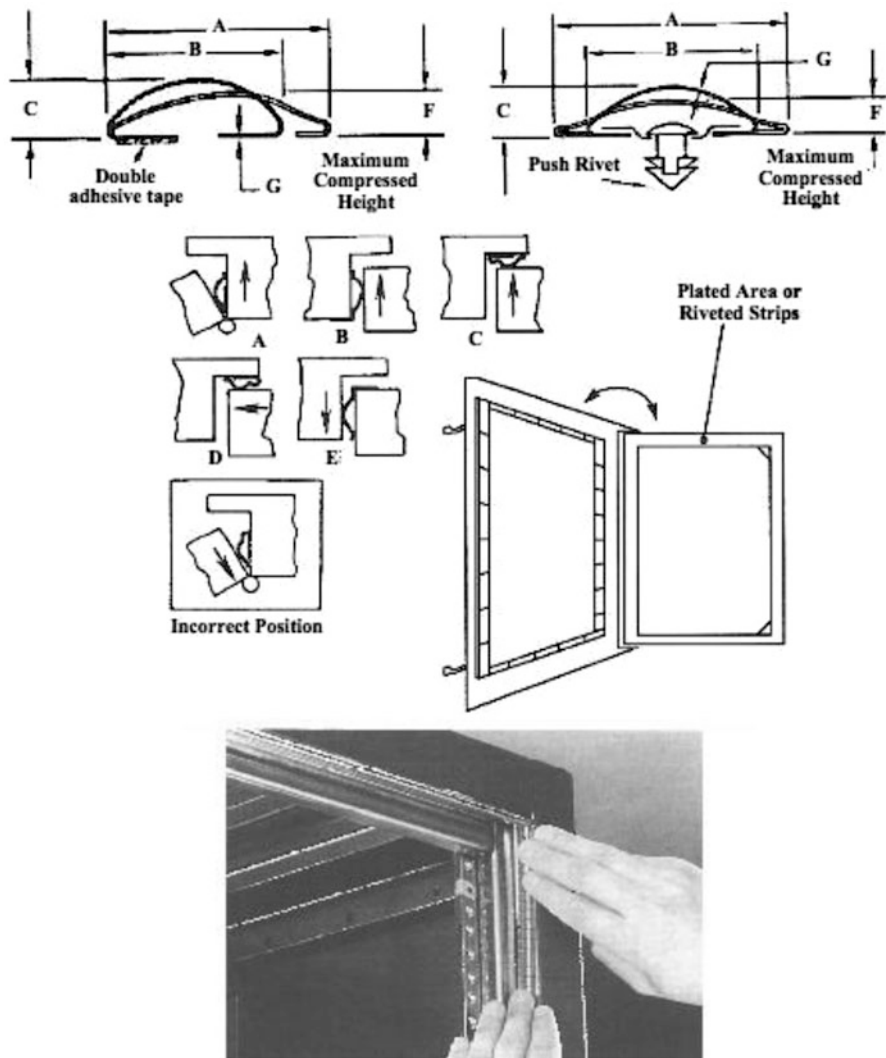
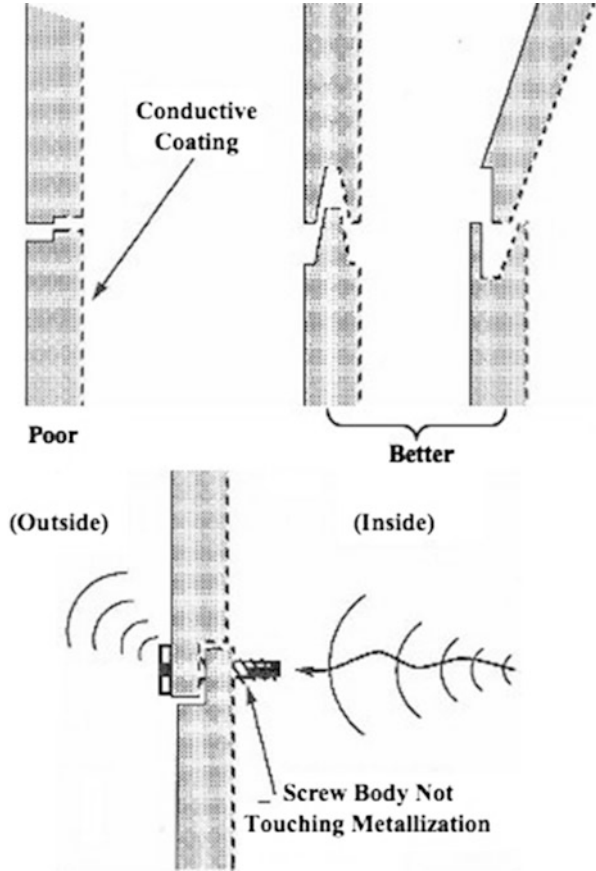


Fig. 10.17 Fingerstocks with 100% perimeter coverage (courtesy of LAIRD Co.)

**Fig. 10.18** Metallized plastic box design against radiation. Conductive coat should extend far enough into the tongue-and-groove shape to make a continuous contact, but not too far (avoid ESD problems). *Bottom:* avoid long, protruding screws that are likely to be not or poorly grounded, since they can become re-radiating RF antennas



### 10.6.2 Shielding for Cooling Apertures

Several techniques can be used to restore shield integrity at convection or forced-air cooling vents (Fig. 10.19):

1. Break large openings into several smaller ones. This has the advantage of virtually no cost if the holes are produced during stamping or molding of the box walls. It also can put the source at a relative greater distance, compared to the aperture size, eliminating some proximity effect. The improvement is

$$\Delta \text{ (dB)} = 20 \log (\text{old length}/\text{new length})$$

or simply  $\Delta(\text{dB}) = 20 \log N$ , if  $N$  is the number of identical holes that are replacing one larger aperture.

This is done by replacing long slots with smaller (preferably round) apertures. If some depth can be added to the barrier such that  $d > \ell$ , the waveguide term in Equ. (10.5) becomes noticeable, improving SE.



2. Install a metal screen over the cooling hole. This screen has to be continuously welded or fitted with a conductive edge gasket having an intrinsic SE superior to the overall objective.
3. Install a honeycomb air vent if an SE greater than 60 dB is required above 500 MHz and up to several GHz, along with a low aerodynamic pressure drop.

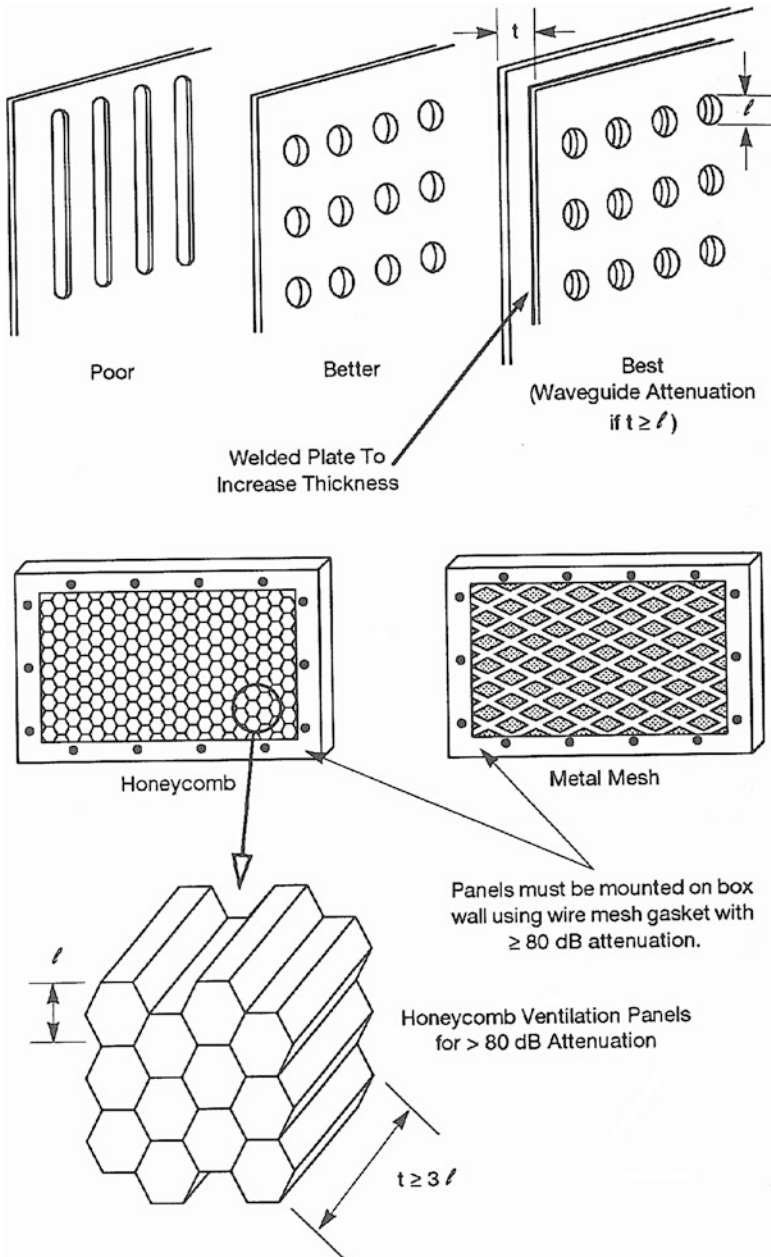


Fig. 10.19 Methods of shielding cooling apertures

### 10.6.3 Shielding for Viewing Apertures

CRTs or LCDs, alphanumeric displays, meters, and the like are often the largest openings in an equipment box, offering the lowest SE of all packages. On the other hand, typical high-frequency sources are seldom mounted right on or behind display panels. Compared to the typical RF “hot plate” represented by a filter mounting panel or I/O connectors interface cards area, experience shows that most equipments can tolerate rather large, unshielded apertures on their user’s display panel, while a ten-times smaller slot in the cable entry zone would radiate significantly. In a sense, the intrinsic SE of any aperture being calculable, its radiation still depends on whether it is excited. Since one does not know in advance how RF currents will be distributed on the box’s inner skin, we will keep with the conservative assumption that viewing apertures are as prone to leak as any other ones. The shielding solutions are:

1. Finely knitted or woven wire mesh, on top of, or sandwiched in the glass, plexiglass or other material. Densities of up to 12 wires/cm (knitted mesh) or up to 100 wires/cm (woven product) are obtainable. The performance can be derived from the curves of Figs. 10.20 and 10.21. The denser mesh offers more SE because the individual holes are smaller, but this is at the expense of transparency. A modern, expensive alternative is the photolithographic deposit of a thin copper mesh.
2. Transparent conductive film, where a thin film of gold or indium tin oxide (ITO) is vacuum deposited on the transparent substrate. The film thickness has to be low ( $10^{-3}$  to  $10^{-2}$   $\mu\text{m}$ ) to keep an 80 to 60% optical transparency, but the thinner the film, the more the surface resistance. Typical transparent coatings have surface resistivities in the range of 50 to 5  $\Omega/\text{sq}$ , corresponding to far-field SE of 10-30 dB. Near *E*-field SE would be better. One recent promising technique [8] is the deposit of a silver nanoparticles emulsion, creating a random mesh pattern.
3. Shielding the display from the rear side: the display is shielded behind the box panel by a doghouse, which is equipped with feedthrough capacitors for connecting wires (see Fig. 10.22).

In all three of the solutions described above, an EMI gasket is needed at the shield-to-box joint. Often, one such fitting is already provided by the shielded window vendor.

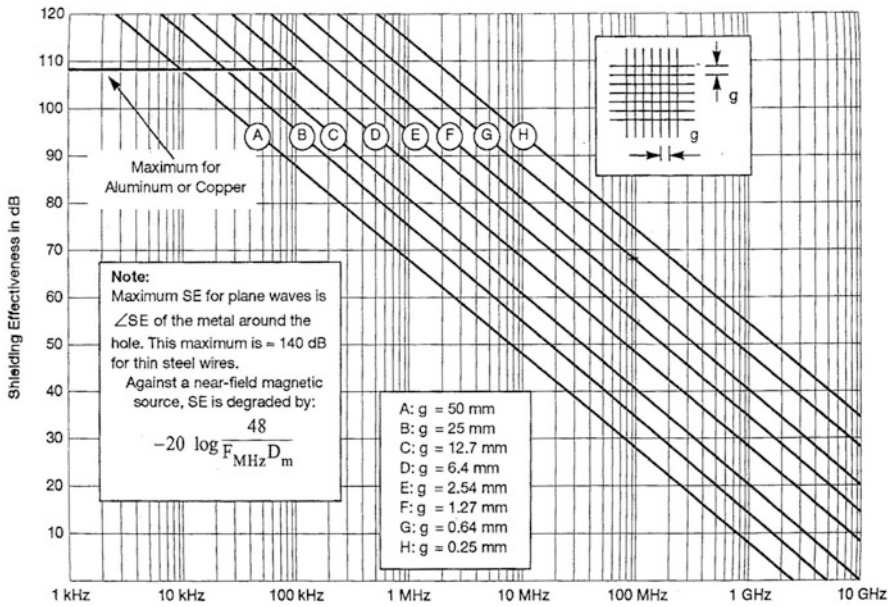


Fig. 10.20 Shielding of screen wire shields, in far-field conditions (distance in meters  $> 48/F$  (MHz))

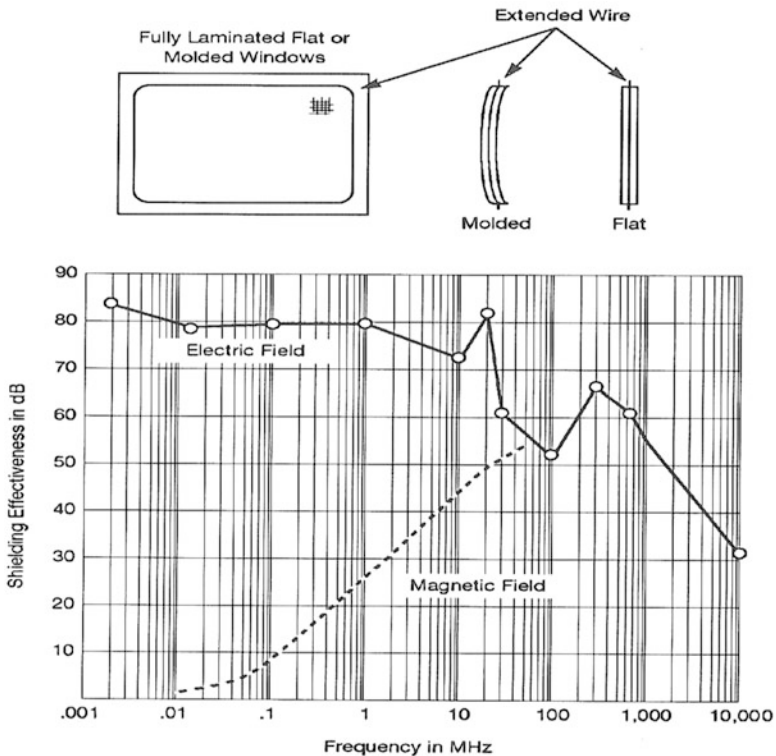
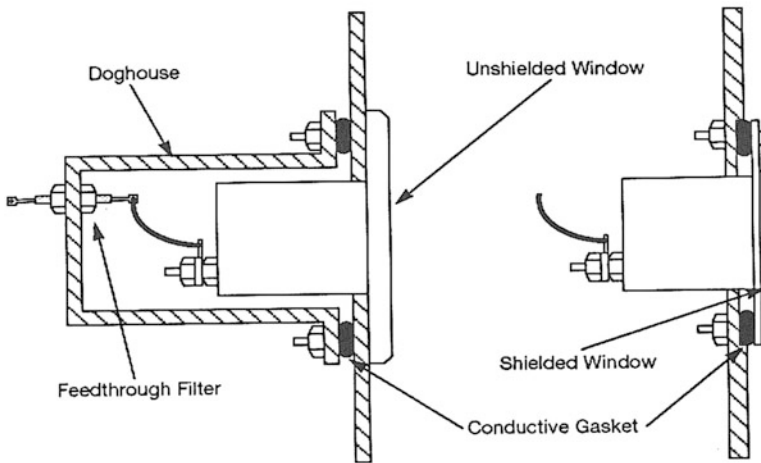


Fig. 10.21 Shielded transparent windows for displays, thin-mesh version with 100 wires per inch, laminated and antiglare treated (source: DonTech, USA)

### 10.6.4 Shielding the Component Holes

Holes for potentiometer shafts, switches, lamps, fuseholders, etc. generally are small. But their mere presence in the middle of metal pieces that have picked up CM current from inside the box will enhance the radiation phenomenon. The shaft, lever, or fuse cartridge will act as a monopole, exiting via a coaxial line: just what is needed to transmit radio signals. As far as FCC, CISPR, and other civilian limits are concerned, component holes are seldom a problem because of the relatively small leakage. With MIL-STD-461 or TEMPEST emission limits, component holes can become significant contributors to EMI radiation.



**Fig. 10.22** Shielding of meter and display openings. Feedthrough filters prevent the wiring to act as an antenna

The solutions are as follows:

1. Use nonconductive shafts or levers and increase the hole depth with a piece of metal tube to create a waveguide attenuation.
2. Use grounding washers or circular contact springs to make electrical contact between the shaft and panel.
3. Use shielded versions of the components.

### 10.6.5 Shielding of Cable Penetrations, Connectors, and Nonconductive Feedthroughs

Last but not least, this breach in box skin integrity is a serious concern, since cables are the largest potential RF carriers in the entire system. The shielding (or no shielding) of the cable penetrations depends on the decision chart of Fig. 10.23. From the first decision (evaluation of cable entry hole), the designer will follow one of two paths:

1. Calculation of box SE shows that the cable exit hole is tolerable (answer “Yes” at step 1). However, even if the box is correct, the cable can behave as a radiator. If the cable needs to be shielded for radiation (and/or susceptibility), its shield must properly terminate at the barrier crossing via a 360° clamp, ultrashort strap, or, best of all, a metallic connector shell. If the cable is not shielded but still is a threat, each of its conductors must have been filtered (see Chaps. 9 and 11). There is no point in shielding the hole.
2. Calculation of box SE shows that the cable exit hole is not tolerable (answer “No” at step 1). In this case, it becomes imperative to use shielded cable and shielded connectors, creating a sort of shielded enclosure for the entire interconnect cabling system.

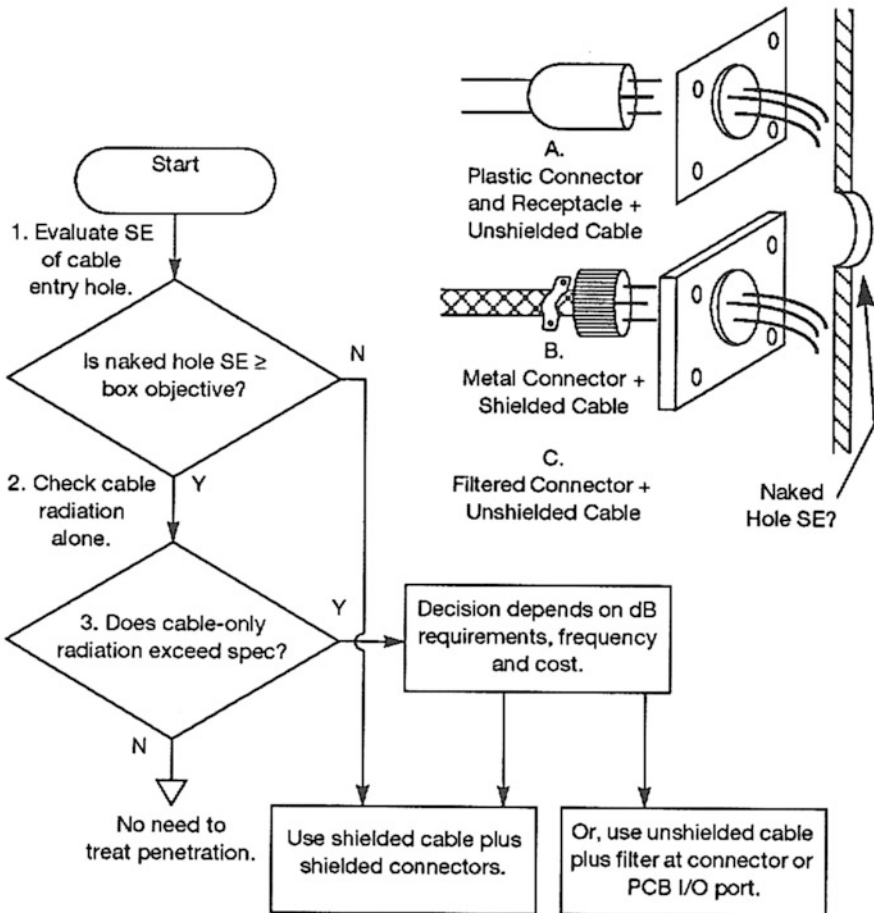


Fig. 10.23 Decision chart for shielding of cable penetrations

A trade-off version would be to use unshielded cable but to block aperture leakage with a shielded and filtered connector receptacle. This would recreate a recessed shield barrier behind the cable hole. The interface of cable shields at box penetration is a topic indissociable from cable shielding. This matter is addressed in Chap. 11.

Some other exit/entry ports exist for nonconductive lines such as pressure sensors, fluid lines, fiber optics, etc. If the tube is nonconductive and the SE of the naked hole is insufficient, this type of leakage is easily reduced by using the waveguide effect. For fiber optics, transmitters, and receivers, metallic packages are available with appropriate tubular fittings.

### 10.6.6 Detrimental Effect of Box Leakages Near a Cable Penetration

When a cable exit is located in the proximity of a slot leakage (e.g., open-edged slot, warped joint), the slot attenuation is locally less than its theoretical far-field value. In fact the exciting source inside can couple to the first centimeters of the outside cable segment (Fig. 10.24) by a mechanism which is closer to magnetic or capacitive crosstalk than to actual radiation. CM currents, then, will be found on the cable, by using a current probe (see Chap.13 “Troubleshooting”) even after I/O filters or ferrites have been installed, turning the cable into a secondary antenna. Such leakages in a “hot plate” area must be controlled very carefully.

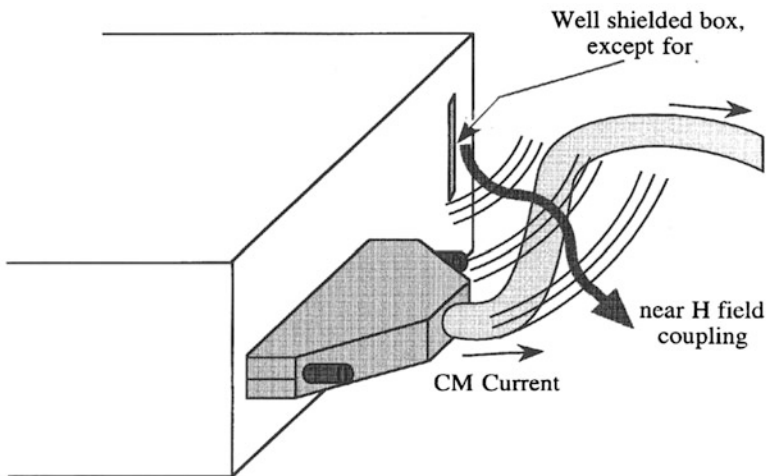


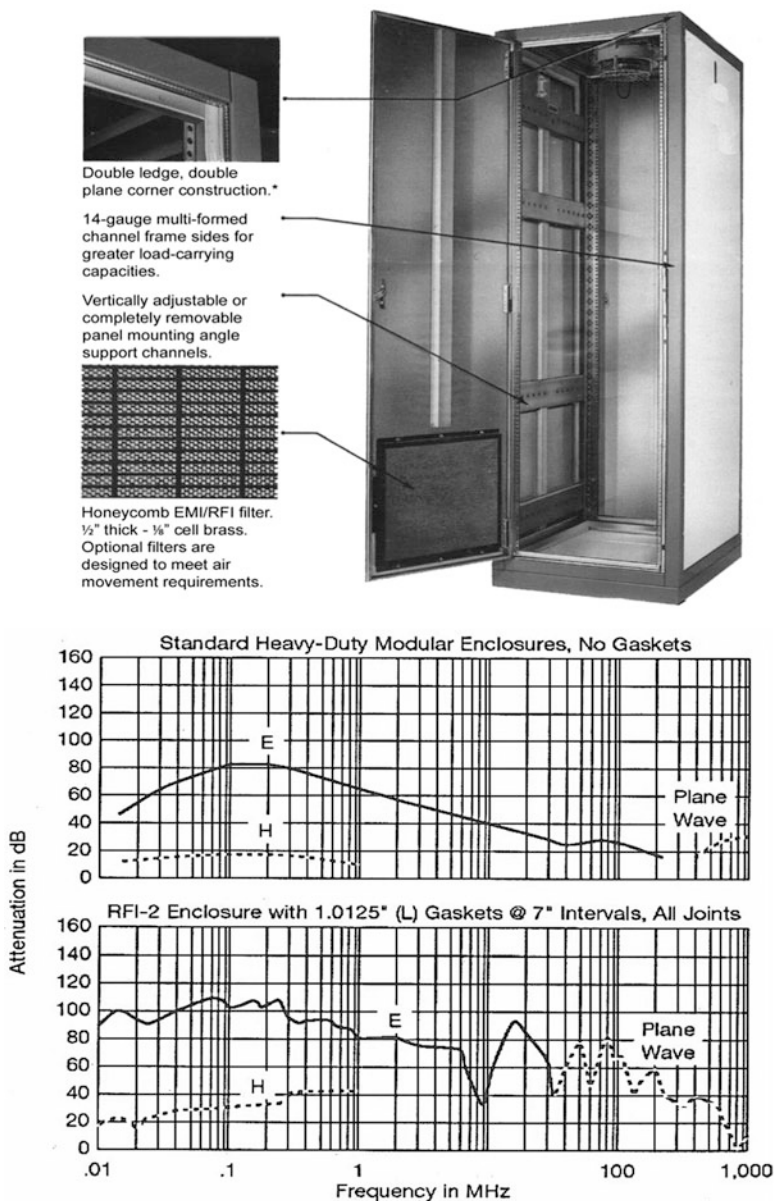
Fig. 10.24 Excitation of I/O cables by a nearby slot

## 10.7 SPECIALLY HARDENED EQUIPMENT HOUSINGS

Several vendors of ready-to-use racks and cabinets offer EMI-shielded versions of their products. Even a standard steel or aluminum cabinet with some simple precautions (paint-free and zinc- or tin-plated contact areas, metal-mesh air filters) provides some degree of shielding.

Equipped with EMI gaskets and shielded air vents, 100% welded frame joints, and piano-hinged doors for better seam tolerances, shielded cabinets offer valuable SE performance (Fig. 10.25), at a cost increase of \$350-\$500 (2009 prices) as

compared to the standard version. Be careful, however, when dealing with emission problems: many SE values reported on shielded cabinet specification sheets are measured by the MIL-STD-285 method, with a radiating source outside, at 30 cm from the doors. These values may not be applicable to a situation where the emitter is inside the cabinet. Proximity effects can cause lower than expected values for SE, especially when housed electronics and cables are near the cover seams.



**Fig. 10.25** Example of a commercially available shielded cabinet (source: Equipito, Aurora IL, USA)

Figure 10.26, taken from the author’s “real-cases story book,” illustrates this point. A telecommunication electronic system was exceeding FCC Class A limits. To understand what was happening, a preliminary *E*-field scan was plotted 360° around the frame with the original, ungrounded covers removed. Then, another plot was made, with each steel cover grounded at one point by its normal 12 cm round wire straps. The engineers expected, based on SE of 1.5 mm thick steel, a significant attenuation (theoretical figure being above 300 dB). To the engineer’s chagrin,

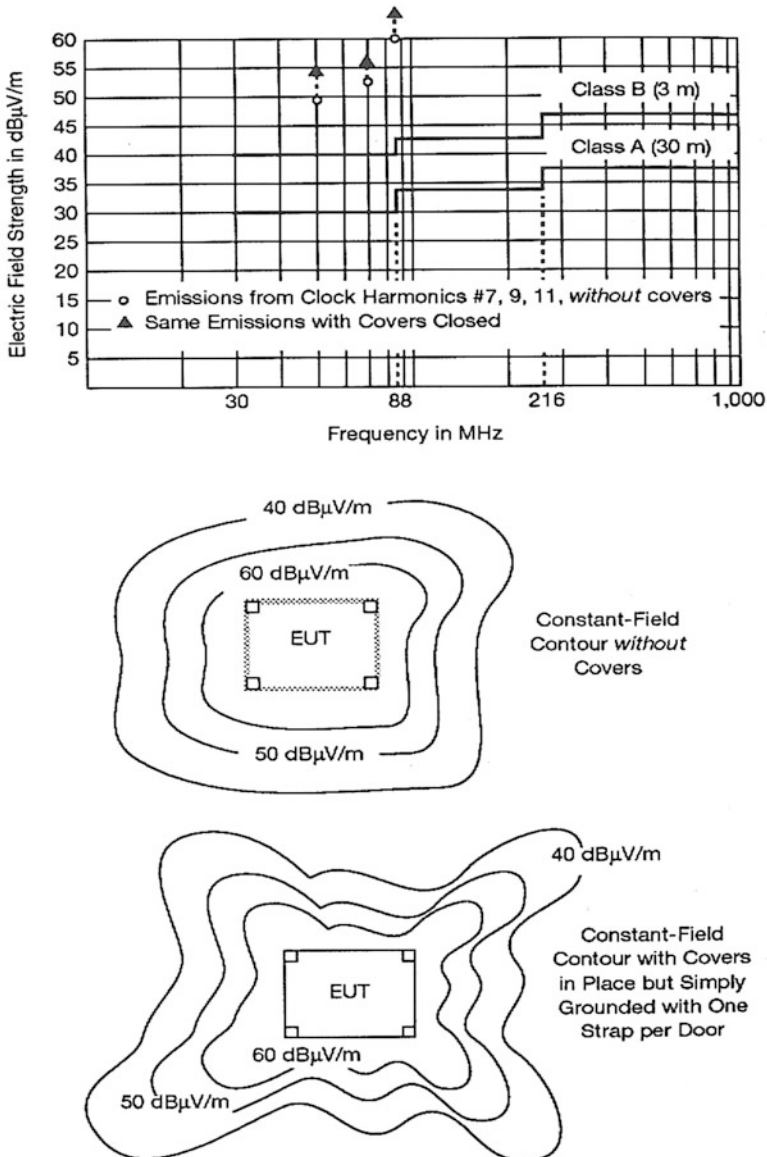


Fig. 10.26 Apparent increase in radiated field due to improper bonding of covers



cover’s attenuation seemed in fact negative: in some directions the metal-covered cabinet radiated 2-4 dB more than the open-sided case. The answer is that long, ungasketed slits (here about 1.75 m long) behave as radiating dipoles with directional gain in some specific angles. The total radiated power had not changed, but its spatial distribution had changed.

## 10.8 APPLICATION EXAMPLE: BOX DESIGN FOR A GIVEN SE OBJECTIVE

We will use, as a carry-on example, the metal box of Fig. 10.10, with aperture leakages as estimated in Example 10.1. The principal radiating source is assumed to be the motherboard/daughter cards assembly of Chap. 3, Example 3.2. The radiation profile of the 50 MHz clock harmonics is the same as shown in Chap. 3, Fig. 3.4 (FCC/Class B compliance).

1. Calculate the existing box SE. Compare the result to the design objective and decide where modifications are necessary.
2. Repeat exercise 1 with MIL-STD-461-RE102, as the specification limit.

In both cases, an approximately 6 dB margin is desired to cover manufacturing and installation variations.

**Solution** The general routine is:

1. Evaluate SE requirements.
2. Evaluate the SE of the box skin material as if it were a perfectly homogeneous barrier of 2 mm thick aluminum.
3. Evaluate SE for all apertures listed, per Example 10.1.
4. Retain the worst SE in each column; compare with SE requirements to decide if improvements are needed.

*Solutions for FCC Class B Compliance (Table 10.2, from example 3.2, Chap. 3)*

**Table 10.2** Summary sheet of SE needs for FCC example

<i>F</i> (MHz)	50	150	250	350	400	500	1,000
A. SE objective (dB) <sup>a</sup>	10	17	14	18	26	18	12
B. Metal SE (dB)	>300	>300	>300	>300	>300	>300	>3,00
C. Openings SE(dB) from Example 10.1							
Display	36	26	22	19	<b>18</b>	<b>16</b>	<b>10</b>
Cooling fan	26	17	<b>12</b>	<b>9</b>	<b>8</b>	<b>6</b>	<b>0</b>
Cover seams	34	25	20	<b>17</b>	<b>16</b>	<b>0</b>	<b>0</b>
Cooling slots	39	30	25	22	<b>21</b>	<b>19</b>	<b>3</b>
Open-ended slot	38	29	24	21	<b>20</b>	18	12
D. Overall SE (dB) <sup>b</sup>	<26	<17	<12	<9	<8	<0	<0
Improvement needed (A-D) (dB)	0	0	>2	>9	>18	>18	>18

<sup>a</sup>Specification violation plus 6 dB margin

<sup>b</sup>Worst figure of each individual SE

*Comments:*

- Instead of retaining the worst figure in each column, calculation of overall SE could be done more precisely [9] by combining the antilog of all *B*, *C*, and *D* leakages, assumed (worst case) in phase:

$$\text{SE (total)} = -20 \log \left[ 10^{-B/20} + 10^{-C1/20} + 10^{-C2/20}, \text{etc.} \right] \quad (10.9)$$

- For equipment with clock frequency <108 MHz, there is no FCC requirement above 1,000 MHz.
- Taking an average of 15 cm for center-to-sides distance, the box walls are at near field from inside sources up to a frequency such that  $0.15 \text{ m} > 48/F$ , i.e., 320 MHz. Therefore, Equ. (10.6) for proximity effects should apply. However, because the radiating circuit impedance is not very different from  $377\Omega$ , no correction has been applied.
- At any frequency, the aluminum SE is way above the requirements. Thus, the metal poses no problem.
- Figures appearing in bold in the table designate the items responsible for insufficient attenuation.
- The needed improvement (10-20 dB in the 150 to 500 MHz range) is rather modest. In fact, leaving the box as is, except for the cover seams where more screws could be added, the field reduction could be obtained by modifying the mother and daughter PCBs, at much less cost. The single-layer, two-sided PCB could be replaced by a 4-layer, with internal 0 V and  $V_{cc}$  planes, reducing the clock trace height by a five-times factor. Clock outputs could be filtered starting  $\approx 200$  MHz, at no prejudice for the signal integrity. For a more precise calculation, actual radiating circuit impedance should have been also taken into account for their impact on near-field wave impedance, resulting in an SE figure correction of -5 dB at 150 MHz, dropping progressively to 0 dB at 320 MHz.

If internal redesign is not feasible, the following changes are necessary:

1. Reduce cover seam lengths by doubling the number of screws. This would shift  $\lambda/2$  resonance up to 1,000 MHz, and SE at 500 MHz would become 20 dB.
2. Subdivide the cooling aperture in a  $10 \times 10$  mm grid. The SE at 500 MHz would become  $>26$  dB. A thin wire mesh is not necessary; this could be done via cutouts in the sheet metal, provided that only thin ribs are kept between.
3. Subdivide the display opening into three  $20 \times 20$  mm openings, leaving two thin metal ribs between. The SE at 500 MHz will become  $>26$  dB. Another option would be using a shielded window.
4. Replace the side-cut, open-ended slots with oval holes. This will reduce the edge radiation, offering an SE  $>30$  dB at 500 MHz.

**Solution for MIL-STD-461-RE102**

First, to evaluate SE requirements, the field envelope should be recalculated for 1 m distance and compared to RE102 limit (Table 10.3, “E(dB $\mu$ V/m) at 1 m”)

**Table 10.3** Summary sheet of SE needs for MIL-STD-461 RE102 example

<i>F</i> (MHz)	50	150	250	350	400	500	1,000
<i>E</i> (dB $\mu$ V/m) at 1 m	54	64	64	68	76	68	62
RE102 limit (dB $\mu$ V/m)	24	28	32	34	36	38	44
Off-specification by (dB)	30	36	32	34	40	30	18
New SE objective (incl. 6 dB margin)	36	42	38	40	46	36	24
SE (overall) as present (dB)	<26	<17	<12	<9	<8	0	0
Improvement needed (dB)	>10	>25	>26	>31	>38	>36	>24

We see that the new requirement demands more hardware changes for frequencies up to 1,000 MHz.<sup>3</sup> A fan hole grid should be employed, with 3 mm maximum spacing. The long cooling slots should be subdivided into shorter, 5 mm  $\times$  3 mm slots or, better yet, into an array of adjacent 3 mm diameter holes. The display window must be equipped with 3 mm maximum thin mesh or transparent conductive film. Cover screw spacing has to be reduced to 50 mm (or an EMI gasket installed).

## 10.9 SHIELDING COMPONENTS FOR MASS-PRODUCTION OF CONSUMER PRODUCTS

Since the late 1990s, the technical evolution has brought a huge number of miniature, popular devices using high-speed digital circuits and wireless RF techniques, operating at  $>1$  GHz. This has urged the development of new shielding hardware [3]. These shielding items have to be economical, lend themselves to mass production techniques (one single manufacturer of portable telephones reported in the year 2000 a production of 60,000 devices per day), and provide performances which were barely attainable by the expensive, sophisticated military electronics of the 1980s. Such shielding hardware includes:

- Heat-formable, shrinkable films.

They are generally polymer-fiber films coated with a metal mesh with low fusion point (like tin, for the 3M #6100) or a conductive ink grid (GE Lexan). When heated at 150-200 °C after die-cut, the film conforms itself to the 3D shape of the plastic housing that needs to be shielded. With total thickness of

<sup>3</sup> Although RE-102 limit extends up to 18 GHz, the table does not show calculations above 1,000 MHz. The reason is that starting  $\approx 400$  MHz, the radiated emission spectrum of our 50 MHz clocks falls-off with frequency, while at the same time the RE-102 limit increases with frequency, such as the SE needs drop to 0 dB around 2.5 GHz.

0.2-0.8 mm, foil resistance is in the range of 0.1-1  $\Omega$ /sq, and the textured nature of the metal content prevents high- $Q$  resonant cavity effects.

- Thin, form-in-place gaskets.

Conductive caulking can be applied in a regular cord gasket with diameter as small as 0.3-1 mm, acting both as EMI and weather gasket. They can be deposited with an automatic dispenser or printed in a single operation like an ink, conforming to very intricate shapes.

- PCB component shields (see Chap. 5)

Five-sided cans, stamped from tin-plated steel or brass, are available off-the-shelf in standard shapes, with heights as low as 3 mm. They can be wave soldered to a printed ground belt around the specific component, or PCB zone, that needs to be shielded. The PCB ground plane (0 V or mechanical ground) is acting as the sixth side of the enclosure.

## 10.10 SUMMARY OF RADIATION CONTROL VIA BOX SHIELDING

1. When the best affordable measures have been taken at PCB and internal wiring level, the equipment housing is the ultimate barrier against radiated emissions.
2. Until the last hole or slot is checked, the best metal box could appear to be useless as a shield.
3. For metal housings:
  - (a) Bond all metal parts (a floated item is a candidate for re-radiation).
  - (b) Avoid long seams and slots: a 30 cm seam is almost a total leak at 300 MHz (upper VHF range) and above.
  - (c) Use gaskets, or waveguide effect: design fold-over shapes for the cover edges.
4. For plastic housings:
  - (a) Use conductive coating  $\leq 2 \Omega$ /sq, then treat the box like a metal housing.
  - (b) Avoid long, protruding screws inside.
5. Preserve, or restore, shield integrity at:
  - (a) Cooling holes
  - (b) Viewing apertures
  - (c) Component holes
  - (d) Cable penetrations
6. Beware of noisy circuits or cables close to seams and slots: they degrade an otherwise sufficient SE.

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# Chapter 11

## Controlling Radiated Emissions at I/O Ports and External Cables

As soon as equipment is fitted with external cables whose length exceeds the largest box dimension, it is highly probable that these cables will be the largest contributors to radiated emissions, and susceptibility as well, at least up to several hundred megahertz. We have seen (Chap. 2, Sects. 2.4 and 2.5) that two types of excitation could drive these cables as radiating antennas:

1. Differential-mode (DM) excitation, where the currents are balanced (equal and opposite) in the wire pairs. Unless the outgoing and return carriers are spaced very far apart and untwisted, this mode is a minor contributor, though measurable.
2. Common-mode (CM) excitation, where the unbalanced portion of the current flows in the whole cable-to-ground loop. Due to the large size of the antenna, this mode largely overrides DM excitation.

Preventing unwanted RF emissions from radiating by the external cabling can be achieved by one or several of the following:

- EMI filtering of the I/O ports at the equipment interface
- Using balanced, differential outputs, isolated or not
- Using shielded cables (coaxial or multiconductors)
- Adding ferrite toroids on the entire cable

### 11.1 FILTERING OF INPUT/OUTPUT PORTS

Generally located at, or close to, the I/O interface of the equipment, the components that are needed for preventing external cables from carrying RF noise from inside out deserve special attention, even more so if the external cables are not shielded. The type and characteristics of these components are closely related to the nature of the I/O interface, data rate/functional bandwidth, galvanic isolation, unbalanced or balanced type, etc., as will be explained next.

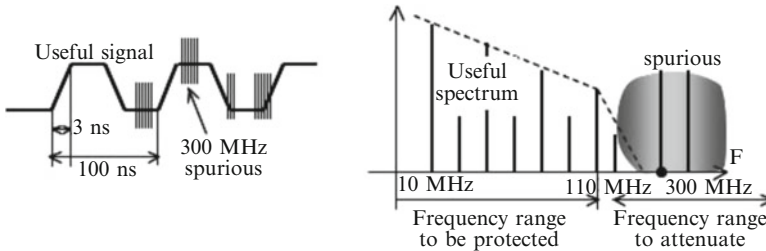
At this juncture, a quick brushup on EMI filtering, starting with a few basic aspects, is in order:

- What cutoff frequency of the low-pass filter can we use without degrading the wanted signal?
- What type of filter, C, L, (L + C), Pi, or T, should be selected?
- What are the component values that will match our needs, the latter being presumably known?

(Readers who are already familiar with these topics can skip to the next section.)

### 11.1.1 Determining the Cutoff Frequency of an EMI Filter for Digital Outputs

Having identified the need for a filter, we must determine its cutoff frequency. Filters that are needed for cleaning-up outgoing wires to prevent EMI emissions are of the low-pass type. They must not significantly distort the useful digital signal (Fig. 11.1). So, how much of the intentional signal spectrum can we sacrifice without endangering its integrity and as result the quality of the data acquisition?



**Fig. 11.1** Useful signal vs. undesirable noise spectra. It is assumed that the frequencies to be eliminated are sufficiently offset from the main, useful spectrum. This is not always the case

From Fourier analysis (see Chap. 3, Sect. 3.1) of a digital pulse, we know that beyond the second corner frequency,  $F_2 = 1/\pi t_r$ , the harmonic amplitudes start rolling off abruptly like  $1/F^2$  (-40 dB/decade). So, we can anticipate that soon after frequency  $F_2$ , the spectrum can be stripped of its remaining harmonics, with little prejudice to signal integrity, since they represent only few percent of the original pulse amplitude [5, 12]. More specifically, where on the frequency scale shall we decide that a filter can start attenuating? Table 11.1 shows that if we truncate totally the spectrum of a pulse train at Harmonic #5 and beyond, leaving only the fundamental and Harmonic #3, the signal suffers a severe distortion with a 15% peak error on the reconstituted waveform. But keeping Harmonics #1, 3, and 5 intact, and stripping everything beyond this, will leave a tolerable distortion (7% peak error). From now on, let us use a carry-on example.

**Table 11.1** Error when only the first “*n*” harmonics are kept (adapted from [12])

Assumption: 1 V pulse, 50% duty cycle,  $t_r, t_f = 10\%$  of period  $T$

Harmonics left	Error	
	(rms)	(Peak)
#1 (Fundamental only)	12%	28%
#2 N.A. (no even harmonics)		
#1 + 3	5.3%	15%
#1 + 3 + 5	2.2%	7%
#1 + 3 + 5 + 7	1%	3%

**Numerical Example 11.1**

Clock-pulse train, 50% duty cycle (no even harmonics)

Amplitude: 1 V

Frequency: 25 MHz (i.e. 50 Mb/s bit rate for the simplest NRZ string 1-0-1-0... etc.)

$t_r, t_f$ : 4 ns, that is,  $\approx 10\%$  of clock period  $T$

Assume that for an EMI compliance, a 15 dB attenuation is needed at 230 MHz and beyond.

The spectrum plot of Fig. 11.2 shows the second corner frequency  $F_2$  at 80 MHz, such that Harmonic #5, at 125 MHz is already in the -40 dB/dec roll-off region. Simple analysis [12] tells us that for maintaining a decent signal integrity, Harmonic #5 should not be reduced by more than 30% (i.e., -3 dB).

This criterion dictates that our filter cutoff frequency, or -3 dB point, must be no less than  $5 \times$  clock frequency. This rule corresponds also, in general, to  $F_{\text{cutoff}} = 0.5/t_r$  since an often-used rule of thumb is to have  $t_r, t_f \leq 0.1 T$ .

In our example we will choose a filter with  $F_{\text{co}} = 5 \times 25 \text{ MHz} = 125 \text{ MHz}$ , such as it will not significantly affect signal integrity. On Fig. 11.2, truncating the spectrum at 125 MHz and beyond slightly affects Harmonic #5, but does not



suppress it (This would leave us with only Harmonics #1 and 3, a serious deterioration). Figure 11.3 shows us to what extent Harmonic #5 and beyond are attenuated. For a first-order filter, attenuation for  $F/F_{co}$  is -3 dB, meaning that Harmonic #5 is keeping 70% of its original amplitude. Harmonic #7, at 1.4 times  $F_{co}$  will still be at 50% of its amplitude. Thus, choosing the filter cutoff at  $0.5/t_r$ , or 125 MHz, will not distort significantly the original signal.

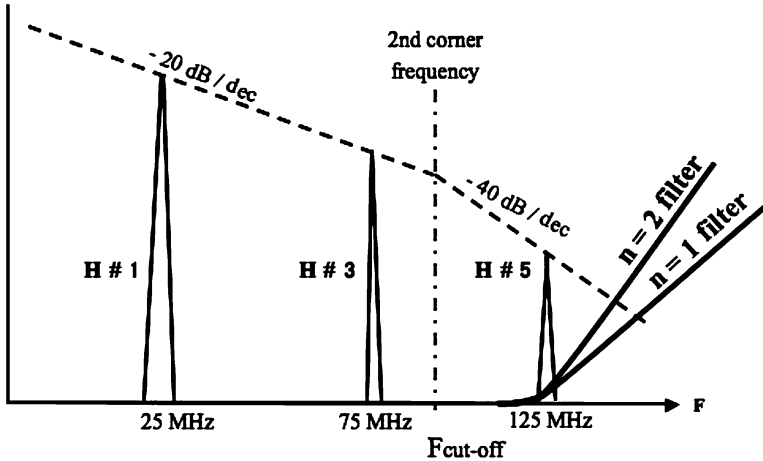


Fig. 11.2 Spectrum of the 25 MHz pulse train of Example 11.1

### 11.1.2 Determining the Proper EMI Filter Order

Once the cutoff frequency has been found, we must check what filter order will meet our need, by continuing the carry-on numerical example.

**Carry-On Numerical Example 11.2** For the 25 MHz signal, 15 dB attenuation is desired at 230 MHz and beyond. Figure 11.3 shows that for a ratio  $F/F_{co}$  of 230/125, or 1.85, the attenuations are:

- First order ( $n = 1$ ): 6.5 dB
- Second order ( $n = 2$ ): 11 dB
- Third order ( $n = 3$ ): 16 dB

Therefore, we must select a  $\pi$  or a T filter. Choosing a one-element filter (for instance, a single capacitor) for a 15 dB loss at 230 MHz would require an  $F/F_{co}$  ratio of 6, hence a cutoff at 38 MHz: even the Harmonic #3 amplitude would be affected. A second-order filter could eventually be used, but at the expense of downshifting the  $F_{co}$  to 100 MHz causing 5 dB deterioration of Harmonic #5. This could be done if some edge rounding and distortion of the signal (about 10% ripple on the flat portion) was tolerable. Interestingly, we remark (Fig. 11.3) the magic of the  $F_{co}$  point: whatever the filter order (1, 2, 3), the attenuation at is always 3 dB.

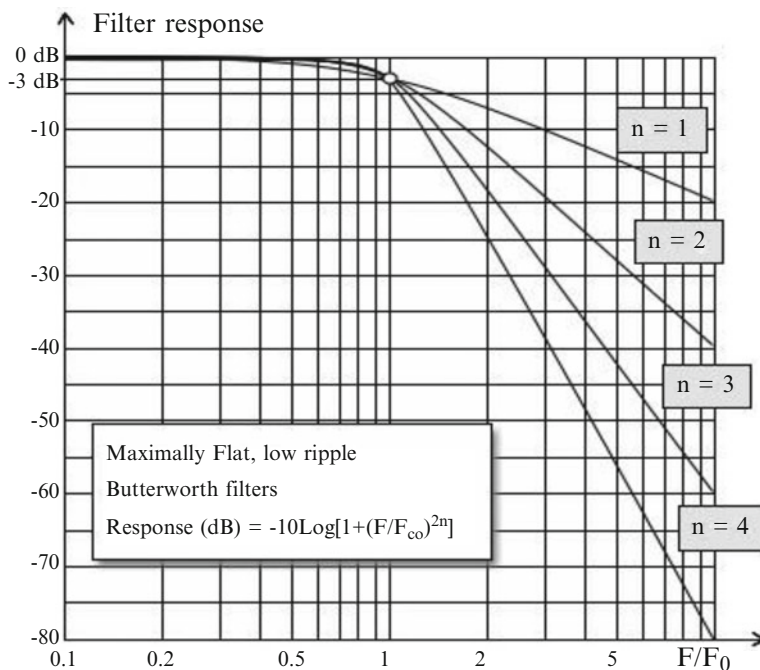


Fig. 11.3 Attenuation for low-pass filters vs.  $F/F_{co}$ . All filters are Butterworth type

### 11.1.3 Determining the Proper EMI Filter Type

Knowing the desired attenuation, cutoff frequency, and number of elements, the last step is to determine the optimum schematic and component values, whether the filter is homemade, custom ordered, or commercially available. Table 11.2 gives basic guidance for filter selection. A simple, elementary rule states that *in a filter, capacitors must look toward high impedances, both sides, and inductors must look at low impedances, both sides*. The designations “low” and “high” for EMI source and load on this table are somewhat arbitrary. However, considering the necessary trade-offs between size, weight, and cost of discrete components plus the recommended criteria of having  $\sqrt{L/C}$  roughly equal to circuit impedance, the high/low grey area can be taken as 100  $\Omega$ . If the I/O port to be filtered is looking at an electrically long line ( $\ell > \lambda/4$ ), load impedance has to be regarded as the cable characteristic impedance  $Z_c$ .

**Continuing Example 11.3** Let us assume that for our application, the interface circuit to be filtered has the following characteristics:

$$Z_{gs} = 30 \Omega, \quad Z_L = 120 \Omega$$

Given that source impedance is  $<100 \Omega$ , a Pi filter is not the best choice, violating our elementary rule (*capacitors must look toward high impedances, both sides*). For an  $F_{co}$  of 125 MHz, our filter capacitor value should be about 80 pF, causing a substantial loading for the 1 V/4 ns rise of our digital pulses. A “T” filter with inductances or ferrites upfront is a better option. Values for the  $L/C$  components can be found using components manufacturer’s software, or SPICE modeling. For this example, with an asymmetrical source/load configuration, the perfect T filter should have different inductances values for each side. Since this is usually not practical, a compromise filter would be selected with the following trade-off values:

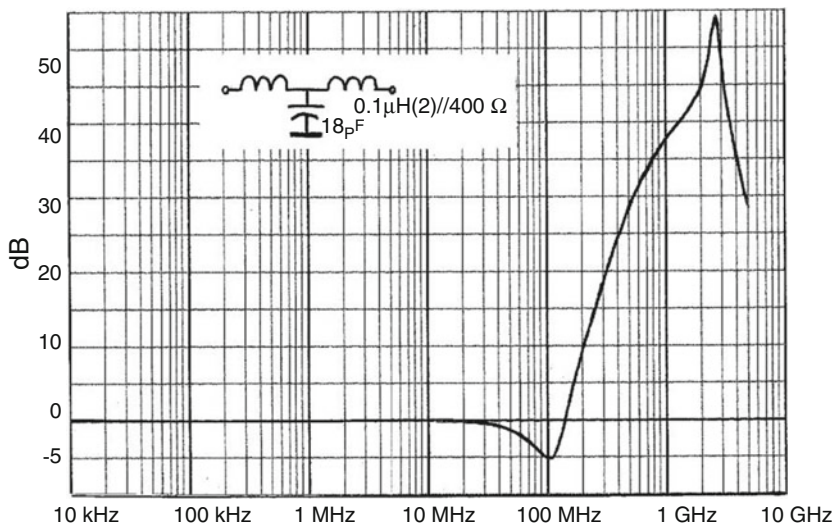
$$L_1, L_2 = 100 \text{ nH, with a ferrite resistive term } \geq 300 \Omega \text{ at } 230 \text{ MHz}$$

$$C = 66 \text{ pF}$$

Figure 11.4 shows an example of attenuation of a custom-made filter, calculated then validated on an actual equipment. The performance differs of what a manufacturer’s data sheet would have given, in the typical 50/50  $\Omega$  arrangement of a standard filter measurement method (MIL-STD-220A).

**Table 11.2** Decision table for EMI filter-type selection

EMI source impedance ( $Z_s$ )	Proper filter scheme	Load impedance Replace by line charact. Impedance if cable length $\geq \lambda/4$
Low		Low condition = $L_\omega > Z_s + Z_L$
Low (for high $\rightarrow$ low condition, reverse filter scheme)		High
High		High condition = $(1/C_\omega) < Z_s, Z_L$



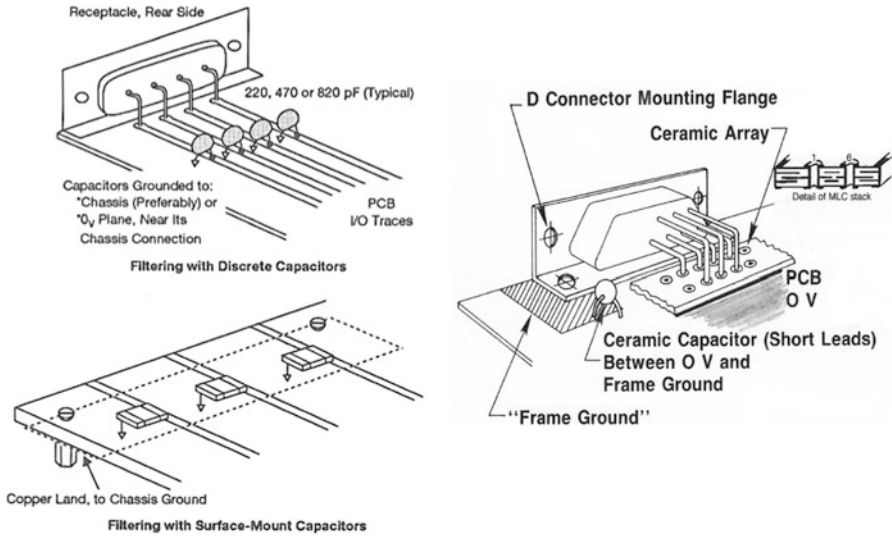
**Fig. 11.4** Example of attenuation for a custom-tailored EMI “T” filter, for fast signals application. Source side:  $30\ \Omega + 4\text{ cm PCB trace}$ ; load side:  $90\ \Omega$  impedance line +  $300\ \Omega$  termination

## 11.1.4 First-Order ( $n = 1$ ) Filtering

### 11.1.4.1 Capacitive Filtering

Looking at the filtering toolbox, capacitors are the lightest, smallest, and least expensive components. If one-pole filtering (20 dB/decade) is deemed sufficient, simple ceramic capacitors of HF quality (generally ceramic) are recommended. Printed circuit board permits economical and efficient mounting of filter elements. Furthermore, SMT packages allow for economical and low-inductance mounting. Since the aim is to reduce CM emissions leaking out by the external cables, the preferred method is to have these capacitors connected to a “chassis-ground” copper land on the PCB edge. If this has not been provided, the capacitors can be connected to the 0 V plane which in turn will be connected to chassis, nearest to the I/O ports (Fig. 11.5).

As already seen in Chap. 6 (PCBs, Sect. 6.3, decoupling), a major problem of EMI filtering with discrete capacitors, especially above 30 MHz, is their unavoidable parasitic inductance. The only component that realizes an ideal capacitor, eliminating totally the parasitic inductance, is the feedthrough coaxial filter of Fig. 11.6. Since it does not lend itself easily to mass-production PCB mounting, some manufacturers have developed an SMT equivalent of the feedthrough, called the 3-terminal capacitor or “semi-feedthrough.” In SMT size #1206, it has a parasitic inductance of only 0.1 nH and allows the signal line to physically jump over the perpendicular ground bus (Fig. 11.7).



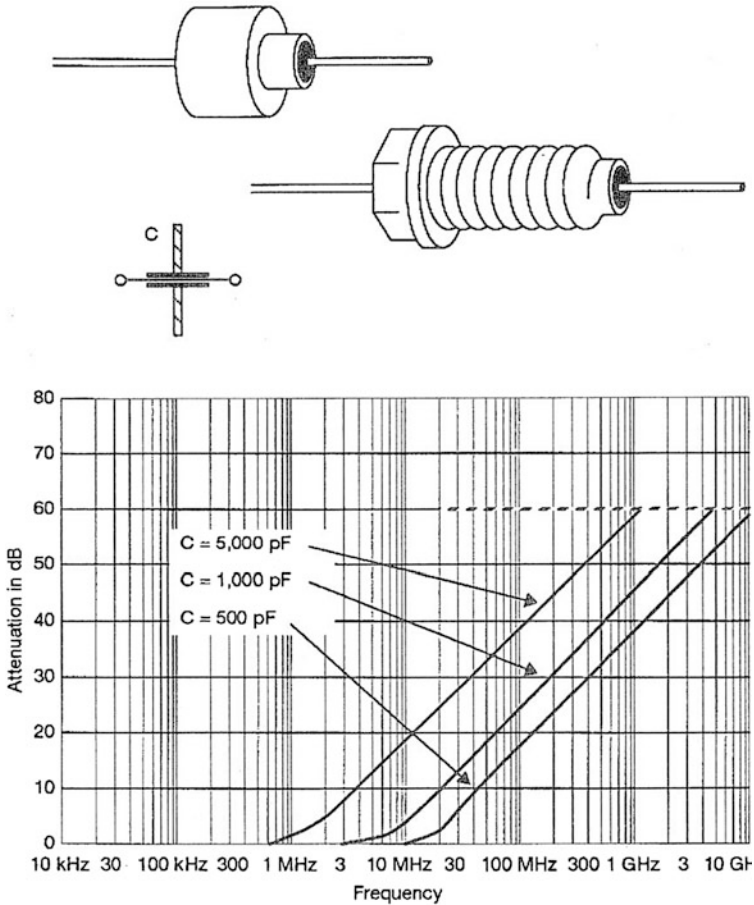
**Fig. 11.5** *Top*: filtering at PCB edge with multilayer ceramic array. It can use standard connector receptacle footprint, or be part of the connector itself. *Bottom*: simple methods of capacitive I/O filtering at the PCB edge

Trying to clean up PCB traces of some undesired HF contents, one should be careful if relying solely on capacitive filtering. A single capacitor across an output trace will shunt the HF current back to its source, returning through the PCB ground network. This will reduce the HF contents escaping to the driven line, but may increase the PCB common-mode ground noise, in a same proportion. The whole attempt may be a frustrating experience since a noisier PCB ground will drive more CM current into the external cabling.

Figure 11.8 shows two classical, treacherous pitfalls of this sort:

In Fig. 11.8a a 200 pF bypass capacitor has been installed at the I/O interface to slow the edges from the original driver output. But return segment B-G, far from being a perfect ground, is a heavily slotted plane, or a set of ground traces, with a total inductance of 10 nH, i.e.,  $10 \Omega @ 150 \text{ MHz}$ . Therefore, capacitor C plays as an exciting source to segment B-G, with point B raising at a fraction of total output  $V_{A-G}$ . Ground noise  $V_{B-G}$  becomes a CM driving voltage for the I/O cable, and eventually *for the entire system*, since it can now feed other cables, including the power cord. Things go from bad to worse if several parallel outputs are filtered, because return currents now accumulate along the same ground impedance B-G.

In Fig. 11.8b the capacitor has been chosen to prevent the I/O trace and the external pair from being polluted by the crosstalk from a nearby clock trace. Let us assume  $V_{A-B} = 100 \text{ mV} @ 150 \text{ MHz}$ , such as the Xtalk coupling impedance to the

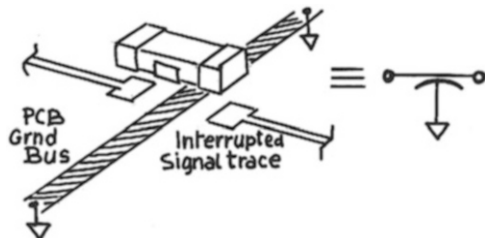


Note: Graph shows typical attenuation in a 50 Ω/50 Ω configuration. For other impedances, correct the curve data using the following expression:

$$20 \log \left[ \frac{R_L R_g}{25(R_L + R_g)} \right]$$

Fig. 11.6 Real feedthrough capacitive filters

Fig. 11.7 SMT, 3-terminal, semi-feedthrough capacitive filters, approaching the feedthrough concept



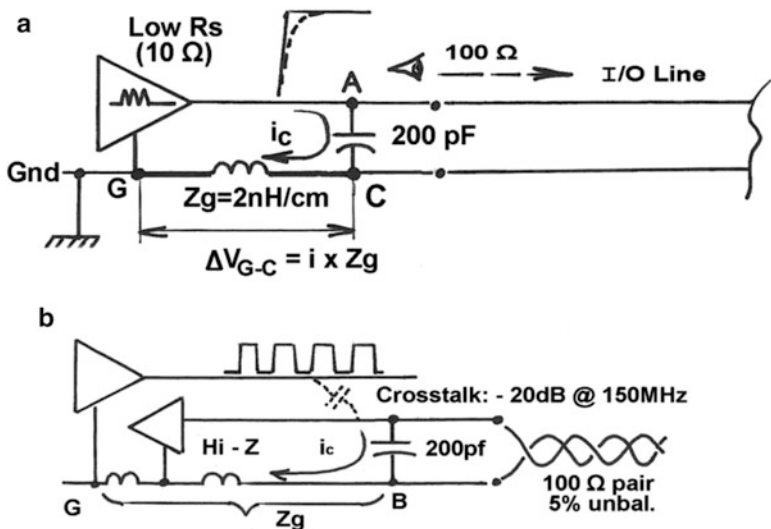
100 Ω load behaves as a 1 mA current source. Without any filtering, since the external link is balanced to 5%,  $V_{A-B}$  is injecting a CM current equal to

$$I_{cm} = 5\% \times (100 \text{ mV}/100 \text{ } \Omega) = 0.05 \text{ mA or } 50 \text{ } \mu\text{A}$$

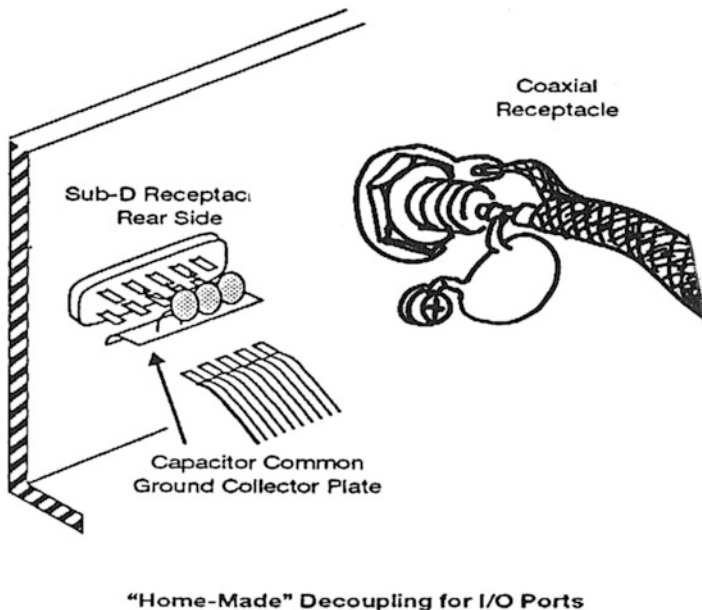
This is 16 times more than our 3 μA (10 dBμA) criteria for not exceeding FCC Class B (Chap. 4, Sect. 4.3). When the 200 pF bypass is added, it represents 5 Ω @ 150 MHz, thus reducing  $V_{A-B}$  by 20 times, which is about what we needed. But the entire 1 mA current is now sinking through the ground segment B-G. With the same 10 nH ground inductance representing 10 Ω @ 150 MHz, we now have  $\Delta V_{B-G} = 10 \text{ } \Omega \times 1 \text{ mA} = 10 \text{ mV}$ . Taking an average CM characteristic impedance of 250 Ω for the external cable (see Chap. 2, Sects. 2.5.1 and 2.5.2), this is causing a 40 μA external current, still ten times more than our criteria!

In both cases, by using brute force capacitive bypass, we have traded one mode of external cable excitation for another, with no or little benefit. Of course, increasing the capacitor value would bring nothing, eventually exacerbating the problem. So, as attractive and inexpensive as they are on PCBs, capacitor-based filters should be used only when:

- A good, low-impedance ground plane exists between the HF source and the I/O interface area or, at least
- The PCB ground is tied to a metal chassis plate very close (within centimeters) to the I/O filtering point (Fig. 11.9).



**Fig. 11.8** Some pitfalls with capacitive-only filters. Ground impedance noise  $V_{B-G}$  is acting as a CM drive for the external cable. The problem gets even worse in (A) if the filtered output is a parallel bus with 4, 8 lines, etc., adding as many times the currents  $i_c$ .  $V_{B-G} = \sum i_c \times Z_g$ . (a) Filtering capacitor for risetime stretching. (b) Filtering capacitor for Xtalk reduction



**Fig. 11.9** Quick-fix “homemade” decoupling of I/O connectors using discrete capacitors (not recommended for use above 30 MHz)

Like for any filter characteristics, single-capacitor filter values should be calculated at least crudely and not picked up by chance, as is too often the practice. The formula giving the insertion loss<sup>1</sup> of a  $n = 1$  capacitive filter is

$$\text{Insertion loss (I.L.)} = 20 \log \left[ 1 + \left( \omega C R_s R_L / (R_s + R_L) \right) \right]$$

The following steps are recommended:

1. Identify the total resistance (or impedance) across the line to be filtered by taking  $R_{\text{source}}$  and  $R_{\text{load}}$  in parallel. If the line is electrically long, replace  $R_L$  by  $Z_0$ , the characteristic impedance of the line. For example, for  $R_s$  (driver) = 50  $\Omega$  and  $R_L$  (receiver input) = 500  $\Omega$ , take total resistance  $R_T = 45 \Omega$ .
2. Identify the highest useful signal bandwidth or the maximum acceptable rise time  $t_r$ .

<sup>1</sup>Insertion loss has a slightly different meaning than attenuation. It is the ratio of across-the-load voltages before and after inserting the filter. As such, it gives a more realistic figure of merit for the filter.



3. On a balanced (or simply isolated) output, the maximum tolerable value of each line-to-chassis capacitor, for no visible signal distortion, is given by the condition:

$$1/(2\pi F_{\max}C/2) \geq 3R_T \quad (11.1)$$

This can translate simply as

$$C_{\max} = 100/(F_{\max}R_T) \quad (11.2)$$

for  $C$  in nanofarads and  $F$  in megahertz.

For instance, if the bandwidth to process is 3 MHz, for a  $R_T = 45 \Omega$  calculated previously:

$$C_{\max} = 100/(45 \times 3) = 0.7 \text{ nF}$$

4. If, instead of frequency, the rise (or fall) time of the useful signal is known:

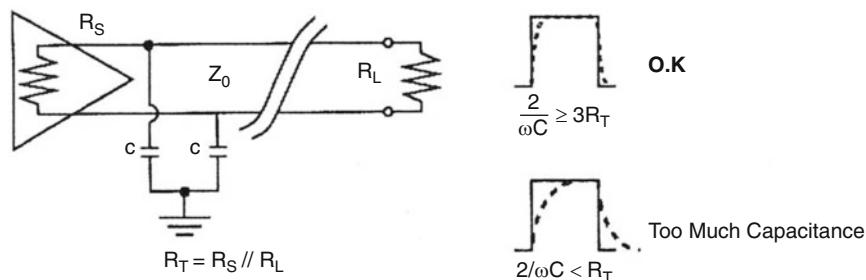
$$C_{\max} = 0.3t_r/R_T \quad (11.2a)$$

where  $C$  in nanofarads for  $t_r$  in nanoseconds  
or  $C$  in picofarads for  $t_r$  in picoseconds.

For instance, if the typical rise time is 100 ns in our 45  $\Omega$  example, applying Equ. (11.2a):

$$C_{\max} = 0.3 \times 100/45 = 0.7 \text{ nF}$$

5. If a slight degradation of the rise time (stretching or corner rounding) is tolerable, up to three times the calculated  $C_{\max}$ , corresponding to the 3 dB point in the attenuation curve, can be used (Fig. 11.10). In most practical cases, the value calculated by Eqs. (11.2) or (11.2a) can be easily rounded up to the next standard value. In our example, 680 or 750 pF is adequate.
6. If the EMI frequency is too close to the cutoff frequency, a one-pole filter will not be sufficient. Use a two- or three-pole (T, Pi) filter instead.
7. Check the capacitor service voltage and surge withstanding voltage against the application.
8. Select a capacitor family with tight tolerances. Large tolerances (such as -0/+50%) would not hurt for ordinary decoupling but could introduce line unbalance in differential links. Prefer NPO ceramic grade, for precision and stability.
9. Install the capacitors with the shortest leads possible, trimmed close to the capacitor body; prefer SMT components.
10. Check that the frequency interval to be attenuated is not significantly within the parasitic (inductive) region of the capacitor.
11. Make sure that all I/O lines have been decoupled in the same zone. One single line left unfiltered can corrupt the others (see Chap. 9, Fig. 9.7).



	Slow interface (typ.)	CMOS	TTL	HC/AC, fast LVDS
Rise time $t_r$	0.5 - 1 $\mu$ s	50 - 100 ns	10 ns	3.5 - 0.5 ns
Bandwidth	350 kHz	3.5 MHz	3.5 MHz	100 - 700 MHz
$Z^*$	120 $\Omega$	3-500 $\Omega$	100 $\Omega$	50 $\Omega$
$C_{max, good}$ pulse integrity	2200 pF	150 pF	30 pF	22-5 pF
$C_{max, marginal}$ pulse shape	6800 pF	430 pF	100 pF	68-15 pF

$Z^*$ : differential impedance =  $R_{load} // R_{source}$ , or  $R_{load} // Z_0$

**Fig. 11.10** Maximum tolerable values for common-mode filtering of differential (or floating) output

**Example 11.4: Filter Selection** An isolated output on a balanced pair is using 20 ns rise times. Source internal resistance (during switching) is 50  $\Omega$ , driving an electrically long external line with 120  $\Omega$  characteristic impedance. Conducted tests on the prototype (or EMI analysis) have found excessive CM current on an I/O cable in the 50 to 70 MHz region, with an excess of 24 dB above the desired objective. Determine the optimal filter.

**Solution** Equivalent bandwidth for 20 ns rise time:  $F_2 = 1/\pi t_r = 16$  MHz.

The total impedance for 120  $\Omega$ //with 50  $\Omega$  is 35  $\Omega$ . Attempting a single capacitive filtering, we find per Equ. (11.3) for each capacitor (each line to chassis ground):

$$C_{max} = 0.3 \times 20 \text{ ns} / 35 \text{ } \Omega = 0.170 \text{ nF}$$

At the 50 MHz EMI frequency, each 170 pF represents 20  $\Omega$  of impedance to ground, i.e., only about half of  $R_T$ . So the attenuation will be barely 6 dB, compared to the 24 dB objective. A multiple-element filter will be needed. Choosing its cutoff frequency at 25% above the useful bandwidth gives

$$F_{co} = 1.25 \times 16 \text{ MHz} = 20 \text{ MHz}$$

Thus,  $F_{EMI}/F_{co} < 50/20 = 2.5$

Looking at Fig. 11.3, we find that for  $F_{EMI}/F_{co} = 2.5$ , 24 dB require a three-stage, 60 dB/decade filter.

### 11.1.4.2 Inductor-Only (or Ferrite) First-Order Filtering

Per Table 11.1, we know that an inductive-only ( $n = 1$ ) filter is only appropriate for low source and load impedance  $\leq 100 \Omega$  both sides. Since this is seldom the case with digital signal ports and given that no wire-wound inductor remains an inductance above few tens of megahertz, this application is restricted to the filtering of DC or remote control lines, where the slow signal is not affected by series impedance at high frequency. Suitable devices are available in styles ranging from large toroids down to miniature multiline DIP or SMT ferrites chokes. The most appropriate for teaming with capacitors are the miniature ferrites, which are widely applied in multistage filters.

Another way of blocking CM currents on wire pairs consists of using longitudinal CM chokes (sometimes improperly called “baluns”). Operating by mutual inductance, they do not affect the useful signal and can be regarded as selective elements against CM current only. They will be described in a further section as “longitudinal transformers.”

## 11.1.5 Multi-element Filters Applications

For more attenuation, or a steeper attenuation slope, decoupling capacitors are complemented by discrete or SMT ferrites to form L, T, or Pi filters. With L/C filters, the ferrite should always be looking toward the low-impedance side (generally the source) and the capacitor toward the high-impedance (generally the load) (Figs. 11.11 and 11.12). Ferrite beads encapsulated with ceramic capacitor, forming a three-lead “T” filter, are commonly available from several vendors (Fig. 11.13). Careful mounting is necessary to avoid:

- Performance degradation above 30-100 MHz
- Serious line mismatch if output signal speeds require transmission line treatment

**Example 11.5: Filter Selection** In the previous Example, we had a case where a first-order, capacitive filter with 20 MHz cutoff frequency was not sufficient for the specified 24 dB at 50 MHz.

Given that  $F_{emi}/F_{co} = 50/20 = 2.5$ , by calculation with filters formula in Fig. 11.3, or from associated curves, we find for a  $n = 3$  filter:

$$A \text{ (dB)} = 10 \log \left[ 1 + (F_{emi}/F_{co})^{2n} \right] = 24 \text{ dB}$$

A two-stage, 40 dB/decade filter would have provided only 16 dB, not enough for our needs. Also, the capacitors value cannot be increased because of the signal rise time constraint.

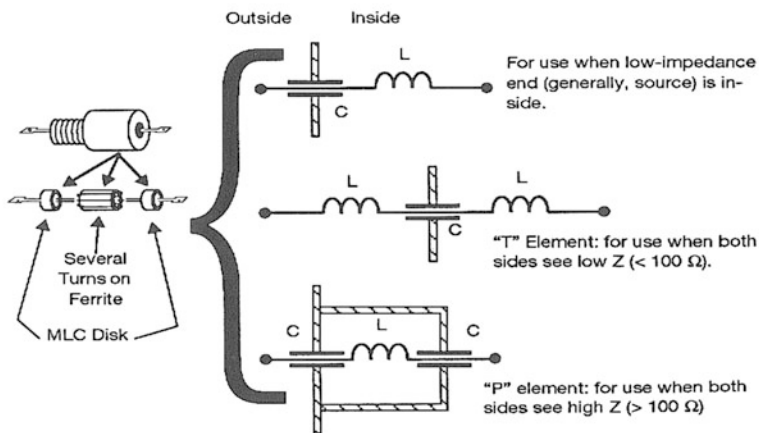
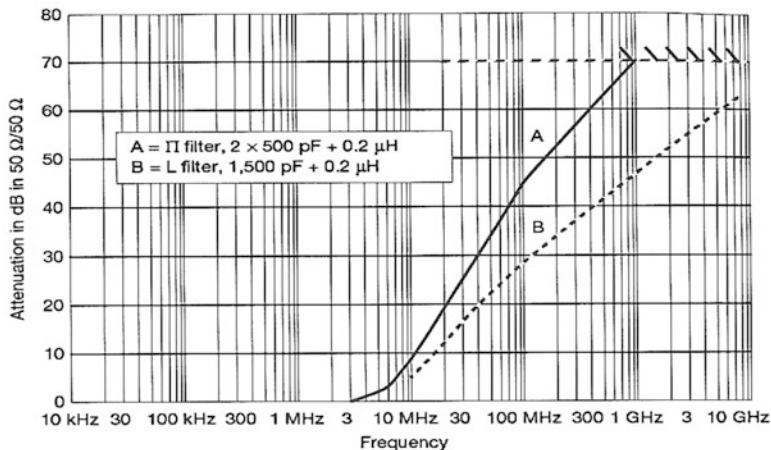
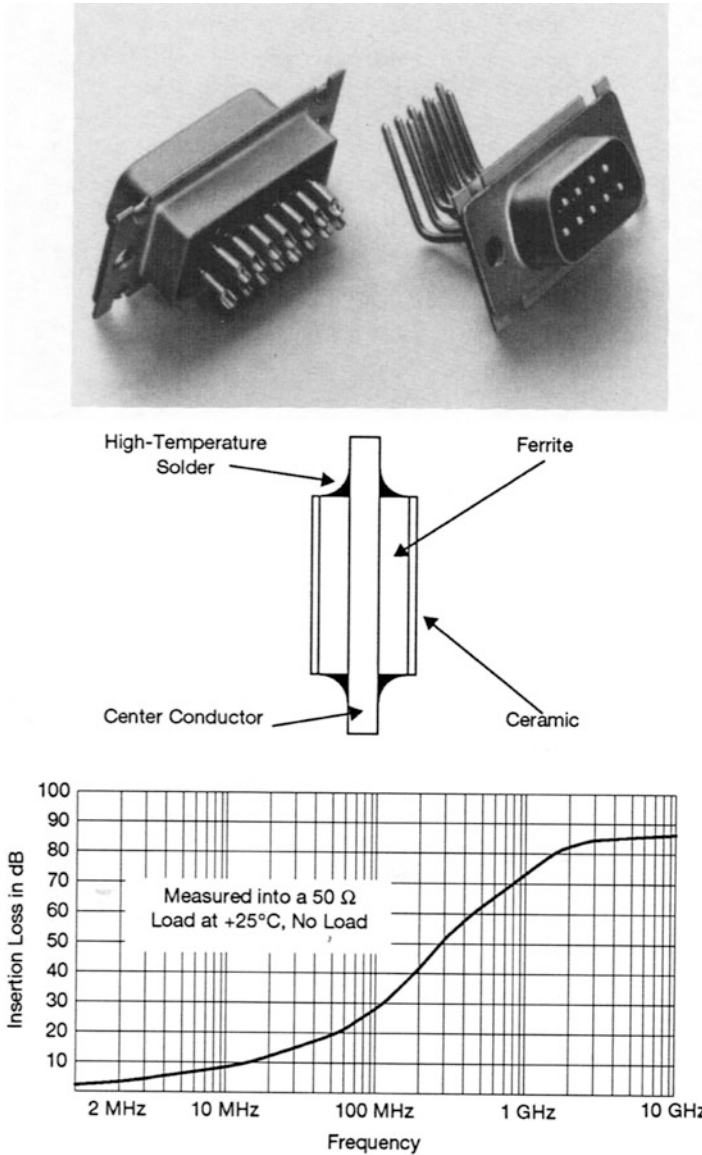


Fig. 11.11 Two- and three-stage feedthrough filters, for low-current signal leads

### 11.1.6 Avoiding the Most Frequent Pitfalls with Multi-element Filters

Pi filters, although a legitimate choice for high source and load impedances, can suffer from a common problem if not carefully mounted. On Fig. 11.14 (top), we see that if the capacitors are not directly grounded via a “quasi-zero” inductance connection, their common ground lead (Y shaped on the figure) will prevent a perfect sink of the capacitive currents to ground. As frequency increases, RF impedances of  $C_1$ ,  $C_2$  are decreasing, while at the same time the impedance of their common ground leg is increasing. Above a certain frequency, the two capacitors will bypass the filter inductance, making both the capacitors and the inductor



**Fig. 11.12** Example of a commercial Pi-filtered connector (1,200 pF contacts, Spectrum Control/ Apitech)

useless. The problem can turn into a maddening affair when someone tries to improve the filtering by changing to higher capacitor values, or more inductance, or both, which immediately makes things worse since the  $L/C$  pair resonance frequency will shift to lower values. This is a frequent case with PCB-mounted,

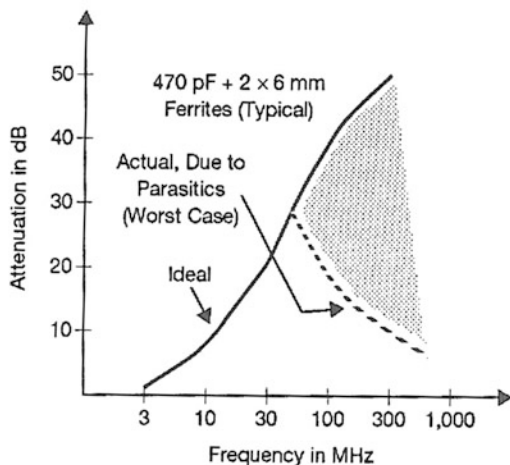
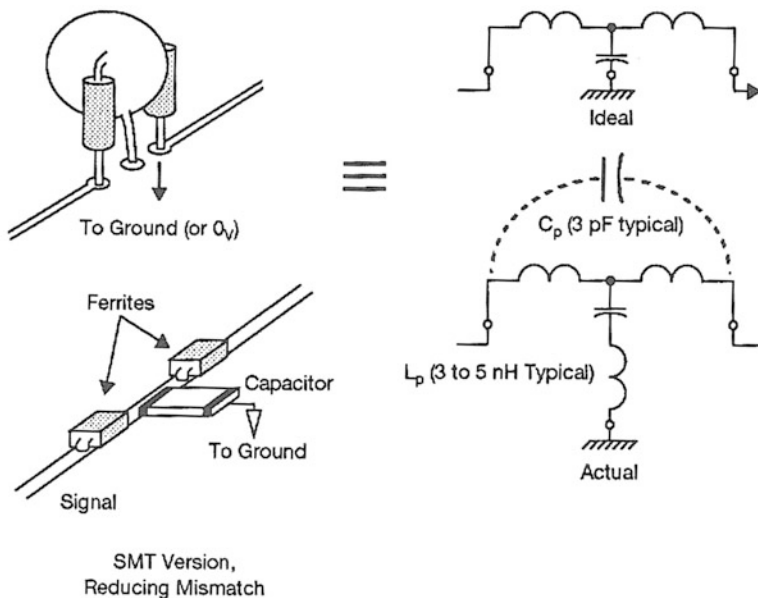


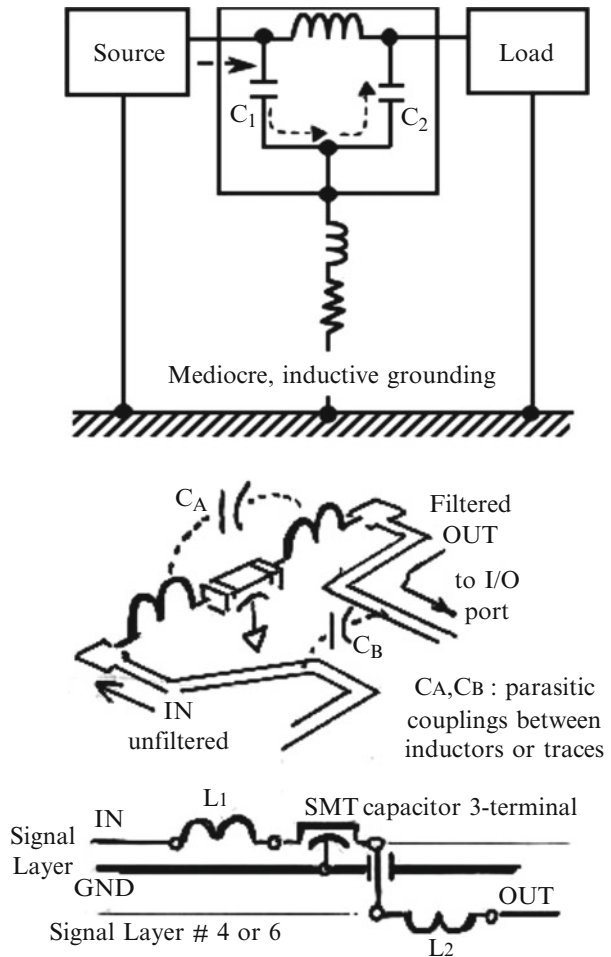
Fig. 11.13 “T” filters for PCB mounting

Pi-filtered receptacles. In this case, one must make sure that the metallic connector housing, that is, the capacitor common, is positively grounded to the chassis (or, by default, to the PCB ground plane). The author has seen occasions where a filter connector housing was simply riveted to the epoxy glass board, with no contact to ground. Not only was the filter useless (as quickly discovered by the technician),

but the filter capacitors floating common ground created crosstalk between the different lines.

Also in Fig. 11.14 (bottom), another stumbling block is shown with T filters: input-to-output capacitive coupling. This can result from coupling between traces or between the input and output inductances. If these latter ones are wire-wound ferrites, the input-to-output coupling can be strong enough to ruin the filter efficiency above a few tens of megahertz. High-attenuation T filters with theoretical 60 or 80 dB attenuation are easily spoiled by a -40 dB input-to-output Xtalk. To avoid this:

- Never run a filtered output trace close to an unfiltered input.
- A drastic solution with homemade T filters is to change side by a through via, putting the second inductance on the opposite face, with the 0 V plane acting as a Faraday shield (see Fig. 11.14, bottom).



**Fig. 11.14** Frequent pitfalls with filters mounting on PCBs

### 11.1.7 Special CM Filters for High-Speed Differential Links

Ever-increasing data rates have reached the upper hundreds of megahertz range, with some differential interfaces operating at 5 Gb/s on short hauls. With respect to signal integrity and EMI radiation from cables, such super fast rates on copper supports are imposing serious constraints, some becoming contradictory:

- Impedance matching, driver-to-line and line-to-receiver, including the connectors, is a crucial element (also see the in next section the problems of DM-to-CM conversion due to skewed edges).
- EMI filters must not cause signal distortion or deteriorate the symmetry vs. ground.
- EMI filter should be literally transparent within the equivalent bit bandwidth, yet jump to a high attenuation half-decade above.
- Not only the filter's common-mode capacitors are restricted to very low values, but their tolerances must be extremely tight.
- Most of the filtering action falls on the magnetic components of the filter, with symmetry requirements on the bifilar windings of CM inductors.

The following example will give a feel for the difficult challenge of CM filtering for a high-speed bus.

**Numerical Example 11.6** For a fast 1.25 Gb differential bus (IEEE 1394), what is the maximum tolerable value for filtering capacitors, line-to-ground? Rise/fall time for this interface is 0.28 ns (typical), and line impedance is 100  $\Omega$ .

Overall symmetry of the bus, including driver output and wire pair (UTP) unbalance, is  $\leq 5\%$ .

Using our criteria of Equ. (11.3) for differential output, we find:

$$\begin{aligned} C_{\max} &= 0.3 t_r / R_T, \text{ for } C \text{ in nF and } t_r \text{ in ns} \\ &= 0.3 \times 0.28 / 100 = 0.84 \cdot 10^{-3} \text{ nF} = 0.84 \text{ pF} \end{aligned}$$

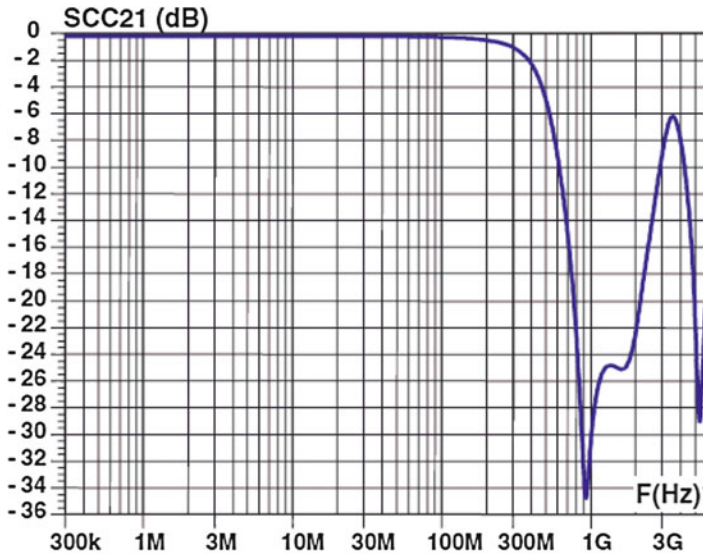
These capacitors must be matched to better than 5% tolerances. Such low values, with such tight tolerances, are almost impossible to get as discrete components in the industrial trade, where  $\pm 10$  or 25% tolerances are more the rule. So they are generally fabricated by pairs, with the same diffusion techniques as ICs.

Some manufacturers (Fig. 11.15 and [10]) are integrating transient voltage suppressors for ESD protection in the filter package, as such the capacitors are actually provided by the junction capacitance of the TVS, whose dimensional characteristics can be precisely controlled. By teaming these capacitances with 100-200  $\Omega$  of CM ferrite impedance at 100 MHz, a good filtering of CM emission is obtained above 100 MHz, at no or minimum prejudice to the differential signal. For this differential loss in the ferrite to be minimum within the useful bandwidth, the DM part in the impedance curve (Fig. 11.16) must also be minimum. For instance, keeping this DM series impedance  $< 5 \Omega$ , for a 100  $\Omega$  CM impedance, can guarantee a dissymmetry  $< 5\%$ . This implies that the balancing of the two windings in the bifilar choke be precisely controlled. The attenuation of such filters,

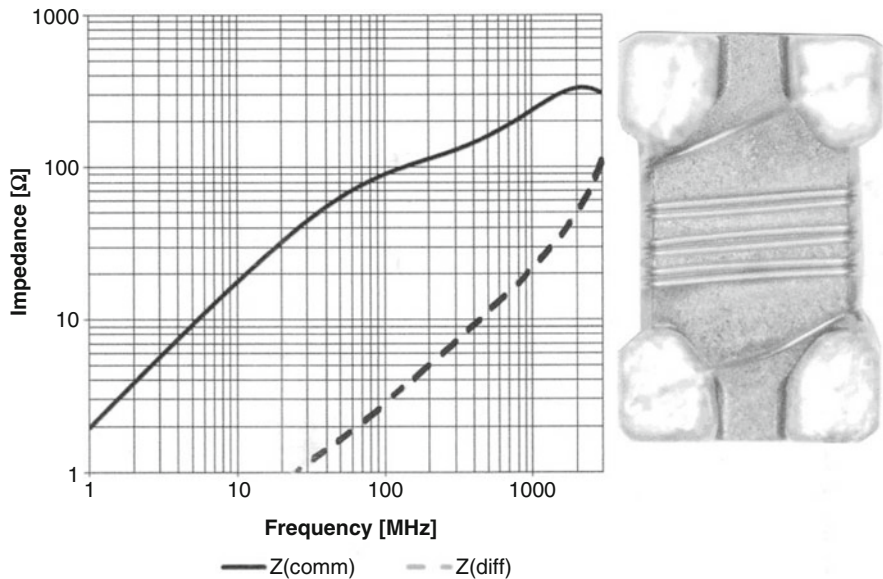


thanks to a 3- to 5-pole structure, can reach 25-30 dB one octave above cutoff frequency. The undesired DM inductance of a bifilar choke is caused by:

- (a) The leakage fields of the two opposite windings (non canceling in air), creating some transmission loss
- (b) A non-perfect symmetry of the two windings, adding some residual unbalance



**Fig. 11.15** Insertion loss of CM filter for high-speed bus, with built-in ESD protection (courtesy of STMicro, France)



**Fig. 11.16** CM (solid line) and DM (dotted) impedances of bifilar ferrite for high-speed bus (courtesy of Würth Electronics)

## 11.2 ADVANTAGES OF BALANCED INTERFACES

Compared with ordinary unbalanced driver/receiver links where each signal is simply transmitted or received between a single wire and a common return (e.g., RS232), balanced links offer the advantage of pairing each signal with its own return. Although primarily intended to improve EMI immunity, balanced links also reduce emissions.

The true balanced scheme (also termed true differential or bipolar) consists of transmitting a signal with equal positive and negative amplitudes relative to ground via a wire pair or twinax. In this manner, 100% of the outgoing current on one wire of the pair normally returned by the other wire, and no net current flows via the chassis and earth grounds (Fig. 11.17b). In reality, CM cancelation is not perfect because the symmetry of drivers and receivers is never perfect nor is the symmetry of the wire pair-distributed  $R, L, C$  parameters. The symmetry generally deteriorates at high frequencies. True differential drivers and receiver pairs normally need a double power supply to provide  $+V_{cc}$  and  $-V_{cc}$  vs. ground, but more and more devices are available where the dual polarity is generated internally, so they can be supplied from a single voltage source.

The pseudo-balanced link simultaneously delivers a logic pulse  $A$  and its complement ( $-A$ ). The signal is still referenced to a ground, as with an ordinary, unbalanced link, but, dynamically, when one output goes up, the other goes down. In theory, this scheme should provide a CM decoupling similar to that of the true symmetrical one. However, the positive signal edge and its complement are not perfectly in phase, due to different delays inside the device and, subsequently, on the PCB or backplane. This small shift (Fig. 11.18) causes both wires of a same pair to be at a positive (or negative) state at the same time for one nanosecond or less, causing the circulation of short spikes in the CM loop. In summary, balanced links will tend to radiate less than unbalanced ones, but no precise figure can be given for this reduction, particularly above 30 MHz, because of these short CM spikes exciting the whole cable. The lack of perfect symmetry between the upgoing and downgoing edges is related to three, more or less cross-related factors [10]:

- Peak amplitudes of the  $+V$  and  $-V$  pulses not perfectly equal
- Transition times  $t_r, t_f$  for upgoing and downgoing fronts not perfectly equal
- Small time lag (skew) between upgoing and downgoing fronts

This is particularly true for the high-speed LVDS links with data rates exceeding a hundred MHz. We have shown in Chap. 5 (Sect. 5.2.4) that although of lower amplitude, the upper end of the LVDS spectrum can easily exceed that of single-ended logic. To benefit from the LVDS in reducing EMI emissions, some parameters need to be strictly controlled:

- Output characteristics of the IC driver (symmetry of the slew rates, etc.)
- Symmetry of the differential traces on the PCB
- Symmetry of the external wire pair
- Proper matching to the characteristic impedance all along the transmitter to receiver LVDS link

Once amplitude and duration of these CM spikes are known, for instance, 50 mV/100 ps, the CM radiation of the link can be predicted like it has been for the short spikes in Chap. 3, Example 3.6, and Fig. 3.11.

### 11.3 LINE BALANCING DEVICES

With ordinary, unbalanced drivers and receivers, it is still possible to transfer data in a balanced mode by using line balancing devices such as:

- Signal or pulse isolation transformers
- Longitudinal (no isolation) transformers

Normally, such devices installed within the equipment near the I/O ports physically belong to Chap. 9. However, because they are aimed at reducing susceptibility and emissions related to external cabling, they are described in this chapter.

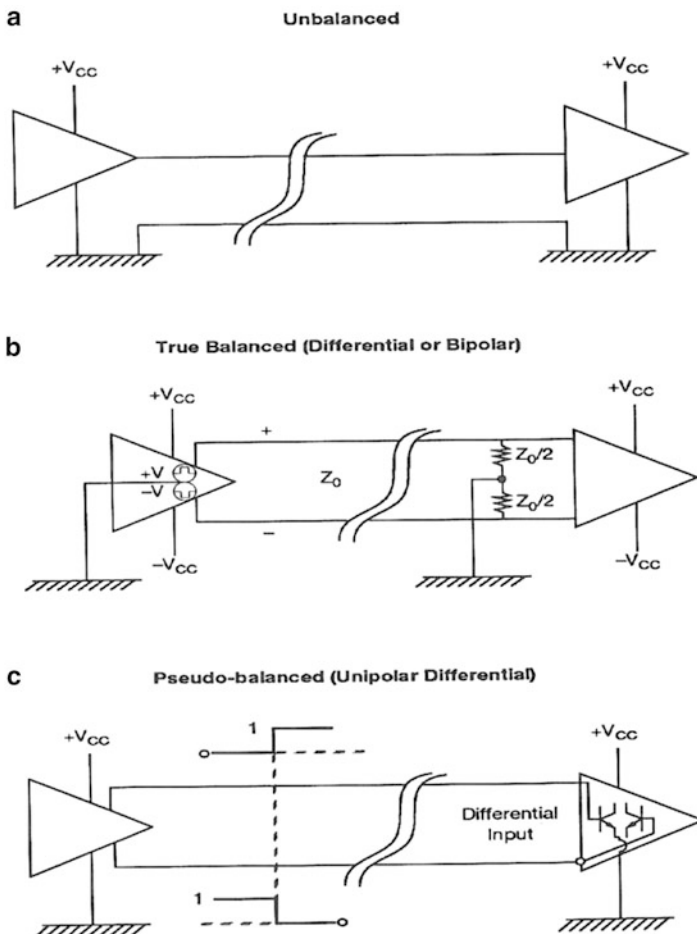
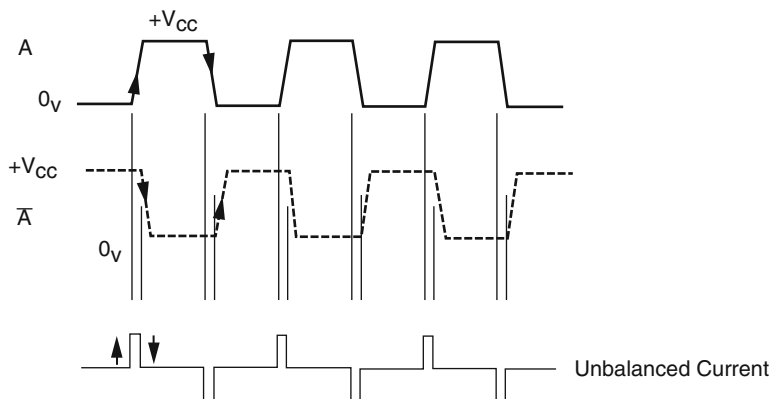
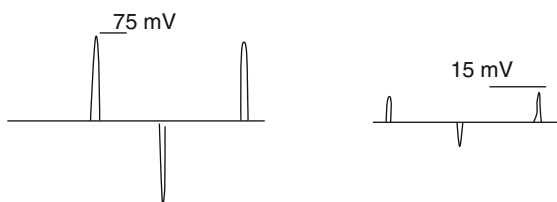


Fig. 11.17 Different types of digital line balancing



Example : Differential signal +/- 0.5V, T = 1 ns (2 GB rate), tr, tf : 50 ps  
 Measured Comm. Mode voltage on pair,  
 Effect of a 25 ps skew:

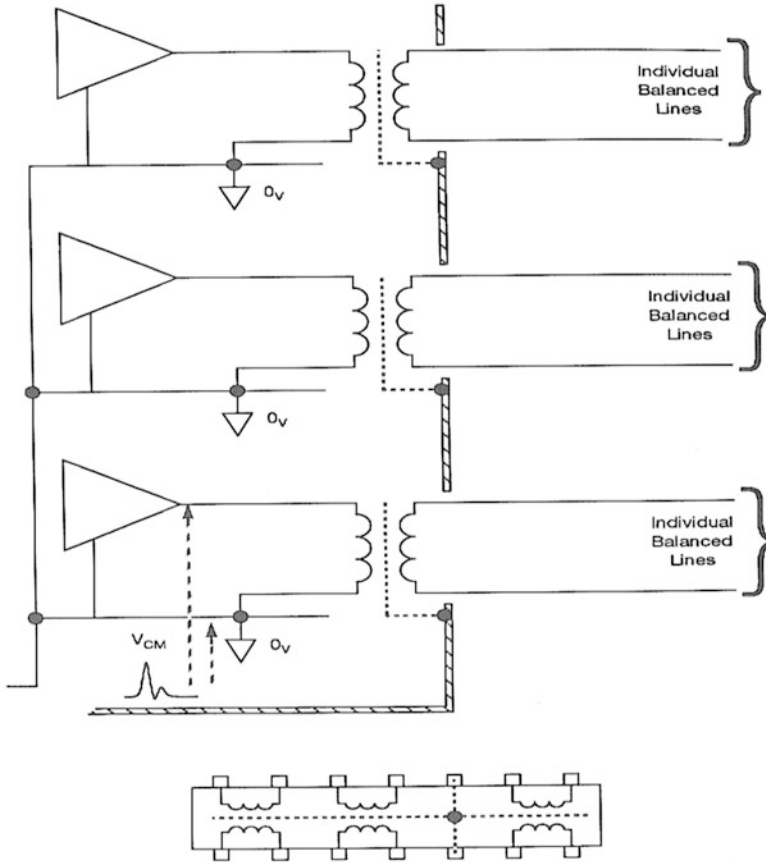
Effect of a 0.2pF unbalance  
 of 2 x 1pF I/O port CM filter :



**Fig. 11.18** Unbalanced problem with pseudo-balanced drivers. Due to small shift or dissymmetry between the A and A-bar transitions, short current spikes are driven into the system ground, corresponding to CM loop voltage

### 11.3.1 Signal Isolation Transformers

Signal or pulse transformers are used in many EMI suppression applications, from audio to video frequencies and above. Its applications include breaking ground loops, creating galvanic isolation, line impedance matching, and preventing balance-to-unbalance conversion, the latter being our prime concern here. Balancing transformers used in the local area networks (LANs), MIL-STD-1553, CAN, Ethernet, USB, and other communication links prevent injecting CM currents in external loops while sending DM signals in the same frequency band. Therefore, with proper precautions against primary-to-secondary couplings, the CM voltages developed on PCB traces and 0 V with respect to chassis do not drive the external pairs (Fig. 11.19).



**Fig. 11.19** Signal isolation transformers for DM transmission. They exist in DIP or SSOP package, with a Faraday shield

However, several secondary effects that are not visible at low frequencies do show up above the bandwidth of the useful transmitted signals, well into the critical frequency domain for spurious radiation. These effects are:

### 1. Mode conversion

Due to imperfect balancing of transformer windings, some of the DM voltage impressed on primary side appears as a CM signal on the line vs. ground. For the best transformers, this fraction is only 1-3% up to a few MHz but could aggravate at higher frequencies. The consequences on radiated emissions are severe, since CM excitation of cables is often the dominant mode. The parameter quantifying this coupling on the transmit side is the transverse conversion loss (TCL, Fig. 11.20).

### 2. Primary-to-secondary capacitance

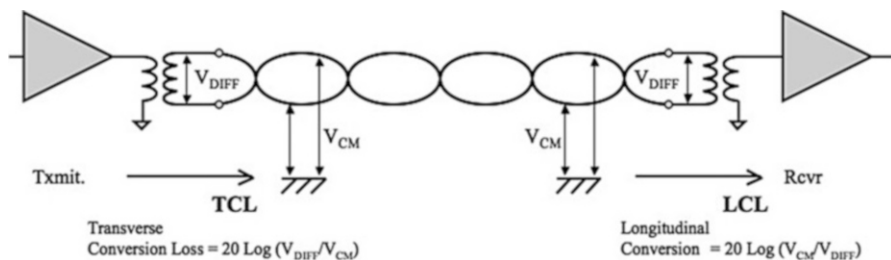
This capacitance can let an increasing portion of high-frequency internal CM voltages to appear as secondary CM voltages driving the wire pair. This too is of serious concern because CM excitation is the most efficient radiation contributor

to cable radiation. An electrostatic (Faraday) shield between the primary and secondary can reduce this effect.

For the designers, the useful information is the practical 3 dB bandwidth, corresponding to:

- The longest pulse width that can be processed without excessive amplitude droop
- The fastest rise time that can be processed without excessive distortion

For example, a pulse transformer with a 3 dB bandwidth of 0.15-100 MHz cannot process pulses longer than 2 μs and rise times shorter than 3.2 ns. The following Table 11.3 shows some features of signal/pulse transformers. In summary, isolation transformers behave as high-pass couplers for CM noise; their blocking effect against cable emission rates from excellent at low frequencies to poor at VHF and above. If employed, they need to be complemented by CM capacitive decoupling or bifilar CM chokes.



**Fig. 11.20** Transformer and interface unbalance, causing DM-to-CM conversion at the emission side

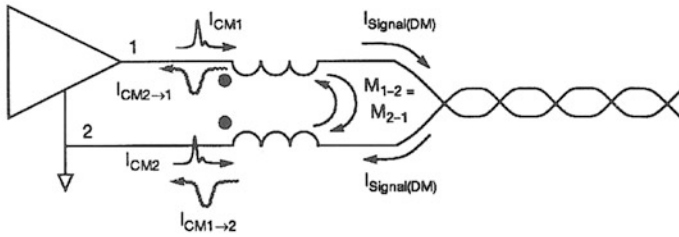
**Table 11.3** Some typical features of signal/pulse transformers

Type	Bandwidth		Parasitic capacitance, primary to secondary	CM rejection ratio CMRR
	$F_{min}$	$F_{max}$		
Audio transformer	300 Hz	3,300 Hz	60-100 pF	60 dB (in band)
Single/pulse (DIP)	10 kHz	100 MHz	15-40 pF (unshielded) 3-5 pF (shielded)	40 dB @ 1 MHz 20 dB @ 50 MHz
Video-wideband	20 Hz	30 MHz	50 pF	120 dB @ 60 Hz 30 dB @ 1 MHz

### 11.3.2 Longitudinal, Non-isolating Transformers

Based on the principle of mutual cancelation of equal CM currents, these bifilar chokes have the opposite features of isolation transformers (see Fig. 11.21). They do not block low frequencies (in fact, they are transparent down to DC) but can have excellent CM attenuation in the VHF (30-300 MHz) and UHF (0.3-3 GHz) ranges.

The mutual inductance between the coupled windings increases the CM loop impedance by as much as 3-30 times while having little effect on the DM signal, because DM fluxes are canceling in the magnetic core. They are available as discrete or DIP, SMT packages. One can assume that cable emission levels will be reduced by the same amount that CM current is reduced, and actual test results confirm this prediction. Isolation transformers and CM bifilar chokes combined in a single component (Fig. 11.22) are commonly found integrated in RJ45 or other high-speed connector sockets.



- For CM currents, fluxes are in phase in the coil. Each  $I_{CM}$  induces in the other wire a counter EMF that drives a cancelling current.
- For DM currents, fluxes are equal and in opposite directions; net flux = 0.

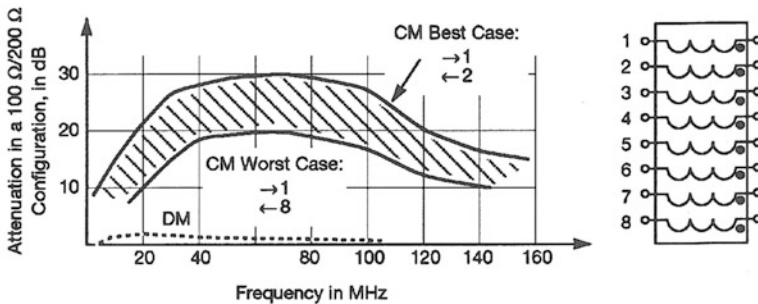
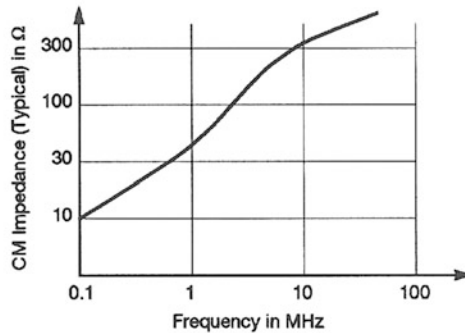


Fig. 11.21 Longitudinal, non-isolating transformer. Attenuation is shown for typical dual in-line signal transformers. DM attenuation for normal signal is less than 2 dB

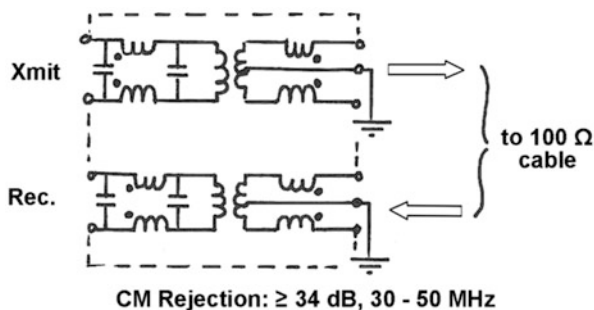


Fig. 11.22 Example of miniature signal transformer, combining galvanic isolation, bandwidth filter, and CM attenuation in a 25 × 10 mm size (source: Valor/Pulse Engineering)

### 11.4 REDUCING CM RADIATION BY FERRITE LOADING

Using a principle similar to that of the longitudinal transformers already discussed, ferrite beads are hollow cores or toroids that can be slipped over a wire or cable. They behave as a lossy inductance with one or more turns. Although they are popular among EMC specialists as quick “last chance” fixes, they can be incorporated in original designs to achieve remarkable EMI reduction, provided their theory is properly understood [3, 13]. In contrast to ferrites used in microwave applications (couplers, circulators) where low loss and best efficiency are aimed at, EMI ferrites are made of lossy materials having a good magnetic permeability ( $\mu_r$ ). Preferably their  $\mu_r$  is flat over a wide-frequency span, with typical values of 30-3,000. Although ferrite beads are generally thought of as inductors, they are in lossy transformers, with an equivalent resistance of 10 to few hundred ohms. Therefore, the impedance of the ferrite is more like

$$Z = \sqrt{(R^2 + (L\omega)^2)}$$

Two simple formulas can be used to calculate the  $L$  and  $R$  terms of a ferrite hollow core:

$$A_L = 0.2 \text{ nH} \times \mu_r \ell (\text{mm}) \log_n(d_2/d_1)$$

$$R \approx 6 \ \Omega \times \ell (\text{mm}) \log_n(d_2/d_1)$$

where

$A_L$  is the core inductive constant in nH for one turn (one pass through), a ferrite key parameter.

$\mu_r$  is the relative magnetic permeability of the core material (vendors can optimize the  $\mu_r$  for a given frequency domain). Above its optimum frequency,  $\mu_r$  generally starts rolling off to lower values.

$d_2, d_1$  is the outside diameter (or side dimension for a cubic shape), inside diameter.



As frequency increases,  $L$  and  $R$  become bypassed by the parasitic capacitance of the winding, typically 0.5-5 pF depending on core size and number of turns. Appendix D gives a more detailed modeling of a ferrite.

**Example** Toroid,  $d_2 = 12$  mm,  $d_1 = 6.3$  mm,  $\ell = 25$  mm,  $\mu_r = 100$ . Find ferrite impedance at 30 MHz for two pass.

$$A_L(\text{nH}) = 0.2 \times 100 \times 25 \log_n(12.7/6.3) = 345 \text{ nH}$$

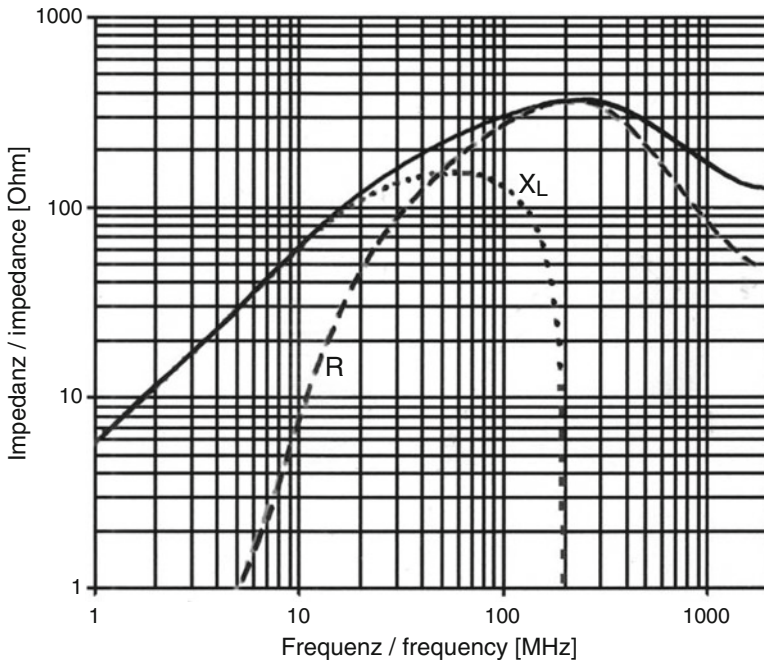
$$R = 6 \times 25 \log_n(12.7/6.3) = 104 \ \Omega$$

$$Z@30 \text{ MHz} = \sqrt{(104^2 + (2\pi 30 \times 10^6 \times 345 \times 10^{-9})^2)} = 123 \ \Omega$$

This is for one pass. With a second pass, impedance increases as  $N^2$ , thus  $Z_{(2 \text{ pass})} = 492 \ \Omega$ .

Assuming an average parasitic capacitance of 2 pF, this impedance will start decreasing above 100 MHz.

Due to their generally small size, ferrite beads can easily saturate for the normal current and become inefficient against the EMI current. The amount of current a bead can handle without significant decrease of  $\mu_r$  is given by the manufacturer and related to the bead outside and inside diameters. Beads with proportionally small holes are more efficient. Permeability is also affected by frequency. Some beads are optimized to work below 10 MHz, while others are suitable from 10 to 100 or even 1,000 MHz. Figure 11.23 shows the resistive and inductive parts of a typical bead impedance.



**Fig. 11.23** Impedance, reactance, and resistive parts of ferrite bead (courtesy of Würth Electronics)

Because of their low  $Q$ , beads are especially efficient for damping high-frequency contents of switching transients, clock harmonics, and parasitic resonances. By adding a frequency-dependent series impedance, they are an inexpensive way to create EMI losses without affecting DC or low-frequency signals. If a circuit or cable is exposed to a high-frequency EMI coupling, the bead will prevent the circulation of induced currents. Conversely, if a signal source contains undesired spurious noise, ferrites will prevent noise currents from propagating, turning the wire into a radiating antenna.

To gainfully use them, it must be understood that ferrites work by series insertion loss. Therefore, the attenuation or more exactly insertion loss they provided will be

$$A_{\text{dB}} = 20 \log \frac{V_0 \text{ without ferrite}}{V_0 \text{ with ferrite}} \quad (11.3)$$

$$\begin{aligned} &= 20 \log \frac{Z_L / (Z_g + Z_w + Z_L)}{Z_L / (Z_g + Z_w + Z_L + Z_b)} \\ &= 20 \log \frac{Z_g + Z_w + Z_L + Z_b}{Z_g + Z_w + Z_L} \end{aligned} \quad (11.4)$$

where

$Z_g, Z_L$  is the circuit source and load impedances

$Z_w$  is the wire impedance

$Z_b$  is the ferrite bead impedance

$V_0$  is the voltage across load

This equation reveals two things:

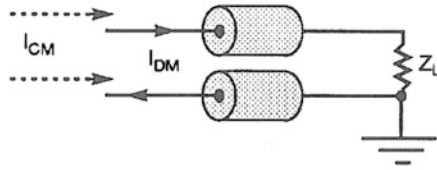
- (a) Ferrites will not work efficiently in high-impedance circuits. Although significant progress was made by manufacturers since the 1980s, the best ferrites today achieve values of  $Z_b$  in the 300-1,000  $\Omega$  range, above 50 MHz. For instance, neglecting wire impedance, the best attenuation a 300  $\Omega$  ferrite can provide in a 100/100  $\Omega$  configuration is:

$$A(\text{dB}) = 20 \log [(100 + 100 + 300)/(100 + 100)] = 8 \text{ dB for one pass through}$$

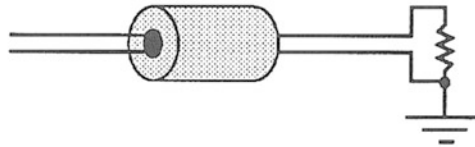
Conversely, ferrites will be very efficient in low-impedance circuits such as power distribution, power supplies, or radio-type circuits where impedances are 50 or 75  $\Omega$ .

- (b) If the cable loop impedance itself is high, ferrite performance may be disappointing because of the presence of  $Z_w$  in the equation.

Regarding the blockage of common-mode currents, as explained in Sect. 11.1.3 for inductors, if the two wires of a signal pair are threaded into the same bead, the ferrite will affect only the undesired EMI currents and have no effect on the intentional differential-mode current (Fig. 11.24) [2]. The same is true when a ferrite is slipped over a coaxial cable.



One ferrite per wire attenuates *DM* and *CM* currents (might affect useful signal)



One ferrite around two wires attenuates *CM* only.

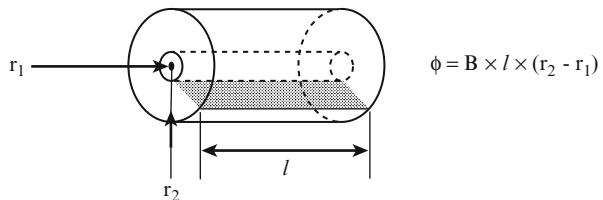
**Fig. 11.24** Common-mode vs. differential-mode operation of ferrite beads

In addition to their impedance limitations, ferrites have the following constraints:

- When cable length approaches  $\lambda/2$ , the bead could become less efficient if it gets into a current “null.” Against emissions this can be overcome by always placing the ferrite near the source side of the cable end.
- The end-to-end parasitic capacitance of the ferrite (typically 1-3 pF) may bypass its resistance above a certain frequency and cause its attenuation to collapse.
- Beyond about 1,500-2,000 Gauss, saturation occurs and efficiency decreases greatly.
- When slipped over multipair cables, ferrites may increase inductive crosstalk between adjacent pairs of different families.

The saturation problem can be controlled by checking the flux density  $B = \Phi/S$ . Figure 11.25 shows that core flux is a function of  $B \times I(r_2 - r_1)$ , given that if  $B$  is too large, core saturates and  $\mu_r$  will decrease.

**Fig. 11.25** Ferrite bead cross section and flux density



**Example 11.7** A ferrite has the following dimensions:

Length  $\ell = 1$  cm, outside radius  $r_2 = 0.5$  cm/inside radius  $r_1 = 0.2$  cm

Manufacturer data give the equivalent inductance  $L_b = 10^{-6}$  Henry, provided that  $B$  does not exceed 1,500 G. What is the maximum current this bead can handle without losing efficiency?

$$I = \Phi/L_b = \Phi/10^{-6} \quad (11.5)$$

Also,

$$\begin{aligned} \Phi &= B \times S(\text{m}^2) = B \times \ell \times (r_2 - r_1) = B \times 0.01 \ (0.5 - 0.2) \times 10^{-2} \\ \Phi &= B \times 0.3 \times 10^{-4} \end{aligned}$$

Given,  $B_{\max} = 1,500$  G = 0.15 T

$$\Phi_{\max} = 0.15 \times 0.3 \times 10^{-4} = 0.45 \times 10^{-5}$$

Equating with expression of  $I$ :

$$I_{\max} = \Phi_{\max}/10^{-6} = 4.5 \text{ A}$$

If the attenuation of a ferrite bead is not sufficient, this can be improved in several ways. One method is to make more than one pass of the wire through the bead hole. The increase in impedance is theoretically proportional to  $N^2$ , so two turns will give a four-times larger impedance (therefore, attenuation), three turns produce nine times the impedance, and so forth. Generally, if one turn gives poor results, two or three may be adequate. Making more turns, above a few megahertz generally won't help or may eventually shift the problem toward a lower frequency; this may also rapidly bring the ferrite into saturation, and the turn-to-turn capacitance could destroy the inductance improvement. Several beads back-to-back on the wire is another method, but less efficient: it would take nine beads to duplicate the result of three turns into a single bead.

Ferrite beads are available in cylindrical or flat core shapes (Fig. 11.26). Split versions are available for quick installation during EMC troubleshooting. Multihole beads are not suitable for fitting on external cables but can be mounted in the PCB I/O area. Be careful that, in this case, the two wires of a line are not mutually coupled: a multihole bead will affect DM signal as well as CM.

Figure 11.27 shows a typical result of installing ferrites on unshielded cables connected to a small personal computer. The objective was to meet FCC Class B specifications. In this case, the cables were the major radiators, and the ferrites did wonders [13]. As will be discussed in Chap. 13, this may not be enough if box radiation alone is also violating the limits.

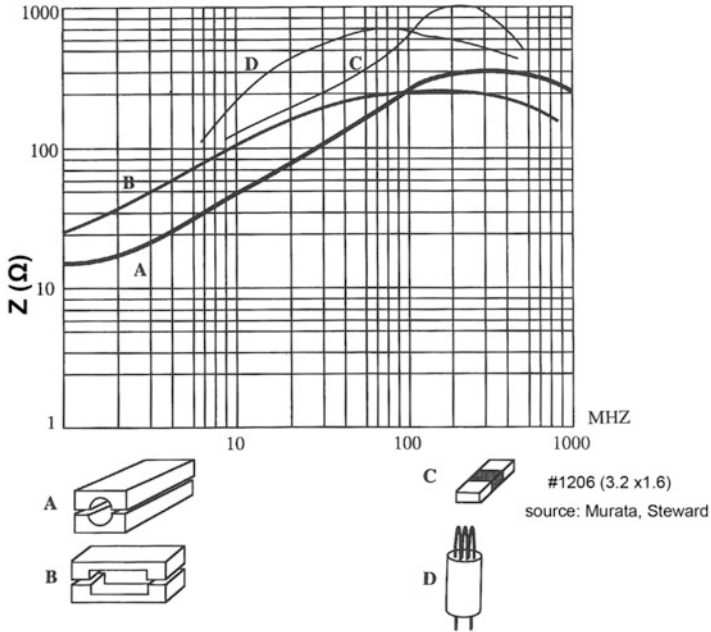


Fig. 11.26 EMI suppression performance of small and large ferrite beads. For A and B styles, impedance is shown for one pass ( $N = 1$ ). For  $N = 2$  or 3,  $Z$  is multiplied by  $N^2$  up to  $\approx 150$  MHz

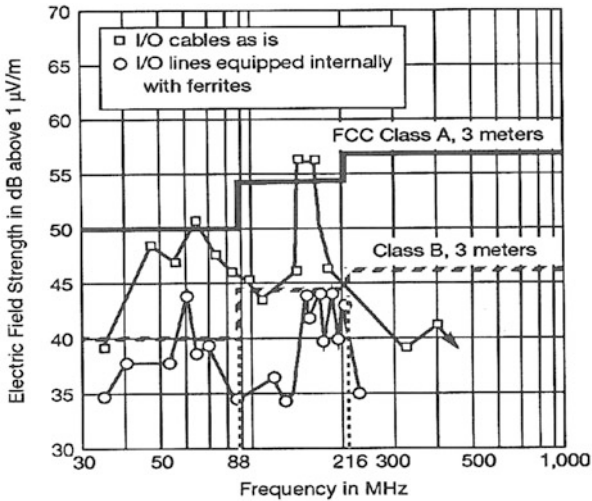
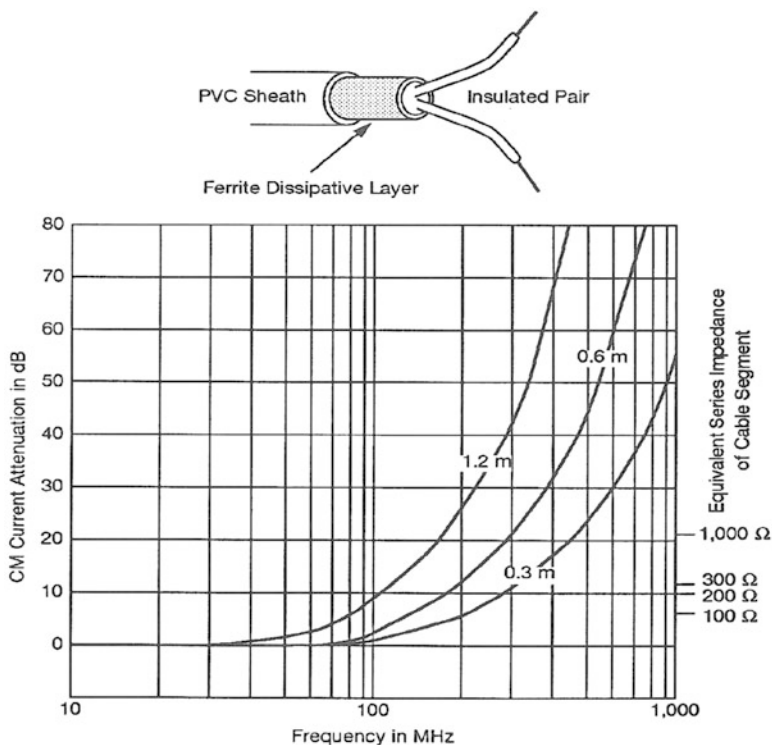


Fig. 11.27 Effect of long ferrite beads on radiation from I/O cables (from [13])

### 11.4.1 Ferrite-Loaded Cables and Tubing

Derived from the lossy ferrite principle, an interesting extension has attracted a growing interest since the late 1970s. Instead of inserting discrete ferrites over a multiconductor cable, the whole cable length is made lossy by coating all the wires under the jacket with a ferrite-loaded jacket [8, 9]. This provides essentially CM attenuation, with very little DM attenuation. To maintain flexibility, the ferrite powder is embedded in a soft binder, so the ferrite percentage in volume is rather low, corresponding to a relative permeability of a few tens. By avoiding the ringing due to impedance discontinuities that a cascade of beads would create, ferrite-loaded wires have a more even attenuation performance above 100 MHz. The impedance of such lossy cables is shown in Fig. 11.28



**Fig. 11.28** Attenuation of lossy cable, measured in 50/50 Ω, cable 5 cm above ground (Eupen Cables)

## 11.5 REDUCING DIFFERENTIAL-MODE RADIATION BY TWISTING

Twisting the two wires of a pair has virtually no effect on CM radiation, although a slight improvement in the symmetry of each wire-to-ground distributed inductance and capacitance may result. It has a strong effect on DM radiation. Since this mode is seldom a problem, twisting does not create a major reduction in overall radiated field. However, since each contributor plays its part, when efficient CM reduction techniques have been applied (such as reducing CM pollution of I/O cables by 25 or 30 dB), the DM contributor may resurface. In fact, if the DM contribution of the untwisted pair is only 5% of the CM one, reducing this latter by 30 dB (a 30-times factor) will reveal the DM radiation. Reduction of the radiated field produced by twisting a wire pair is expressed (from [16]) by

$$A_{\text{dB}} = 20 \log \frac{E \text{ field w/o twisting}}{E \text{ field after twisting}} \quad (11.6)$$

$$= 20 \log \frac{1 + 2n\ell}{1 + 2n\ell \sin \frac{F(\text{MHz})}{100 \times n}} \quad (11.7)$$

where

$n$  = number of twists/m

$\ell$  = total twisted length

Looking at Equ. (11.7):

When  $F \ll 100n$ , the attenuation simplifies as  $A = 20 \log (1 + 2n\ell)$ .

When  $(F/100n)$  approaches  $\pi/2$ ,  $A = 0$  dB.

This formula assumes that:

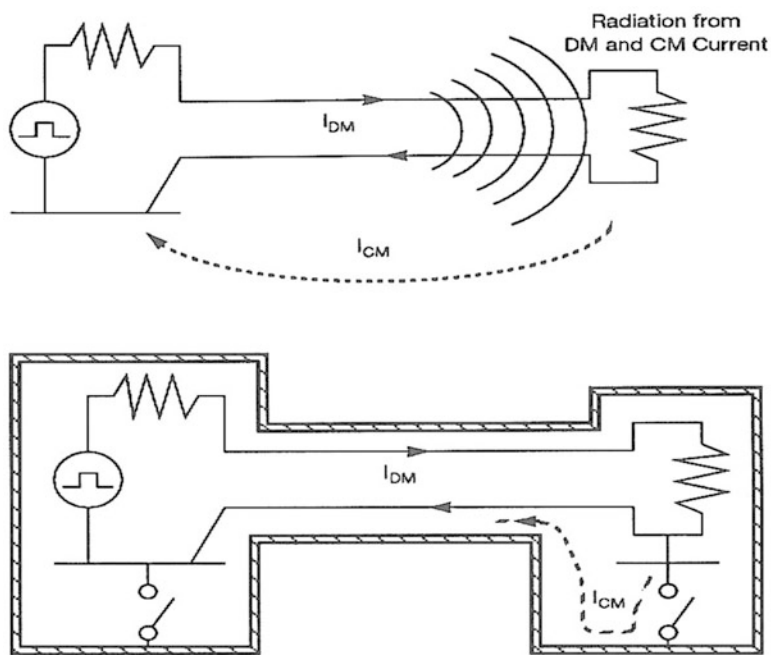
1. There is always an odd (uncancelled) loop, or a small untwisted segment at the end of the wire, whose length equals approximately  $\ell/n$  meters.
2. The entire pair length is twisted. (Twisted flat cables with untwisted sections will show less reduction.)

## 11.6 REDUCING CABLE RADIATION BY SHIELDING

Although shielding a cable may appear as the obvious “catch-all” barrier to radiated emissions, application may not be so easy. Throwing-in shielded cables at the last minute may give disappointing or nonexistent results. The author has even seen weird cases where shielded cables increased radiated levels at some frequencies. There are explanations to this, of course, as will be seen. The basic principle for a shield to work against all types of EMI, with the widest coverage of situations ( $E$  field and  $H$  field, low and high frequencies, DM and CM, etc.), is to create a

continuous barrier that encloses the conductors and is 360° bonded to the conductive boxes at both ends. No matter which theory is employed to model this shield (reflection loss, absorption loss, Faraday cage effect, mutual inductance, ad infinitum), calculations and experiments show that when the entire system is enclosed in a continuous barrier, its radiated EMI is reduced. This principle works whether the barrier is earthed or not (Fig. 11.29).

If the boxes are not six-face metallic cubicles, the principle still can work, provided there is at least one large metal face or ground plane on both ends that terminates the shields and closes the cable-to-shield return path for CM currents. Otherwise, without reference plate for terminating the shields (as in the case of solid plastic boxes), a cable shield will not be efficient in reducing EMI-radiated emissions. Adequate I/O port decoupling and ferrite loading are more appropriate for such a situation, if less than 20 to 30 dB reduction is needed.



**Fig. 11.29** An ideal shielded system. Provided the metal barrier is uninterrupted and homogeneous, radiation is strongly reduced, whether or not the inner circuit is grounded to the shield or the shield connected to earth

If, for legitimate reasons (e.g., low-frequency ground loops between distant boxes, upsetting a sensitive analog input), a cable shield has to be grounded at one end only, it will be only effective against LF electric fields and capacitive crosstalk. It has virtually no effect on CM immunity or radiation, as the CM loop current does not return by the shield but rather by the chassis and ground plane, as if



there were no shield. However, as frequency increases, some percentage of the CM current returns by the internal wire-to-shield capacitance. But shield impedance also increases with frequency (Fig. 11.30). Therefore, if we designate:

- $V_{CM}$  the CM noise voltage driving the pair
- $C_p$  the pair-to-shield distributed capacitance
- $Z_{sh}$  the shield impedance =  $R_{sh} + j\omega L_{sh}$
- $L_{sh}$  the external shield-to-ground self-inductance
- $I_{sh}$  the shield current

Then, we can express the voltage vs. ground of the shield’s floated end:

$$V_{CM} = \sum I_{sh}Z_{sh} = V_{CM}C_p w (R_{sh} + j\omega L_{sh}) \tag{11.8}$$

Therefore, above a few kilohertz,

$$V_{sh}/V_{CM} = L_{sh}C_p\omega^2 \tag{11.8a}$$

The shield voltage vs. ground increases with frequency squared, becoming a significant fraction of  $V_{CM}$ . The floated end of the shield becomes the “hot” tip of a radiating monopole, and we have just replaced a radiating pair by a radiating shield. So, exceptions acknowledged, *a cable shield must be connected at both ends to the boxes, whether these are grounded or not.* Exceptions are:

- Low-level analog instrumentation (strain gages, thermocouples, etc.)
- Audio interface cables

In these applications, only an electrostatic shield is needed. Ground loops are suppressed by galvanic isolation amplifiers, differential amplifiers, and so forth, and grounding a shield at both ends could inject LF (few kHz) noise into the cable. A few millivolts injected this way are harmless for digital interfaces but can constitute strong interference for low-level analog signals. Notice that it is unlikely that such analog cables would radiate RFI. If this were to happen, at least the floated end of the cable shield should be grounded at RF frequencies (>MHz) through a capacitor of a few nanofarads value.

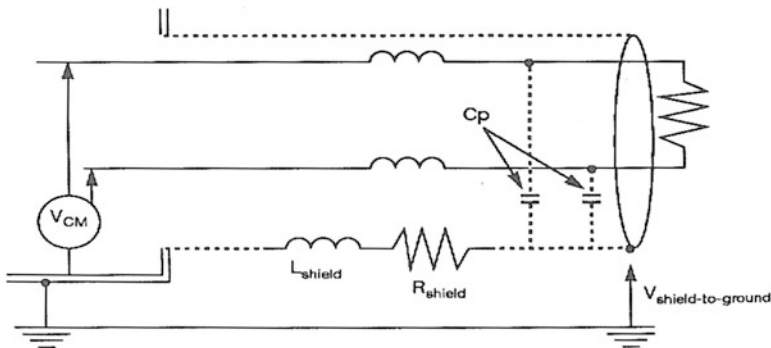


Fig. 11.30 Radiated emission with floated-end shield

### 11.6.1 Fields Radiated by a Coaxial Cable

Most RF signals, baseband video, some LAN links, and other high-frequency signals are carried on coaxial cable. When a coaxial cable carries a signal, only a very little current (typically 0.3-0.1%, above a few MHz) returns by paths other than the shield itself (Fig. 11.31). This assumes that the shield is at least correctly tied to the signal ground reference at both ends and preferably also to the chassis by the coaxial connectors. This external current radiates a small electromagnetic field that can be associated with the quality of the shield and its installation. It is related to the voltage appearing along the shield due to the transfer impedance of the braid.

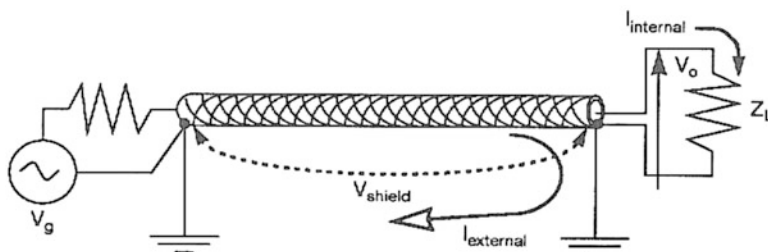


Fig. 11.31 Field radiation by the external shield current

A convenient way of characterizing the merit of a cable shield [14, 15] is by its transfer impedance,  $Z_t$ . It relates the current flowing on a shield surface to the voltage it develops on the other side of this surface (Fig. 11.32). This voltage is due to a diffusion current through the shield thickness (if the shield is a solid tube, this diffusion rapidly becomes unmeasurable as frequency increases, due to skin effect) and to the leakage inductance through the braid's holes. The better the quality of the braid, the lesser the longitudinal shield's voltage.

Initially,  $Z_t$  was used for susceptibility calculations and defined as

$$Z_t(\Omega/m) = V_i/(\ell(m) \times I_{sh}) \tag{11.9}$$

where

$V_i$  is the longitudinal voltage induced inside the shield, causing a noise current to circulate in the center conductor

$I_{sh}$  is the external current injected onto the shield by the EMI source

However, the principle is perfectly reciprocal and can be applied to emissions as well (see Fig. 11.32). The internal, intentional current  $I_0$  returning by the shield's inner surface causes an EMI voltage to appear along the outer side of the shield; it can be expressed as

$$V_{ext} = Z_t(\Omega/m)\ell(m)I_0 \tag{11.10}$$

$$= Z_t(\Omega/m)\ell(m)V_o/Z_L \tag{11.11}$$

where:

$V_{ext}$  = external voltage appearing along the shield-to-ground loop  
 $V_0, I_0$  = signal voltage and current on load side ( $Z_L$ ) of the coaxial cable

This voltage excites the antenna formed by the external cable-to-ground loop. Typical values of  $Z_t$  for various cables are shown in Fig. 11.33. If the shield is grounded by pigtails (a poor practice), the pigtaills' and other impedances must be added to the  $Z_t$  and loop impedances calculations.

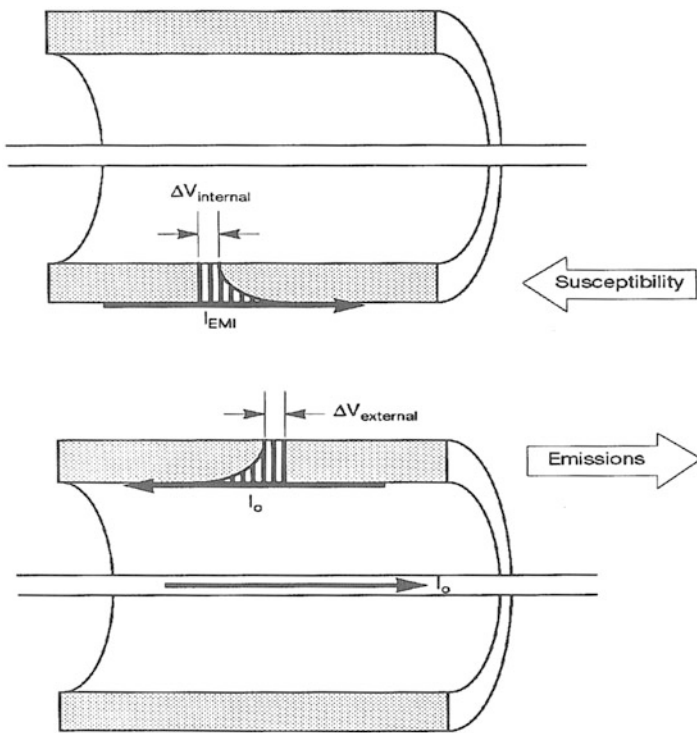
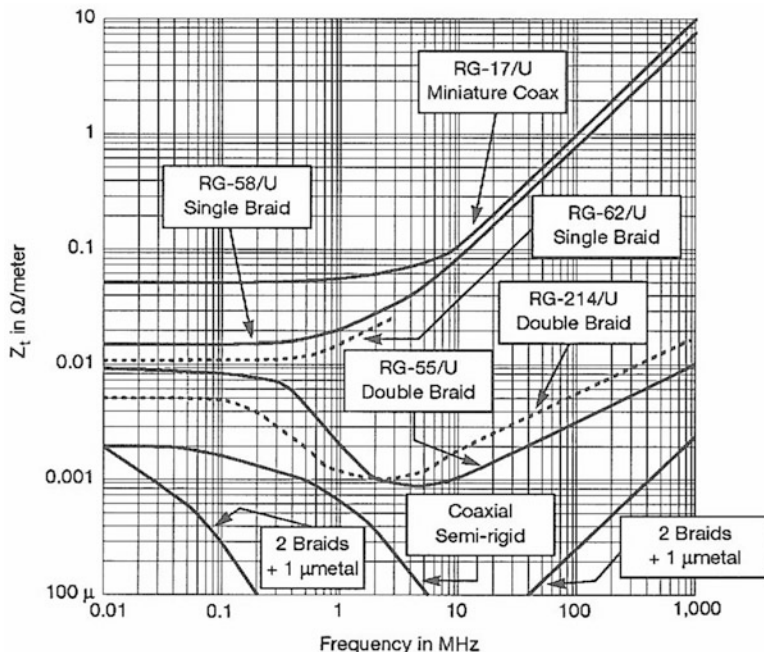


Fig. 11.32 The transfer impedance concept: reciprocity of susceptibility and emissions



**Fig. 11.33** Typical values of transfer impedance,  $Z_t$ . Above 150 MHz, values in  $\Omega$  for 1 m are indicative only, since  $l > \lambda/2$

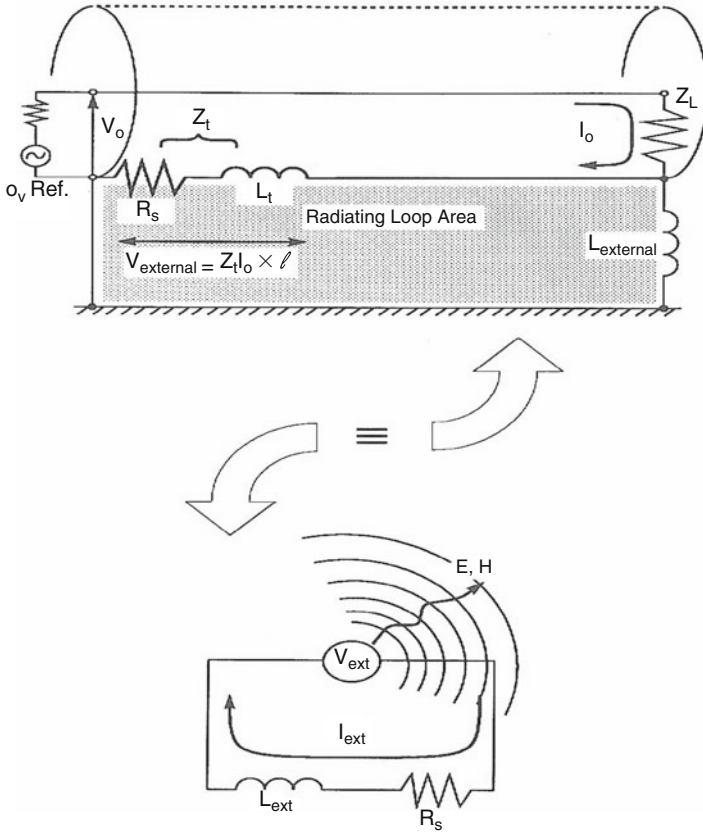
The term  $Z_t$  itself contains the shield resistance  $R_h$  and the shield transfer inductance  $L_t$  that can be regarded as the leakage inductance from the inside-out (or the reverse), such as

$$Z_t(\Omega/m) = R_{sh}(\Omega/m) + j\omega L_t(H/m)$$

Typical values of  $R_{sh}$ ,  $L_t$  for a decent quality, single-braid shield are 15 m $\Omega$ /m and 1-2 nH/m, respectively.

For a single-braid coaxial, with an outer diameter in the 5 to 15 mm range, at a height of 50-500 mm above ground, an average value of the external loop impedance is:

$$Z_{ext} = [10 \text{ m}\Omega + j 6 \Omega \times F(\text{MHz})] \text{ per meter length}$$



**Fig. 11.34** Equivalent circuit to predict coaxial cable radiation

Eventually, pigtail or connector impedances have to be incorporated into  $Z_{ext}$ , although their contribution is usually minimal. *In contrast, their contribution to  $Z_t$  is very important*, as  $Z_t$  must be hundreds or thousands of times smaller than  $Z_{ext}$ , for a good shield. Then, to estimate  $E$  and  $H$  field from this low-impedance loop (Fig. 11.34), the external shield current can be calculated by

$$I_{ext} = V_{ext}/Z_{ext}$$

If the shield is floated from the chassis, the coaxial becomes an electrically driven radiator, and Fig. 2.6 (Chap. 2) can be used with  $V_{ext}$ , as the input. When the cable becomes electrically long,  $Z_t$  ( $\Omega/m$ ) no longer can be multiplied by the length, since the current is not uniform along the cable shield. A default approximation is to consider that the maximum amplitudes of the shield voltages distributed along the shield is:

$$V_{ext}(\max) = Z_t(\Omega/m) \times \lambda/2$$

Thus, as  $Z_t$  increases with  $F$ , the effective length that multiplies  $Z_t$  decreases with  $F$ , such as the two effects are canceling each other, resulting in a maximum external

voltage that remains constant with frequency. At the same time, the cable-to-ground external impedance needs to be replaced by  $Z_0$ , the corresponding characteristic impedance, using the formula shown earlier as Equ. (2.25), Chap. 2:

$$Z_0 = 60 \log_n(4h/d)$$

### 11.6.1.1 Defining a Shield Reduction Factor $K_r$

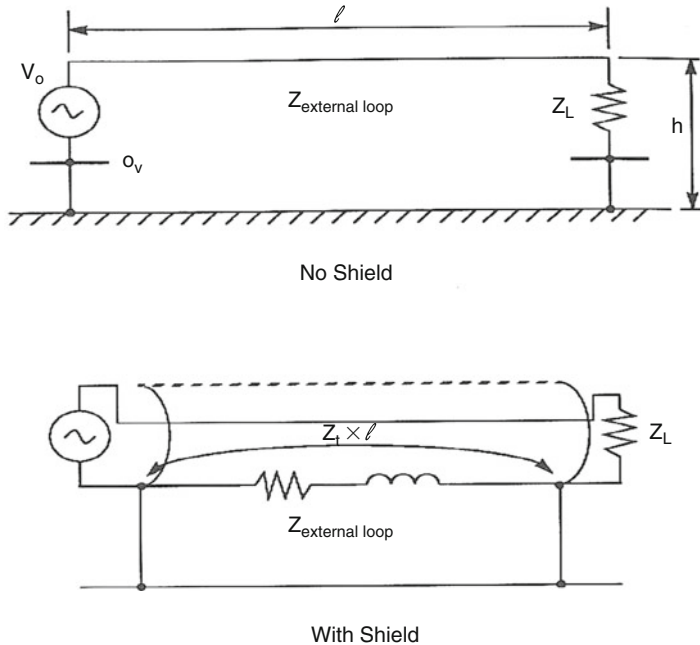
The concept of using  $Z_t$  and associated mechanisms as the cause for the signal inside to radiate outside is interesting and allows for a correct estimation of the field radiated by a coaxial (or any shielded) cable.

Yet, the sequence of calculation steps is laborious: it requires calculating the inside current, then the longitudinal voltage outside the shield, and finally the field radiated by the external loop excited by this shield voltage. On top of this, the design engineer—not necessarily an EMC specialist—is often more interested by the final result: “How many dB of radiated EMI reduction can I expect from a given shield?” Urged by this legitimate need to predict and compare the efficiency for a variety of shielded cables, having various screens, braid, foil, spiral, corrugated, shields, very simple practical formulas that directly express the cable shielding factor  $K_r$  given its transfer impedance  $Z_t$  ( $\Omega/m$ ) have been devised [6]. This shielding factor  $K_r$  becomes a dimensionless number in dB, which incorporates  $Z_t$ , but allows for a straightforward prediction of an installed shielded cable.

*Regarding susceptibility*, a shield reduction factor ( $K_r$ ) is the ratio of the differential-mode voltage ( $V_d$ ) appearing, core to shield at the receiving end of the cable, to the common-mode voltage ( $V_{cm}$ ) applied in series into the loop. It can be expressed by

$$K_r(\text{dB}) = 20 \log(V_d/V_{cm})$$

*Regarding emission*, a reciprocal definition, similar to the basis of Equ. (11.11) can be used for characterizing a shielded cable, simply by the ratio of the common-mode voltage ( $V_{cm}$ ), appearing in series into the external loop, to the differential-mode voltage ( $V_d$ ) applied, core to shield at one end of the cable. Calculations and experiments have shown that, except for the sign, the  $K_r$  factor is the same. This figure could also be regarded as the mode conversion ratio between the internal circuit (center conductor and shield) and the external one (the shield-to-ground line). A variation of this definition would be to compare the current in the loop if the shield was not there to the remaining loop current when the shield is in place, grounded both ends (Fig. 11.35).



**Fig. 11.35** Simplified view of the shield reduction factor ( $K_r$ ) definition. It compares the current in the external loop with and without the shield connected

This latter definition, more rigorous, is somewhat reminiscent of the insertion loss used in EMC terminology, i.e., it compares what one would get without and with the shield, for a same excitation voltage. This eliminates the contribution of the core wire resistance and self-inductance, since they exist in both measurements. A complete demonstration of the rationale leading to the expression of  $K_r$  can be found in [6]. We will just give the end results, expressing  $K_r$  as a *dimensionless number, independent of the cable length*:

$$K_r = \frac{R_{sh} + j\omega L_t}{R_{sh} + j\omega L_{ext}} \tag{11.12}$$

where

$R_{sh}$  = shield resistance in  $\Omega/m$

$L_{ext}$  = self-inductance of the external shield-to-ground loop

$L_t$  = Transfer inductance of shield

This expression unveils three basic frequency domains:

**(a) For very low frequencies**, where the term  $\omega L_t$  is negligible,  $Z_t$  is dominated by  $R_{sh}$ :

$$K_r = R_{sh} / (R_{sh} + j\omega L_{ext})$$

$\approx 1$  (0 dB) below few kHz, since the lower term, loop impedance reduces to  $R_{sh}$

(b) *At medium frequencies* (typically above 5-10 kHz for ordinary braided shield):

$$K_r = (R_{sh} + j\omega L_t)/(j\omega L_{ext})$$

Here the reduction factor increases linearly with frequency.

(c) *At higher frequencies* (typically above 1 MHz), up to first  $<\lambda/2$  resonance, the reduction factor stays constant, *independent of length and frequency*:

$$K_r = L_t/L_{ext}$$

A quick, handy formula is derived that is valid for any frequency from 10 kHz up to first  $<\lambda/2$  resonance<sup>2</sup>:

$$\boxed{K_r(\text{dB}) = -20 \log [1 + (6 F(\text{MHz})/Z_t(\Omega/\text{m}))]} \quad (11.13)$$

The value for  $Z_t$  being that taken at the frequency of concern

### 11.6.1.2 $K_r$ Values When Cable Length Is Approaching or Exceeding $\lambda/2$

As already said for  $Z_t$ , when the dimension of the cable reaches a half-wave length, the shield is no longer carrying a uniform current. In fact, the “electrically short line” assumption becomes progressively less and less acceptable when cable length  $\ell$  exceeds  $\lambda/10$ . The shield grounded both ends behaves as a dipole exhibiting self-resonance and antiresonance for every odd and even multiple of  $\lambda/2$ , respectively.

Accounting for the fact that actual wave propagation in the loop is about 0.7 times slower than in free space ( $3 \times 10^8$  m/s), the effective wavelength  $\lambda'$  is recalculated to find the actual resonances. At these frequencies, the shield current will exhibit peaks, resulting in approximately 10 dB periodic degradations of factor  $K_r$  (Fig. 11.36). This is translating correctly the actual situation where, for a uniform signal voltage driving the inner conductor, the radiated field will periodically increase beyond the first resonance point. Entering typical values for the shield-to-ground characteristic impedance, worst-case values for the outer shield current at  $\lambda/2$  resonance, resulting from the inner signal is:

$$I_{sh(\max)} = I_{loop(\max)} = V_{\max}/Z_c$$

<sup>2</sup> Several formulas have been proposed in the past, expressing a cable shield effectiveness based on its  $Z_t$ . An often mentioned quick rule is  $SE(\text{dB}) = 40 - 20 \log(Z_t \ell)$ . Although it is correct above the ohmic region of  $Z_t$ , it can give widely optimistic results, like 50 or 70 dB at 50/60 Hz where an ordinary shield has no effect at all against common-mode-induced interference.



where  $Z_c$  is the characteristic impedance of cable-above-ground transmission line =  $150 \Omega$  for a height/diameter ratio = 4 (typical of MIL-STD-461 test setup)  $\approx 300 \Omega$  for a height/diameter ratio = 50

For simpler calculations,  $Z_c$  can be given an average default value of  $210 \Omega$  (a  $\pm 3$  dB approximation)

Combining these  $\lambda/2$  specifics with a conservative approach,  $K_r$  (worst case) is aligned on the asymptote of the humps (Fig. 11.37), and we arrive at a simple expression for worst-case  $K_r$  above resonance:

For susceptibility:  $K_{r(\min)} = V_{\text{dmax}}/V_{\text{cm}} = (0.7 L_t V_{\text{cm}}/210)/V_{\text{cm}}$

For emission:  $K_{r(\min)} = V_{\text{cm}}/V_{\text{dmax}}$

Thus, for both cases, above resonance:  $K_{r(\min)} \text{ (dB)} = -20 \log [210/0.7 L_t(\text{nH/m})]$

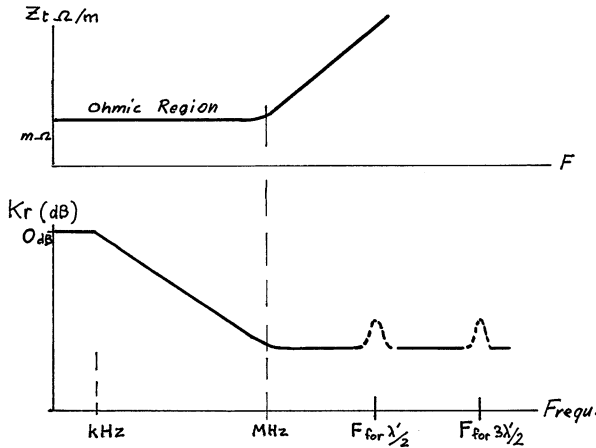
$$K_{r(\min)}(\text{dB}) = -20 \log [300/L_t(\text{nH/m})] \tag{11.14}$$

As a recap of  $K_r$  for below and above resonance conditions:

For cable length  $< \lambda/2$ :  $K_r \text{ (dB)} = -20 \log [1 + (6 \cdot F(\text{MHz})/Z_t(\Omega/\text{m}))]$

For cable length  $> \lambda/2$ :  $K_{r \text{ min}} \text{ (dB)} = -20 \log [300/L_t(\text{nH/m})]$

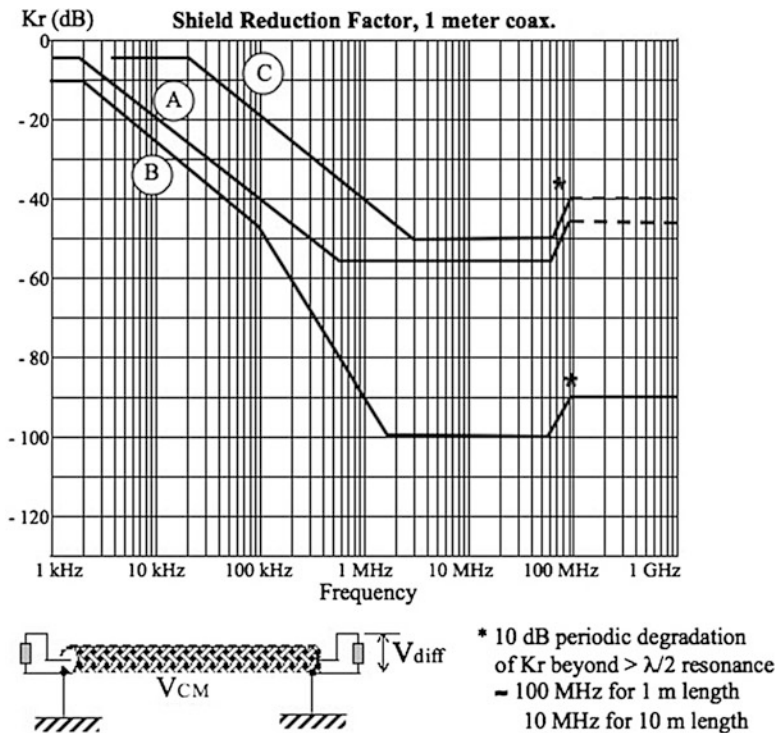
Details of calculations for obtaining these  $K_r$  equations can be found in [6].



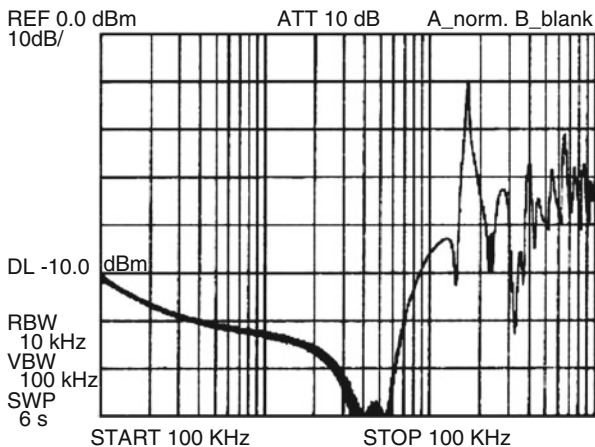
**Fig. 11.36** Conceptual view of the  $K_r$  behavior above resonance. Even with a good quality shield, the periodic shield current humps at odd multiples  $\lambda/2$  account for a typical 10 dB deterioration of  $K_r$

### 11.6.1.3 A Few Practical Results for $K_r$ , Below and Above First Cable Resonance

The following figures show calculated results using the formulas and actual test results. Figure 11.37 shows calculated results for three types of coaxial cable, 1 m above ground, with perfect 360° contact at connector backshell. The curves are valid for any length, provided that the resonance region is adjusted if length is different from 1 m. Figure 11.38 shows test results for a 5 m coaxial cable where the shield is intentionally spoiled by a 10 cm pigtail. The deterioration of  $K_r$  above 8 MHz is spectacular.



**Fig. 11.37** Reduction factor for shielded cables: (a) RG-58 single-braid coaxial, (b) RG-214 double-braid coaxial, (c) RG-174 single-braid, 2 mm diameter miniature coaxial



**Fig. 11.38**  $K_r$  for a 5 m coaxial cable, shield grounded with 10 cm pigtail (courtesy of AEMC, France)

Knowing its  $Z_t$ , hence its corresponding shield reduction factor  $K_r$ , the routine for predicting the radiated field from a given shielded cable is simple. It assumes that the radiation from the shield equals what would be radiated by the signal current of the bare, unshielded center wire, reduced by the  $K_r$  factor:

1. Determine the driving signal voltage spectrum.
2. Determine the signal current in inner conductor ( $V_{source}/R_{load}$ ).
3. Read from curve, or calculate,  $K_r$  for this shielded cable.
4. From (2) and (3), determine the outer current in shield-to-ground loop.
5. From loop (or dipole) radiation equations (Chap. 2), calculate the radiated  $E$  field.

**Example Problem 11.8** A 2 m piece of RG-178 coax is connecting two racks. The electrical parameters are:

Useful signal	15 MHz video
Load resistance	50 $\Omega$
$V_o$ amplitudes	Fundamental = 10 V
	Harmonic #3 = 3 V
	Harmonic #10 = 0.3 V

The cable parameters are:

Shield resistance and transfer inductance (from manufacturer's  $Z_t$  curve):  $R_{sh} = 45$  m $\Omega$ /m,  $L_t = 2$  nH/m  
 Cable outer diameter = 0.2 cm  
 Height above ground = 30 cm

Good quality BNC connectors are used at both ends (2.5 m $\Omega$ /connector).

Calculate the radiated field at 3 m for these three frequencies (fundamental and harmonics #3 and #10).

**Solution** We need to determine the radiating loop area:  $A = 2\text{ m} \times 0.3\text{ m} = 0.6\text{ m}^2 = 6,000\text{ cm}^2$  or  $76\text{ dBcm}^2$ .

The table below shows the calculation steps for radiated field at 3 m.

Frequency	15 MHz	45 MHz	150 MHz
(1) $V_0(\text{dBV})$	20	10	-10
(2) Current = $V_0/50\ \Omega$ , $I_0(\text{dBA}) = V_0 - 34\text{ dB}$	-14	-24	-44
(3) $Z_t\ (\Omega/\text{m})$ , from curve	0.15	0.5	(*)
(4) $K_r$ (coax), ( $\ell < \lambda/2$ ) calculated with $Z_t$	-55 dB	-54 dB	
( $\ell > \lambda/2$ ) calculated with $L_t$			-44 dB
(5) Outer loop current = (2)-(4) (dBA)	-69	-78	-88
(6) Radiating area, with reduction above $\lambda/4$ ( $\text{dBcm}^2$ )	76	74	64
(7) $E$ field @ 3 m for $1\text{ cm}^2$ loop carrying 1 A: $E = 20\log[(1.3 \times 1\text{ A} \times 1\text{ cm}^2 \cdot F^2)/3]$ ( $\text{dB}\mu\text{V/m}$ )	40	59	80
(8) Total $E$ field: (5) + (6) + (7)	47	55	56
Limit FCC Class B ( $\text{dB}\mu\text{V/m}$ ) <sup>(**)</sup>	NA	40	43
$\Delta$ above limit (dB)	NA	15	13

<sup>(\*)</sup>For the 150 Mz case, where ( $\ell > \lambda/2$ ),  $Z_t$  is not used, and  $L_t$  is used instead

<sup>(\*\*)</sup>As it was explained in Chap. 2, Sect. 2.5, the 3 dB that should be subtracted for peak-to-rms conversion are  $\approx$  offset by the ground plane reflection of the FCC/CISPR test setup

Although these radiated levels are about 50 dB lower than if a bare wire were carrying the same current with a return by the ground plane, FCC limit is exceeded by 13-15 dB. Had the requirement been a MIL-STD-461-RE102 instead, the field (45 MHz) would be  $49\text{ dB}\mu\text{V/m}$  at 1 m, that is, 29 dB above limit.

Several possibilities exist to reduce the radiated field:

1. Select a coaxial cable with a lower  $Z_t$ , i.e.,  $Z_t \leq 0.1\ \Omega/\text{m}$  at 45 MHz. Such performance is achievable with optimized braided shield (thicker, denser braid) or more easily with more costly double-braid shield.
2. Slip a large ferrite bead over the cable shield. It will take an added series impedance of about  $1,500\ \Omega$  to achieve the required attenuation. Passing the cable three times into a large bead will provide such impedance (Fig. 11.26).
3. Decrease cable height above ground by at least five times.

### 11.6.2 Fields Radiated by Shielded Pairs or Multiconductor Shielded Cables

The concept of transfer impedance, used for radiated emission modeling of a coaxial cable, is transposable to shielded twisted pairs (STP). However, there is a noticeable difference: the shield is no longer an active return conductor (Fig. 11.39). With balanced interfaces and wire pairs, the current returning by the

shield is only prorated to the percentage of asymmetry in the support [6]. If the transmission link is balanced with  $X\%$  tolerance, the current returning by the shield is, for the worst possible combination of tolerances, only  $X\%$  of the total current in loop impedance  $Z_{EXT}$ . In this case, Equ. (11.11) becomes

$$V_{ext} = X\% [Z_t(/m)\ell V_0/Z_{EXT}] \tag{11.15}$$

As a result, the radiated field is reduced by a factor equal to  $X\%$ , compared to an ordinary coaxial cable situation. Depending on the quality of the balanced link,  $X$  may range from 1 to 10%, with typical (default) value being 5% (good quality, category #5 or equivalent STP). If the wire pairs are interfacing circuits that are not balanced (e.g., the signal references being grounded at both ends), a larger portion of the signal current will use the shield as an alternate return path. This portion is difficult to predict. At worst, this unbalanced configuration cannot radiate more than the coaxial case.

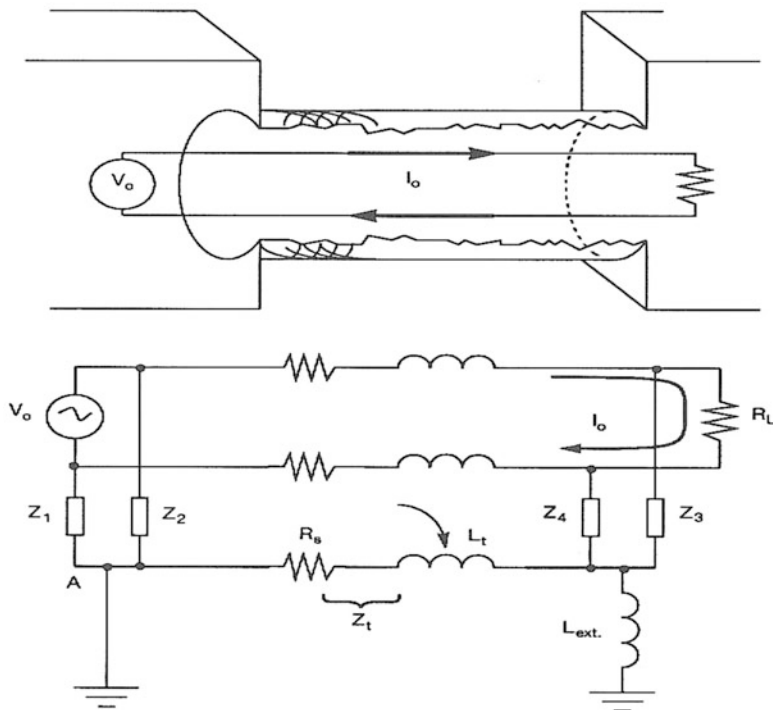


Fig. 11.39 Radiation from a balanced shielded pair

### 11.6.3 Shielded Flat Cables

One specific case of shielded multiconductor cable is the shielded flat cable. A few typical versions are shown in Fig. 11.40. Caption “a” sometimes advertised as “shielded,” is merely a flat cable with an embedded ground plane. Although offering some advantages, its reduction is often insufficient because CM current can still flow on the single-side foil edges and radiate. The caption (b), also marketed as “shielded” is leaky at HF due to the long, unclosed seam that runs over the entire length. The drain wire is acceptable as a low-frequency shield connection, but absolutely inadequate at HF. Caption c, d deserve to be called “shielded” as the shield totally encircles the wires. However, with (c), because there is no access to outer metal surface, 360° bonding is not easily made, and the drain wire is still there.

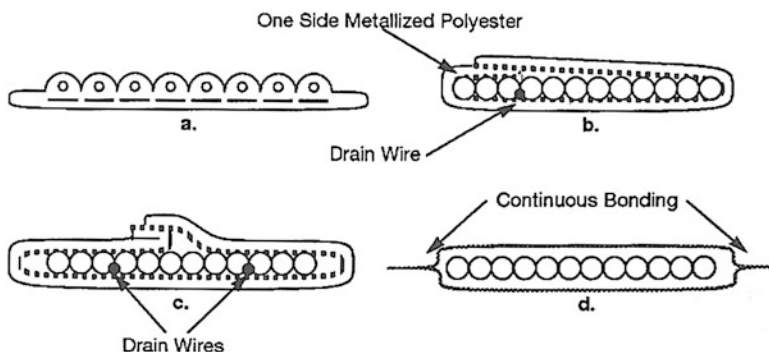


Fig. 11.40 Various shielded flat cable configurations (source: [11])

Figures 11.41 and 11.42 (from [11]) shows some results of radiated EMI measurements from flat cables carrying high-speed digital pulses. It is clear that no cable carrying clock pulses faster than 10 MHz with <10 ns rise time can meet Class B limits without having a 360° shield (unless the signal is cleaned up by other methods, such as ferrites, I/O filtering, balancing, and so on).

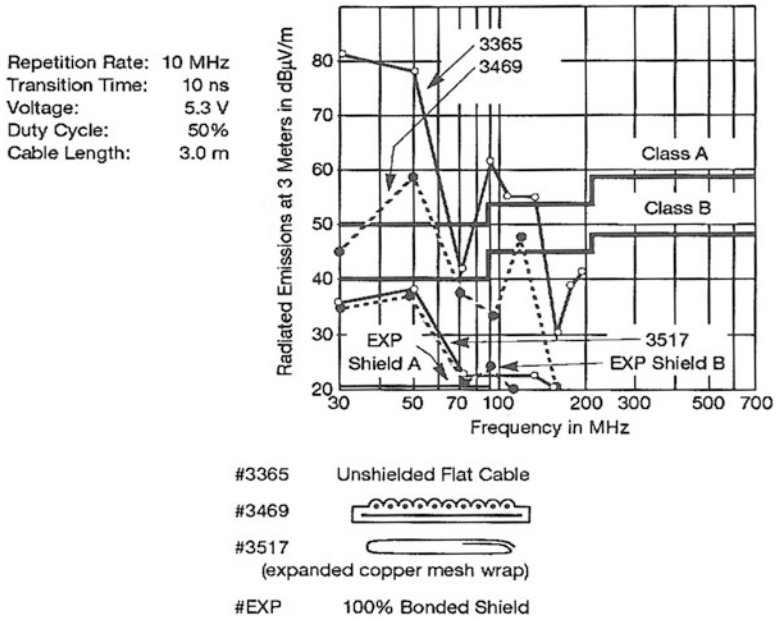


Fig. 11.41 Comparison of radiated levels from different flat cables [11]

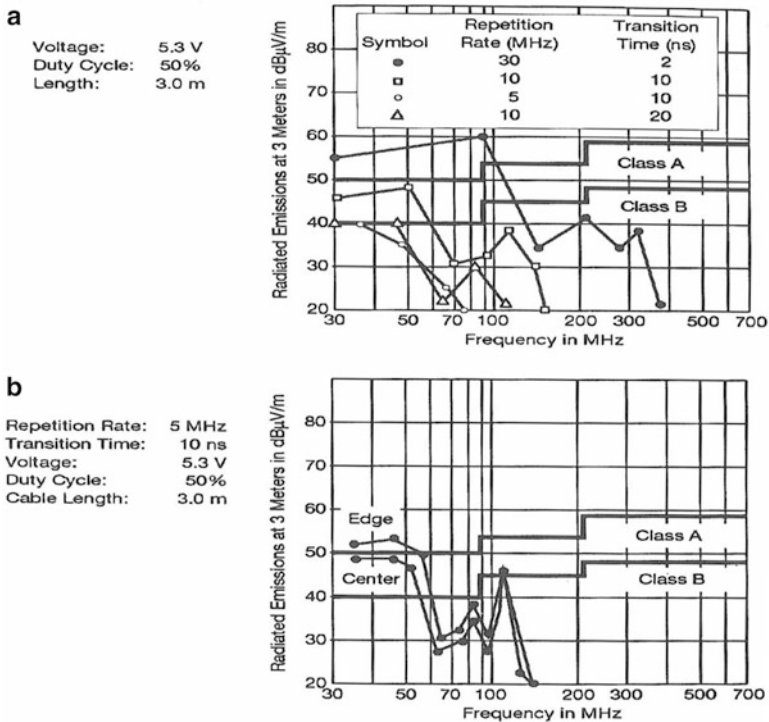


Fig. 11.42 Radiated levels from different signals and conductors location (Source: 3 M, [11]). (a) Effect of clock rate and transition time on radiated field (cable #3517, edge connector). (b) Effect of conductor location (#3469)

### 11.6.4 Importance of the Shield Connections

As important as a good shield with low  $Z_t$ , its low-impedance termination to the equipment metal boxes must be insured [4]. Figure 11.43 shows that connection impedance  $Z_{ct}$  is directly in the signal current return path, in series with  $Z_t$ . Therefore,  $Z_{ct}$  can strongly increase the voltage  $V_{ext}$ , which excites the cable-to-ground radiating loop. The following values can be taken for typical transfer impedances of *one*-shield end connection:

	DC to 10 MHz	100 MHz	1,000 MHz
$Z_t$ , BNC connector (m $\Omega$ )	1-2.5	5	30-100
$Z_t$ , <i>N</i> connector (threaded) (m $\Omega$ )	<0.1	0.03-1	0.1-5
$Z_t$ , SMA connector (threaded) (m $\Omega$ )	<0.05	1.5	3
Ordinary multicontact connector (metal case, sliding, non-threaded) (m $\Omega$ )	10-50	70	300
Pigtail, 5 cm	$Z_t \approx 3 \text{ m}\Omega + j 0.3 \Omega \times F(\text{MHz})$		

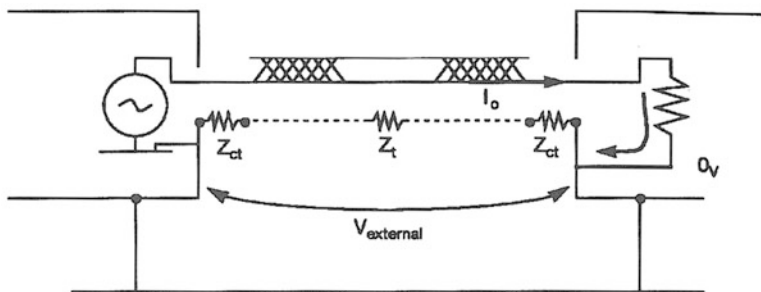


Fig. 11.43 Contribution of shield connections impedance  $Z_{ct}$  to the global effectiveness

**Example 11.9** Referring back to Example 11.8, find the radiation increase if the cable shield was terminated by 2.5 cm pigtails, one at each end.

The new value of  $Z_t$  to use in the calculations of factor  $K_r$  would be  $[Z_t \text{ cable } (\Omega/\text{m}) \times \ell + 2Z_{ct}]$ . Calculations results are shown below:

	15 MHz	45 MHz	150 MHz
$Z_t$ , 2 m cable only	0.3 $\Omega$	1 $\Omega$	1.5 $\Omega$ ( $\lambda/2$ limit)
$Z_{ct}$ , two pigtails	4.5 $\Omega$	13.5 $\Omega$	45 $\Omega$ (only one pigtail)
Previous $Z_t$ (dB $\Omega$ )	-10	0	0
New $Z_t$ (total dB $\Omega$ )	14	23	33
$Z_t$ increase, $\Delta$ dB	24	23	29

The pigtail impedance alone represents  $\approx 15$ -30 times the cable shield transfer impedance. The radiated field will increase by the same amount as the  $Z_t$  increases. Any attempt to solve the problem by using a better shield will be for naught, as the pigtails are the problem.

Figure 11.44 shows another frequent cause of cable shield inefficiency: an internal pigtail picks up PCB radiation and drives the resulting current over the shields, causing them to radiate. Fixing this simple detail can produce a 20 dB reduction in the radiated



emission level. Obviously, it is vital that a cable shield be terminated by a low-impedance connection (lower than  $\ell \times Z_t$  of the cable itself). Most connector styles are now available in shielded versions, allowing a 360° contact on the braid (see Fig. 11.45).

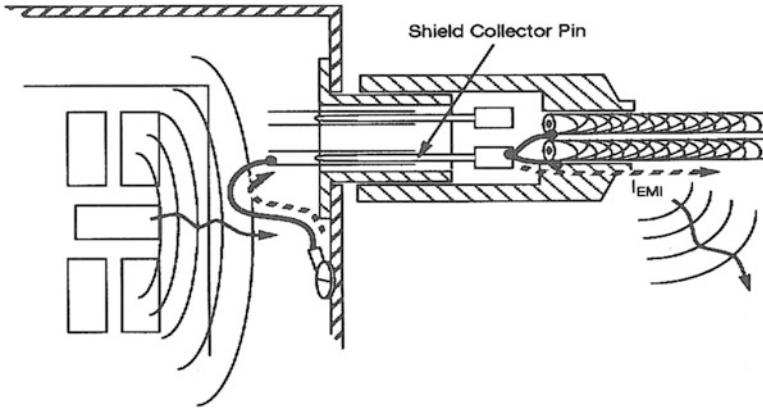


Fig. 11.44 External radiation of cable shields caused by internal pigtail

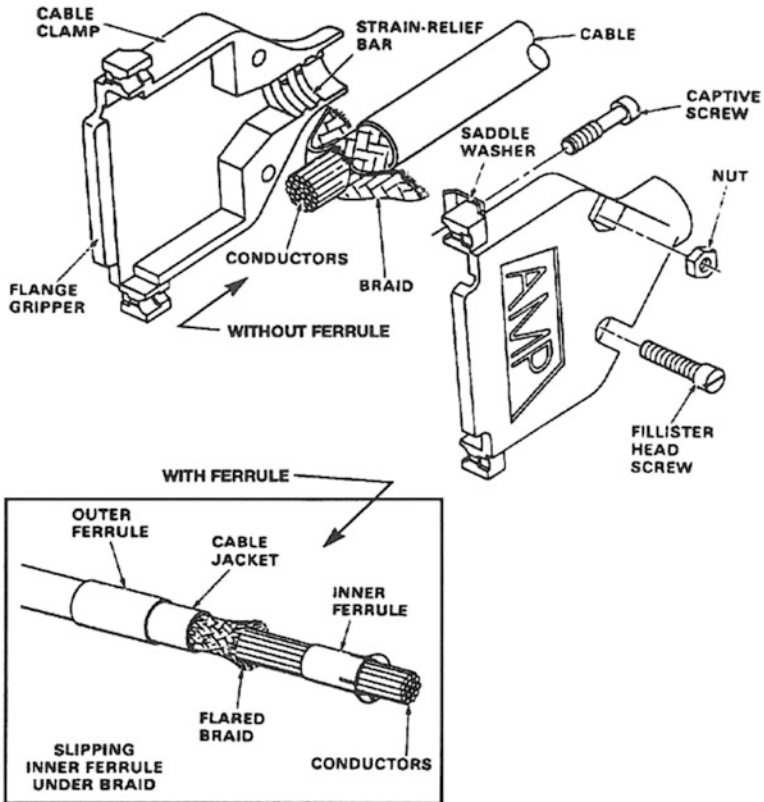


Fig. 11.45 Commercial shielded connectors with low- $Z_t$  shield connection (courtesy of AMP, Harrisburg, PA)

### 11.6.5 Specifying $Z_t$ from a Given Shielding Effectiveness Objective

At the first gross estimate of EMC requirements for a system, hardening is often presented in terms of shielding effectiveness (SE). Therefore, it would be interesting to be able to grade the cable hardening in the same terms as the box/enclosure hardening. Although comparison is not totally rigorous, the shield reduction factor  $K_r$  described previously allows a correlation of  $Z_t$  with SE.

**Example 11.10** The following requirements have been set for system radiation containment:

SE > 50 dB at 10 MHz, and > 60 dB at 100 MHz

The cable length is 2 m, termination resistance  $Z_L = 50 \Omega$

Using Eqs. (11.13) and (11.14) and assimilating  $K_r$  to SE(dB):

*Below 75 MHz ( $\ell < \lambda/2$ ):* SE =  $20 \log(1 + 6 F(\text{MHz})/Z_t)$

For 10 MHz, the condition translates as 50 dB =  $20 \log(1 + 6 \times 10/Z_t)$ .

Solving for  $Z_t$ , via the antilog:  $10^{50/20} = 1 + 60/Z_t$ ; hence  $Z_t < 0.2 \Omega/\text{m}$  at 10 MHz.

*Above 75 MHz ( $\ell > \lambda/2$ ):* SE, at worst-case resonances =  $20 \log(1 + 300/L_t)$  from Equ. (11.14)

Therefore, at 100 MHz the condition translates as 60 dB =  $20 \log(1 + 300/L_t)$ .

Solving for  $L_t$ :  $1,000 = 1 + 300/L_t$ ; hence  $L_t < 0.3 \text{ nH/m}$  corresponding to an optimized single braid.

These data can serve as a cable shield selection guideline. The 10 MHz requirement is compatible with a standard single-layer braid (see  $Z_t$  on Fig. 11.33). The 100 MHz requirement for transfer inductance  $L_t$  requires an optimized single braid, with tighter braid coverage, or a foil + braid arrangement. A double braid would be unnecessary. Notice that the shield connections impedance is included in this  $Z_t$  objective.

## 11.7 DISCUSSION REGARDING SHIELDED VS. UNSHIELDED TWISTED PAIRS

There has been a continuous controversy regarding the possibility of using unshielded twisted pairs (UTP) for high-speed data links inside buildings, without resorting to more expensive STP.

Based on measured data, as well as cable CM radiation models of Chap. 2, we have seen that in the 30 to 200 MHz range, a 20 to 25 dB reduction factor was needed for an ordinary wire pair to satisfy FCC Class B. If, instead of the typical 10-30% unbalance of an ordinary single-ended link, a differential link with a high-grade UTP is used, a total 2% unbalance can be achieved, meeting the 20 dB reduction goal. The same goal could also be achieved with the help of balancing transformers (see Sect. 11.2).

Furthermore, it is true that the normal symmetry with an STP cable is slightly inferior to that of the same cable in UTP version; this is due to the fact that a perfect geometry of two wires twisted inside a shield is more difficult to control: a 0.05 mm unevenness in a 0.5 mm dielectric thickness results in 10% asymmetry of each wire-to-shield capacitances and inductances (impedances  $Z_1/Z_2$  and  $Z_3/Z_4$  in Fig. 11.39). High-grade, Class 5 UTP with  $\leq 2\%$  unbalance are available, while the corresponding STP version exhibits  $< 3\%$ . In addition, symmetry impairment is frequently aggravated by mediocre practices for shield continuity in building wiring. Therefore, many articles exist, suggesting substantial savings by not using STP. But radiated emission is not the only EMC constraint. In industrial sites, hospitals, or high-rise commercial buildings, immunity to RF fields of 10 V/m and to Electrical Fast Transients requires 30-40 dB of added CM protection, which even higher-grade UTP cannot provide. Thus, on the basis of immunity STP is often preferred in harsh environments.

## 11.8 ELIMINATING CABLE RADIATION BY FIBER OPTICS

Optical fibers, besides their low loss, smaller cross section, and wider bandwidth, offer total EMI isolation, since they neither emit nor pick up electromagnetic fields. Replacement kits are available for most standard (RS 232, RS 422, USB, etc.) digital interfaces. So, when affordable and compatible with other ambient constraints, fiber optics are the ultimate answer to I/O cable EMI reduction.

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# Chapter 12

## Principal Radiated Emission Specifications and Test Methods

This chapter is intended to make available only the essential radiated EMI limits as a complement to the design information provided in this book. These excerpts by no means constitute an acceptable substitute to the official texts, and any reader who is actually involved in testing should use the formal specification documents instead.

All radiated emissions specifications share several characteristics in that they define:

- A receiver bandwidth(s) and detection mode
- A test distance and types of antennas
- A typical arrangement of the test instrumentation and equipment under test (EUT)

### 12.1 MIL-STD-461

MIL-STD-461, presently at Rev. F, is still one of the most widely used EMC standard. It is a complete, tri-service document applying to the Army, Navy, and Air Force. As of 2013, it is undergoing its 5 year review.

The upcoming Rev. G will include additional tests like indirect lightning effects and ESD. Information on updates will be found on <http://dlsemc.com/crebd>.

Since Rev. D (issued in 1993), noteworthy changes were introduced, a major one being the deletion of the NB/BB segregation, which resulted in a single set of emission limits. Also, instead of the ten independent chapters repeating numerous limits and curves for each equipment category (as was the case in former issues), the standard is grouping them into generic curves. The limits are generally identical to, or less severe than former, “pre-D” versions up to 1 GHz, becoming progressively more severe above.

The various test methods and setup, which up to Rev. D, were described in a different document MIL-STD-462 have been combined with the limits in the main body, making the practical use of the standard extremely handy, avoiding

redundancies and duplications. A comprehensive matrix indicates which type of test is required according to the location and use of each category of equipment or subsystem:

- Equipment and subsystems in surface ships
- Equipment and subsystems in submarines
- Equipment and subsystems aboard Army aircrafts
- Equipment and subsystems aboard Navy aircrafts
- Equipment and subsystems aboard Air Force aircrafts
- Equipment and subsystems installed in spacecraft and launch vehicles, including associated ground support equipment (GSE)
- GSE for Army
- GSE for Navy
- GSE for Air Force

Tests are broken down into conducted emissions (CE), conducted susceptibility (CS), radiated emissions (RE), and radiated susceptibility (RS). With respect to the RE family of tests, different limits are specified according to the installation location and branch of service. Figure 12.1a, b shows two of the most often quoted radiated limits, corresponding to the most severe categories. Only a few limits are shown here, for illustrative purpose, and the reader should refer to the original documents for practical applications.

### ***12.1.1 RE101: Magnetic Field, Narrowband (NB), 30 Hz to 100 kHz***

Test distance: 7 cm

Antenna: magnetic loop, diameter 13.3 cm, 36 turns with electrostatic shield and a 5-10  $\Omega$  DC resistance.

Suggested receiver bandwidth (6 dB):

10 Hz from 30 Hz to 1 kHz

100 Hz from 1 to 10 kHz

1 kHz from 10 to 100 kHz

The limit is given in dBpT (picoTesla), a rather cumbersome unit, but it has to follow the standard unit for magnetic induction, that is, the Tesla or its submultiple. In practical EMC units, the dBpT is converted into its equivalent  $H$ -field value in air: 0 dBpT = -2 dB $\mu$ A/m. The test practice requires that the loop be oriented for maximum reading on each of all EUT faces and connectors. Only equipment intended for use in critical magnetic ambients (e.g., Navy, antisubmarine warfare) are subject to this very severe specification.

One must notice that for its entire frequency range, this test is in a very near-field condition, where the  $H$  field varies by  $1/D^3$ . Because of such close distance, some equipment containing magnetic elements like transformers, solenoids, inductors,

including those used in EMI filters, etc. can easily cause a limit violation, even with a decent box shielding (remember, near-field shielding effectiveness of metal barriers is generally poor against  $H$ -field sources). The procedure includes some sort of escape door if the limit is exceeded at 7 cm. Keeping the loop oriented for maximum reading, the antenna can be progressively moved away until the limit is satisfied. The *test is not considered successful*, yet the compliance distance must be recorded, such that the procuring authority can eventually consider a waiver.

### **12.1.2 RE102: Electric Field (NB and BB), 10 kHz to 18 GHz<sup>1</sup>**

Test distance: 1 m

Antennas:

Vertical monopole, 1.04 m (10 kHz to 30 MHz)

Biconical (30-200 MHz),  $V$  and  $H$  polarization

Double ridged horn above 200 MHz (log periodic is not allowed),  $V$  and  $H$  polarization

Required receiver (6 dB) bandwidth:

1 kHz from 10 to 150 kHz

10 kHz from 150 kHz to 30 MHz

100 kHz from 30 MHz to 1 GHz

1 MHz above 1 GHz

Detection mode: Peak

These bandwidths are provided as a good trade-off between test duration and receiver sensitivity. The prescribed 6 dB bandwidth (instead of the 3 dB BW commonly used in other disciplines) is close to the receiver's impulse bandwidth, allowing for a more standard capture of broadband contents of the measured signal. It also facilitates a comparison with civilian type of emission measurements like FCC or CISPR, provided appropriate distance and cables height corrections are made.

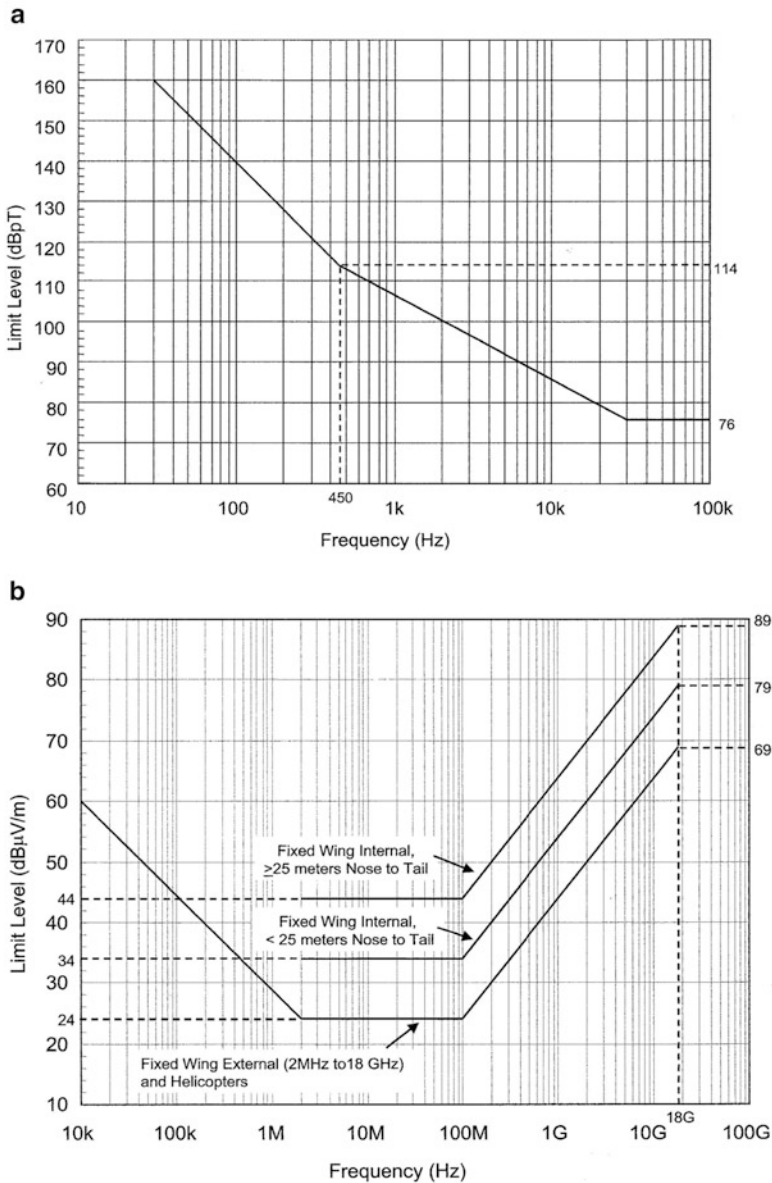
Although the need for NB/BB discrimination does not exist anymore, other bandwidths can be used, for instance:

- Narrower bandwidth for investigative analysis requiring a better receiver sensitivity/selectivity
- Larger bandwidth for speeding up the frequency sweeps

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<sup>1</sup>In practice, the upper frequency is limited to 1 GHz or ten times the highest intentional EUT operational frequency, whichever is the highest.

In any case, for the formal reporting, only specified bandwidth should be used, since the single NB/BB limit implies a strict respect of the standard bandwidth. The annex states very clearly that “Larger receiver bandwidths may be used; however, they may result in higher measured levels, for which NO BANDWIDTH CORRECTION FACTORS SHALL BE APPLIED TO TEST DATA.”

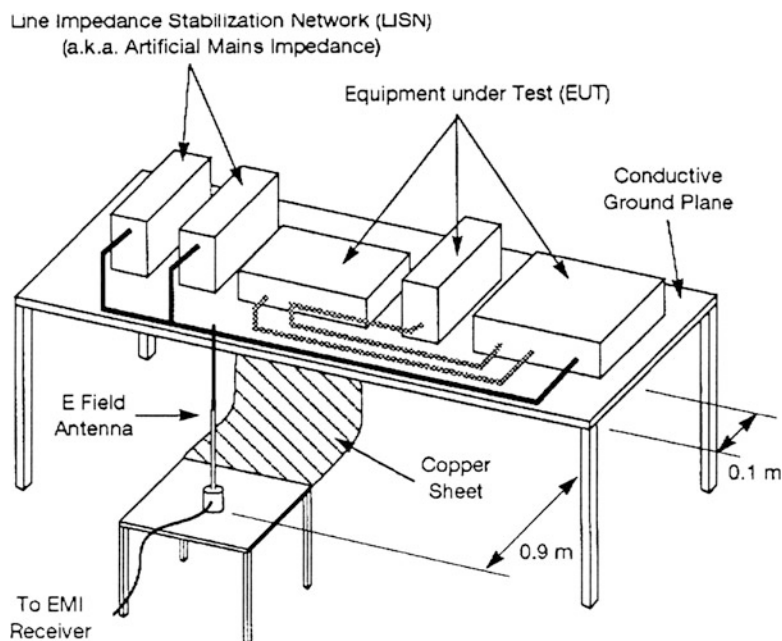


**Fig. 12.1** (a) RE101 radiated magnetic field limit of MIL-STD-461F. (b) RE102 radiated emission limit of MIL-STD-461F (only the most severe curves shown)



The EUT is installed as shown in Fig. 12.2. One important feature of MIL-STD-461 testing is that cables are laid at a fixed height (5 cm) above a copper ground plane. This is a good practice for test repeatability, but it can give optimistic results when compared with an actual equipment installation where, for example, cables are routed higher than 5 cm above a metallic structure, or without any metallic structure nearby.

The vertical rod antenna setup has been a cause of controversy with the copper sheet connecting the antenna ground plane to the test bench ground plane. The latest setup of MIL-STD-461 Rev. F recommends not using the copper sheet and arranging a vertical chute of the coaxial cable that must be firmly bonded to the metal floor with an elbow bracket and fitted with a lossy (low-inductance) ferrite toroid providing  $\geq 20 \Omega$  of damping resistance at 20 MHz.



**Fig. 12.2** Radiated emission test setup, per MIL-STD-461 or RTCA/DO-160. *Left:* rod antenna with copper foil connection as per MIL-STD-461 up to Rev. E. *Right:* MIL-STD-461F rod antenna setup with vertical cable chute and ferrite

### **12.1.3 RE103 Radiated Emissions, Antenna Spurious, and Harmonic Outputs, 10 kHz to 40 GHz (Only for Equipments with RF Functions and Antenna Output)**

This test which is meant to verify that no undesired radiated emissions emanate from the EUT, other than the intended signal at the carrier frequency. Although it is part of the RE family, this test is an alternative for CE106 when testing a transmitter with

the actual antennas used in installations (e.g., a transmitter with non-removable antenna). RE103 is often replaced by the CE106 conducted version that is faster and easier to perform directly on the antenna port.

## 12.2 CISPR INTERNATIONAL LIMITS, TEST INSTRUMENTATION AND METHODS

Outside the military and aerospace domains, whether they are:

- Recommended in a given industry
- Legally enforced in a given industry
- Legally enforced in a group of nations, such as the European Community

the radiated emissions specifications generally correspond to the CISPR recommendations (see Chap. 1), endorsed internationally by the International Electrotechnical Commission. Also, the Class B/A distinction (residential vs. industrial and commercial use) is common to most CISPR-derived civilian standards.

This is particularly the case with the few limits described herein for US FCC regulations, Canadian regulations, European Norms (ENs), or Japanese Voluntary Council for the Control of Interference (VCCI) standards. Although there can be some variation in the limit values, the measurement methods correspond to those of CISPR publications #13, 16, and 22<sup>2</sup> which can include the following instrumentation and methodology:

- Receivers must conform to CISPR Publication 16, including a 6 dB bandwidth of
  - 9 kHz for  $0.15 < F < 30$  MHz
  - 120 kHz for  $30 < F < 1,000$  MHz
  - 1 MHz for  $F > 1,000$  MHz
- Use of average and quasi-peak detection for conducted and radiated emissions measurements up to 1,000 MHz and peak plus rms-average above 1 GHz.
- Use of a 10 m measuring distance (or 3 or 30 m in some cases, with a  $1/D$  correction factor).
- Use of a calibrated open-area test site or, as a substitute, a semi-anechoic chamber whose result can be correlated to a calibrated open area. Since the year 2000, proposals were made for the use of a fully anechoic chamber, recreating free-space, eliminating the tedious vertical antenna scan, provided a corresponding -5 dB reinforcement of the limit. This was not officially accepted.
- Laying the I/O cables in a typical customer arrangement but trying to reproduce a realistic worst-case scenario for the first 1.50 m of cable-e.g., a vertical cable drop of 80 cm for tabletop equipment.

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<sup>2</sup>However FCC and Canada use ANSI methods which differ slightly from CISPR, particularly above 1 GHz.

- Searching for maximum field reception by *all the following*:
  - Using the horizontal and vertical polarization of antennas
  - Moving antenna height from 1 to 4 m to search for maximum ground reflection (see other option above)
  - Rotating the EUT 360° to find the worst emission pattern (or moving the antenna around the EUT)

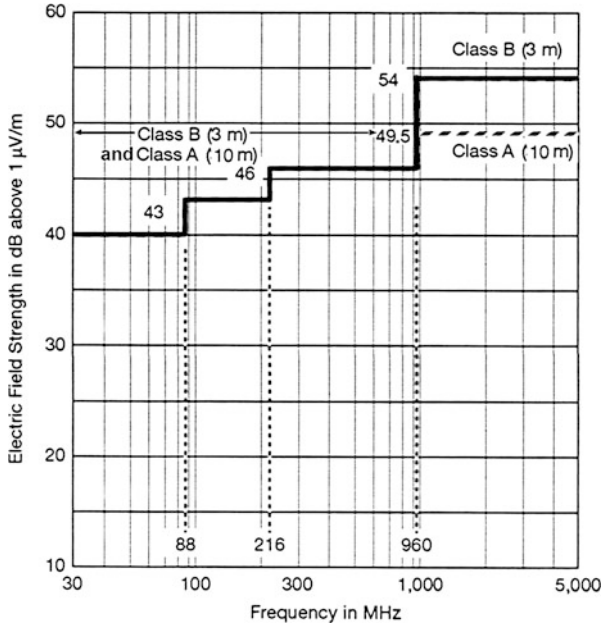
The quasi-peak detector, plus the fixed bandwidth, allows for no distinction between BB and NB signals, thus avoiding the need of a double limit. The limit is designed to protect adequately against both types of interference. However, even if in principle the issue has been eliminated by the single limit, there still remains some NB/BB problem, as explained next.

Given that the quasi-peak detector is imposing a very slow-frequency scanning, most EMC labs will run the sweep using a peak detection to speed up the test. Since EMI receivers are calibrated for displaying the rms value of a sine wave, in case of a NB interference the peak-mode detection will produce the true rms value of the NB sine wave. If the emissions level measured with peak detection is below the limit, the tested equipment is compliant, and no further verification is needed. If the limit is exceeded at one or few frequencies, a second chance is given by making a slow scan around the frequency of concern, in quasi-peak mode. If the limit is met, the EUT is regarded as compliant. This is nothing else than admitting that there is in fact a limit relaxation allowed by the use of the QP detector, the time constants of which automatically “de-penalizes” the BB interference (see Chap. 3, Sect. 3.2). A current application of this is the spread spectrum clocks that can result in a -2 to -7 dB reduction in the radiated emissions readings.

## 12.3 FCC PART 15 SUBPART B AND INDUSTRY CANADA

FCC Part 15-B applies to electronic data processing equipment. The radiated emission limits for Classes A and B digital devices are shown in Fig. 12.3. The FCC had anticipated a trend toward increasing clock speeds by extending theoretically the limit up to 40 GHz. However, measurements above 1 GHz are conditioned on the highest operating frequency of the device (see FCC frequency Table below). The EUT must be operated using the maximum configurations of hardware and software options, and at least one sample of each attachable peripheral devices.

FCC frequency range	
Highest frequency generated or used in device	Upper frequency of radiated measurement
Below 1.705 MHz	No radiated testing required
1.705-108 MHz	1 GHz
108-500 MHz	2 GHz
500 MHz-1 GHz	5 GHz
Above 1 GHz	Fifth harmonic of the highest frequency or 40 GHz, whichever is lower



**Fig. 12.3** Radiated FCC Part 15-B limits, for EDP equipment. Up to 1 GHz, receiver (6 dB) bandwidth is 120 kHz, with quasi-peak detection. The limit extension above 1,000 MHz applies only to equipments using clock frequencies >108 MHz. Officially, measurements can be required up to 40 GHz

### 12.4 CISPR 32

Almost similar to FCC, the radiated emission limits for Classes A and B digital devices (termed “information technology equipment” in typical bureaucratic parlance) are shown in Fig. 12.4. These limits are close (within 2 dB, accounting for proper 1/D distance factor) to FCC 15-B and the test setup is similar. In 2005, CISPR 22 introduced an amendment which extended its limits above 1 GHz, to protect satellite and cellular telephone bands. The limits extension up to 6 GHz are conditioned on the highest operating frequency of the device (see CISPR frequency table next).

	1-3 GHz	3-6 GHz
Class B limits average/peak (dBμV/m)	50/70	54/74
Class A limits average/peak (dBμV/m)	56/76	60/80

- Measuring distance: 3 m for both A and B categories
- Antenna height: fixed, 2 m (default value) or adjusted depending on EUT size

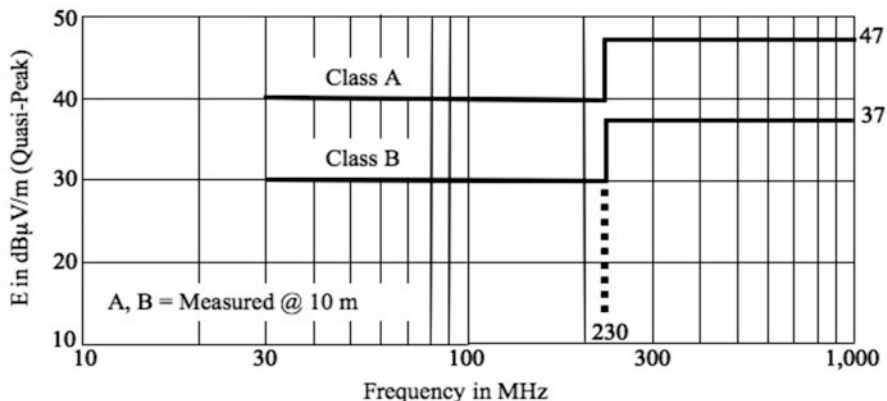


Fig. 12.4 Radiated limits of CISPR 22 (or EN 55022). Although 3 m distance test is commonly made for practical reasons, official distance for class B is 10 m

CISPR frequency range	
Highest frequency generated or upper frequency of used in device	Upper frequency of radiated measurement
Below 108 MHz	1 GHz
108-500 MHz	2 GHz
500 MHz-1 GHz	5 GHz
Above 1 GHz	Fifth harmonic of the highest frequency or 6 GHz, whichever is lower

## 12.5 EN 55014/CISPR 14

These limits are mandatory for “non-intentional RF sources,” defined as electric/electronic devices not using operating frequencies above 9 kHz. They cover household appliances with motors, dimmer switches, fluorescent lights, and so forth, basically BB sources (as perceived with a 9 or 120 kHz receiver BW). The limit from 30 to 230 MHz is 30 dBµV/m at 3 m, changing to 37 dBµV/m from 230 to 1,000 MHz.

For small equipment (i.e., box size less than 1 m), a simpler method for radiated emission assessment is permitted. Instead of measuring actual field strength, the equivalent radiated power is measured using a special current probe called the “absorbing clamp.” The limit is, accordingly, expressed in decibels above a picowatt (dBpW). Interestingly, there is an approximate relationship between the dBpW and the actual field at 3 m. Between 30 and 300 MHz, this relationship is

$$E(\text{dB}\mu\text{V}/\text{m}) = P(\text{dBpW}) + 20 \log(F(\text{MHz})/200)$$

Because the EC/EMC directive requires non-interference, it is recommended, for EUT using digital circuits, that actual radiated emissions be checked for high clock frequencies.

## **12.6 JAPAN VOLUNTARY COUNCIL FOR THE CONTROL OF INTERFERENCE**

The Japanese VCCI limits for EDP equipment are exactly the same as CISPR 22, for Classes A and B.

## **12.7 CISPR 32 EMISSION, MULTIMEDIA EQUIPMENT**

The more recent CISPR recommendation 32 is expected to replace both CISPR 13 and 22. It covers in a same document, audio, video, home entertainment devices (generally covered by CISPR 13 for radio and TV sets) and information technology equipment (digital data processing equipment) essentially computers and associated peripheral units, ruled so far by CISPR 22. The reason is the growing addition of digital radio/video devices integrated into PCs or entertainment devices, plus the low-power, short-distance wireless links like Bluetooth. This standard (first released in 2006, current Rev. 2012) is now endorsed by the European CENELEC at the time of this writing.

The standard keeps the same A and B classification as CISPR 22/FCC 15 for residential vs. nonresidential use. It includes a very complete review of all types of I/O ports: RF antenna, AC input, DC input/output, Ethernet, analog, etc. with the corresponding (conducted) measurement setups and limits for each. As sometimes is the case with emission standards, the cable-conducted limits are not fully coherent with radiated emission limits. In other words, a successful conducted emission test with under-the-limit results around 30 MHz could give a false sense of security that the product will comply with RE limits around 30 MHz. In fact, it will probably not. Radiated emission limits are similar to CISPR 22, with QP and average detector modes. It is extended to 6 GHz, plus specific requirements for RF reception circuits like local oscillator harmonics, harmonics of local oscillator, etc. (if the EUT has such features). The procedures for maximum worst-case configuration, pre-scan, and maximum searching are precisely defined and as such time-consuming.

## 12.8 FCC PART 18 AND EN 55011 (CISPR 11)

These regulations cover ISM high-frequency generators (see discussion in Chap. 2) such as:

- Industrial heating systems
- Medical diathermy equipment
- Ultrasonic devices
- Microwave ovens
- Plasma generators
- RF-operated lamps

Due to the operational nature of such devices, a certain number of frequencies have been allocated to them, within which they are permitted to radiate without any restrictions. These are the following:

6.78, 13.56, 27.12, 40.68, 915 MHz  
2.45, 5.8, 24.125, 61.25, 122.5 GHz

Outside of these authorized fixed frequencies, specific emission limits are required for:

1. General requirement for RF power-operated devices Class B (residential) and industrial environment
2. RF industrial heaters (for instance, FCC limit is 10  $\mu\text{V}/\text{m}$  at 300 m)

Since new categories of industrial and medical applications of RF power are constantly appearing, new limits are issued accordingly. The reader is invited to review the FCC or European Norms for the most current limits.

## 12.9 CISPR 25, AUTOMOBILE ELECTRONICS

In order to prevent RF interference caused by onboard electronics from adversely affecting the operation of vehicular onboard radio receivers, stringent RF emission limits are recommended by CISPR 25 (see Clause. 1). Different performance classes (levels being agreed upon by the purchaser and the supplier and documented in the test plan) are provided. Unlike the recent trend in MIL-STD-461 emission requirements, CISPR 25 still calls for compliance with both NB and BB limits. Table 12.1 shows the radiated NB and BB limits for Class 4 electronic modules, the one which is most used for passenger cars.

Note: Because of the potential for close proximity of components or harnessing location in a vehicle, a product may meet a particular limit requirement at the component level and still have problems at the vehicle level.

**Table 12.1** CISPR 25 limits (2008 update) for Class 4 radiated emissions

	EdB $\mu$ V/m		
	NB	BB	R <sub>CVR</sub> BW
Frequency (MHz)			
0.15-0.3	36	56	9 kHz
0.5-1.8	28	48	9 kHz
5.9-6.2	26	46	9 kHz
26-108	24	41	120 kHz
174-230	28	38	120 kHz
468-944	37	47	120 kHz
Frequency (GHz)			
1.5-1.6 (GPS)	24	34	1 MHz
1.56-1.58	16	NA	1 MHz
1.8-1.99 (GSM2)	30	50	1 MHz
2.4-2.5 (Bluetooth)	30	50	1 MHz

Field measured at 1 m. NB limits are average detector values, and BB limits are peak values. When measured in quasi-peak, peak limit is reduced by 13 dB

## 12.10 RTCA/DO-160

This standard, published by the US Radio Technical Commission for Aeronautics, applies to equipment used aboard civilian aircraft. The RTCA is responsible for specifying tests that meet US Federal Aviation Administration (FAA) and other international regulations covering electronic equipment installed on any civilian aircraft, from small private aviation models up to transoceanic airliners. The updating of DO-160 is coordinated with RTCA's twin organization EUROCAE, so that this standard can be regarded as a worldwide accepted document.

DO-160 includes 26 sections, but only eight of them (#15-25) deal with EMC, the rest of the document dealing with other environmental effects: vibrations, temperature, power quality, etc. Part 21 "emission of RF energy" describes test methods (similar to those of MIL-STD-461) and limits. In the current Rev. G (issued in 2010), *emission limits include six severity grades*, according to the location of the equipment and its potential interfering effect on onboard RF receivers. From less critical to the most critical, these are B, L, M, H, P, and Q. Category B applies to areas with moderate interference control needs, while the requirements become progressively more severe, up to categories P, Q for locations in direct view of receiving antennas, typically outside the aircraft fuselage, or in nonmetallic hulls (for instance, helicopters), and receiving sensitive, vital RF signals (GPS, navigation aids, etc.). Since Rev. D (issued in 1997), as for MIL-STD-461 evolution, subsequent updates have deleted the double NB/BB limits, being replaced by a one-limit/one-bandwidth approach. Although the



measurements methods are quite similar to those of MIL-STD, some very important differences are worth noticing:

- Radiated emissions (RE) measurements now start at 100 MHz (Fig. 12.5), no field measurements being made below 100 MHz.
- DO-160 RE limits are 15-20 dB more permissive than MIL-STD-461 ones, for approximately equivalent categories.
- Conducted emissions (CE) measurements extend up to 152 MHz, a rather unprecedented range for conducted emissions requirements.

Although conducted limits seem to be out of scope in this book on radiated emissions, they are in fact strongly related. We have shown in our emission models and numerical examples that radiated emissions are often dominated by those due to the common-mode currents on interconnecting cables (see Chap. 2, Sects. 2.2 and 2.5 and associated numerical examples). The following example will show that there is some correlation between the CE and RE limits of DO-160:

For categories  $P$ ,  $H$ , and  $Q$ , the RE curve is quite severe in the 108-152 MHz range, with a 25 dB $\mu$ V/m limit (i.e., 18  $\mu$ V/m) at 108 MHz. Given that:

- For 1 m distance, a frequency of 108 MHz puts the EUT in far field.
- The 1.50 m cable length is  $\geq \lambda/2$  condition.

We can use far-field equations like Equ. (2.28), applying the height correction factor for the 0.05 m elevation above ground plane (Chap. 2, Fig. 2.15, and Equ. (2.29)):

$$E \text{ (}\mu\text{V/m)} = (60 I(\mu\text{A})/D) \times (10h/\lambda)$$

Replacing  $\lambda$  by  $300/F(\text{MHz})$  and entering the height  $h = 0.05$  m:

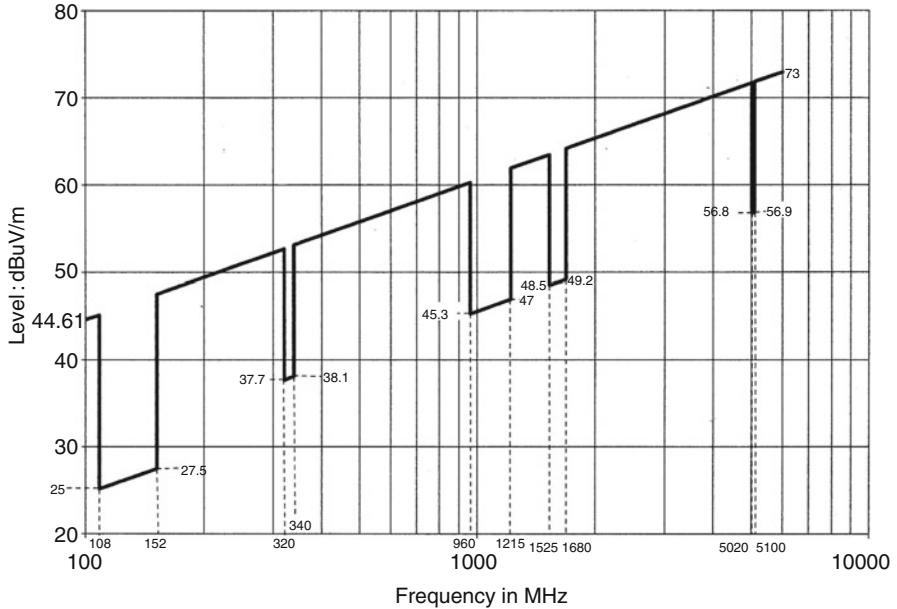
$$E \text{ (}\mu\text{V/m)} = (60 I(\mu\text{A})/D) \times (10 \times 0.05F/300)$$

Replacing  $E$  by the limit value and solving for  $I(\mu\text{A})$ , we obtain

$$I_{\text{CM max}} = 18 \times 300 / (60 \times 0.5F) = 16 \mu\text{A}, \text{ that is } 24 \text{ dB}\mu\text{A}$$

DO-160 interconnecting bundle conducted limit for this same category  $P$ ,  $H$ , and  $Q$  is 20 dB $\mu$ A at 108 MHz.

Therefore, the conducted limit provides some guarantee that, up to 152 MHz, the cable radiation should not cause a specification violation.



**Fig. 12.5** Radiated emission limits for civilian aircraft equipment, RTCA/DO-160F and G, most severe categories (*P*, *Q*, and *H*)

## 12.11 RE MEASUREMENTS BY THE REVERBERATION CHAMBER METHOD

The DO-160 Revs. F and G allow for an alternative to shielded anechoic room measurements for both radiated susceptibility (RS) and radiated emissions (RE) qualification testing. The reverberating chamber method that started being used in the early 2000s for susceptibility testing has been officially put into practice for DO-160 radiated emission. The method is an interesting application of the statistical electromagnetic (SEM) discipline that consists in predicting, within a given probability, the maximum value of the radiated field generated by a local RF source in a closed 3D space, accounting for the multipath reflections of a highly resonant enclosure.

The principle is exactly the reverse of an anechoic chamber with absorbing layers: instead of trying to damp the walls and ceiling reflections to an acceptable degree (that relates to an accepted measurement uncertainty), these reflections are enhanced, using a highly reflective enclosure and a rotating paddle, turning the room into a “stirred-mode” reverberating chamber. The measure of the received RF power (and no longer the *E* field), over a certain stirring time, gives a statistical mean of the interference potential of the EUT, given that all possible combinations of additive and canceling reflected waves have been encountered and recorded. Figure 12.6 based on DO-160G shows a simplified view of the procedure.

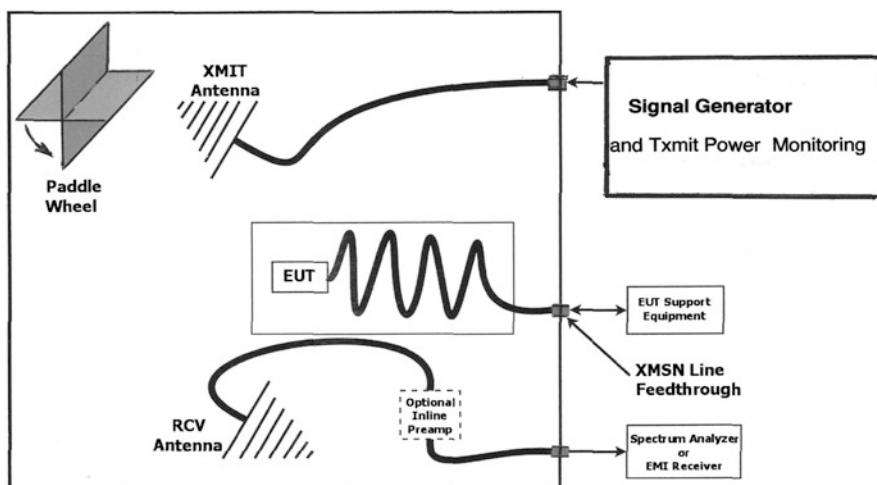
1. First, a calibration of the room is performed, using:

- A transmitting antenna fed by a calibrated RF source
- A receiving antenna in the opposite angle of the room
- The paddle wheel rotating slowly
- The EUT, normally installed but NOT functioning

The received power (dBm) is recorded at the receive antenna. The difference between the known transmitted power at the transmit antenna input and the receive antenna power is *the calibrated path loss of the room, with this EUT in place*.

2. Then, the transmit antenna stays in place unpowered, its feed line being terminated into  $50\ \Omega$ , and the EUT is turned on. The new received power is recorded at the receive antenna. By comparison with the calibration in (1), the actual RF power emitted by the EUT can be found, since the chamber mean multipath loss has been accounted for by the method. A simple formula allows to retrieve the equivalent field in  $\mu\text{V/m}$ .

In terms of controlling the measurement uncertainty, the method is superior to the classical antenna method. In terms of testing cost the method is extremely time-consuming: while the paddle wheel is rotating, 200 EMI receiver sweeps are required for each frequency step, and a new calibration is needed for every different EUT size.



**Fig. 12.6** Radiated emission measurements by the stirred-mode reverberation chamber method. The setup shown is the calibration, with the EUT present but not functioning. For the actual test, the signal generator is turned off, and the EUT is on

# Chapter 13

## Troubleshooting Radiated EMI Problems

Compliance with radiated emission limits of FCC or EEC regulations, or the more stringent levels of MIL-STD-461 and TEMPEST, has always been a difficult challenge for the EMC engineer and a nightmare for the electronic designer. Too often, using a blend of rules of thumb, tradition, and company's homegrown recipes, the designer does his best to have a prototype working unplugged by internal noise problems and then brings it to an EMI test site to "see if it passes." In many cases, it does not, and several redesign and retest iterations are necessary to reduce the radiated spectrum sufficiently. These test iterations are generally costly, even if they are covered in the general "hidden" costs that appear in preliminary financial projections. The method described in this chapter allows the designer to identify and reduce out-of-spec radiations without necessarily having to return to an RFI test site for each trial fix.

### 13.1 CABLE RADIATION VS. BOX RADIATION IN SPECIFICATION COMPLIANCE

In Chaps. 2 and 3, we saw that external cables, via CM excitation and antenna size, generally radiate higher field amplitudes than the box, at least up to 200 MHz, for equipments whose largest dimension is less than 1 m. The circuit areas formed inside the equipment by the PCB traces, the IC modules, power supply wiring, and other internal wiring are several orders of magnitude smaller than those formed by the external cables. Instead of square meters with cables, we are dealing with tens or hundreds of square centimeters internally. However, due to their smaller length, these components reach their first-quarter-wavelength resonance at a higher frequency and may cause specification violations if the box is unshielded, or poorly shielded [1]. In contrast with I/O cables, these internal circuits are generally neither twisted nor balanced, so their excitation is basically DM. This means that, in some

critical frequency ranges (typically at mid-VHF and above), box radiation levels can be close to (only 10 or 20 dB below) cable radiation.

A difficulty arising from this situation is that after having struggled very hard to reduce CM cable radiation by shielding, ferrite loading, balancing, and all the EMC armory, the engineer returning to the test range does not see all the improvement he was expecting. This frustration is even aggravated by the fact that box radiation can illuminate cables that have been “cleaned up” from CM emissions, again turning them into secondary radiators. The method explained next has been developed and proven over time to avoid fruitless cut-and-try iterations [3, 5]. Because schedules are usually tight by the time compliance testing takes place, this is particularly useful.

## **13.2 STRATEGY WHEN A PRODUCT FAILS RADIATED EMISSION TESTS: QUANTIFYING THE DB REDUCTION**

The philosophy behind this method is that one must first try to identify whether the most significant radiation is caused by the external cable(s) or by the equipment box alone. The routine is described in the flow chart of Fig. 13.1. Notice that the method is equally applicable to susceptibility problems. Referring to the first box in the flowchart, we try to gather as much information as possible while the equipment is still on the test site (shielded room, open-field site, anechoic chamber, or whatever). The reason is that test sites and EMC labs are generally busy and are not convenient places to rework PC boards, cables, or mechanical packaging. The progression steps are described in the following paragraphs.

### ***Step 1***

While on the test site, disconnect all external cables from the EUT.

### ***Step 2***

Once all the external cables have been disconnected (excluding the power cord, unless the EUT can be powered from an internal battery), rerun the test and see if the unit passes. This implies, of course, that the unit can be set to run in a stand-alone mode, using self-diagnostic, self-looping, or dummy loads of some sort, such that the EUT is exercised exactly like in its actual operating conditions.

### ***Step 3***

If the answer is “Yes” in decision box A (diamond shaped), this clearly indicates that these cables were the RF carriers. At this point, if necessary, we can take the equipment out of the test area and bring it back to the engineering lab for a more efficient application of EMI fixes.

**Step 4**

If the answer from box A is “No,” we can conclude either one or both of the following:

- (a) The only cable left (the power cord) is radiating.
- (b) The box itself is radiating.

To decide which of (a) or (b) is true, we need to install temporarily, on the test range, a good-quality<sup>1</sup> filter [CM + DM] at the power cable entry on the machine. One could also shield this cable, but the results may be misleading unless this shielding were made perfect by a thick flexible metal sleeve or thick braid, bonded 360° to the EUT, and extending beyond the test area. This is generally difficult to improvise on the spot. By default, if the specification violation occurs beyond about 10 MHz, we can insert one or two large ferrites on the power cable, with several turns on each. Ferrites with the best possible impedance vs. frequency curve must be selected, providing at least 150 Ω at 30 MHz, for one or more turns. The power cord can also be pressed tightly onto the test range ground plane, using conductive or ordinary adhesive tape.

**Step 5**

After doing this, if answer from box B is “Yes,” it is prudent to reconnect the other cables and again check them for radiation while still on the test range. It could be that the power cable radiation, being the dominant coupling mode, was masking some radiation from the I/O signal cables. In this case, some rework will be required in this area as well (as in the “Yes” path from box A).

If the external cables are the culprits (box in the upper right corner of the chart), once the EUT is back in the engineering lab, efficient progress can be made at the workbench by using an EMC current probe. We shall try to filter the I/O ports with filtered connectors, feedthrough filters or ferrites. Shielding the cables is an alternative, paying special attention to a good, integral bonding of the shield to the chassis. One must keep working until the current probe readout shows that, in all the frequency range, the *CM current spectrum has been reduced by the amount (in decibels) by which the radiated limit was exceeded* [2, 3]. This is for the radiated emission case. If it were a test for susceptibility instead, we would use an inverse method by injecting with a current clamp, the same current that was induced during the actual radiated susceptibility of this EUT. In any case, it is almost guaranteed that the equipment will pass after the proper amount of cable hardening has been installed. Rationale for this: Steps #3, 4, and 5 have told us that cables are the major cause.

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<sup>1</sup>“Good quality,” of course, is vague. But the filter must provide a supplementary attenuation that is commensurate with our specification violation in decibels, at least up to the highest frequency at which the unit failed.

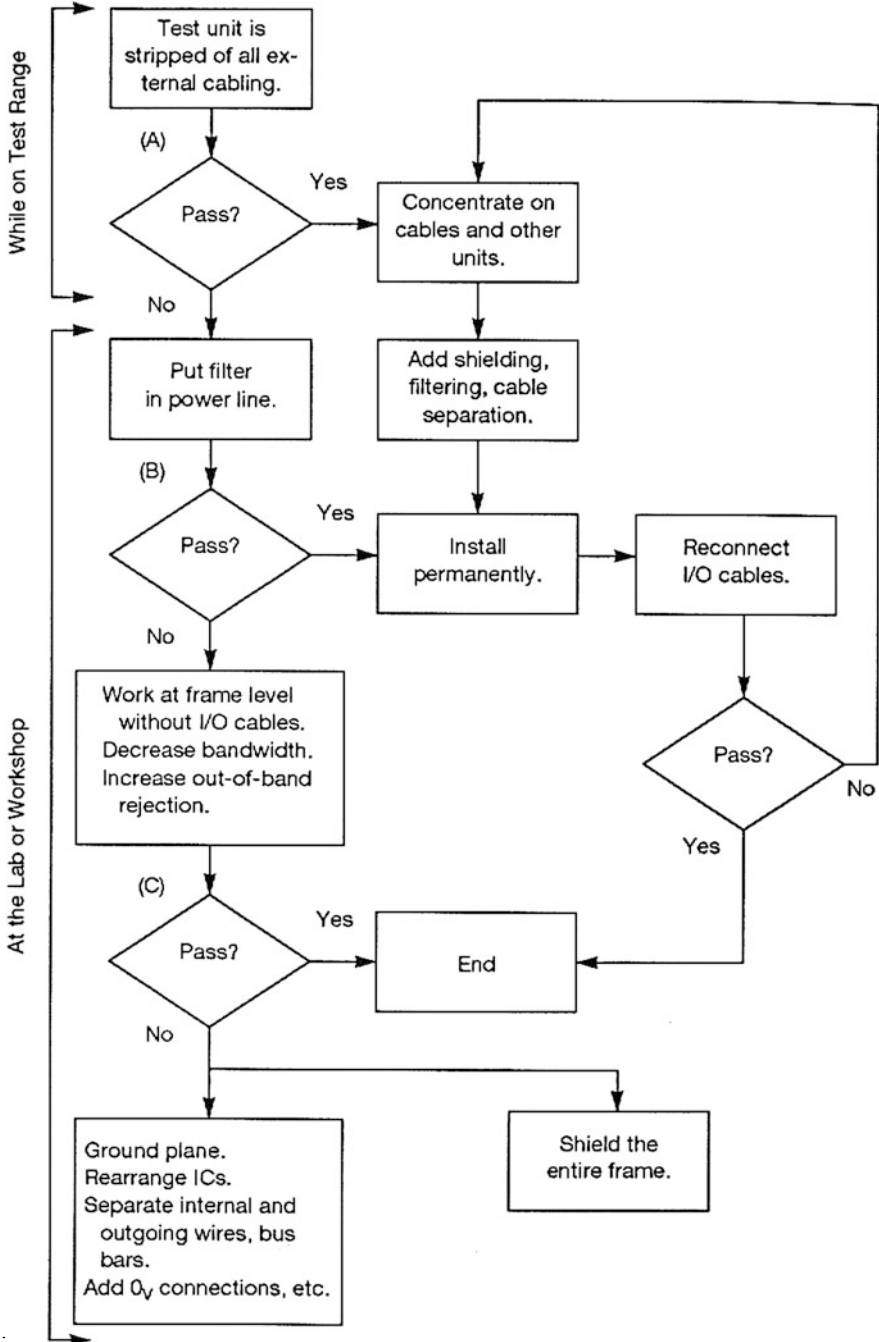


Fig. 13.1 Strategy for radiated EMI diagnostic and prototype improvements

If answer to box B is “No,” we will become involved in a more difficult task of hardening the product itself. Depending on the stage of the EUT in the development or production cycles, one can work:

1. At circuit or internal packaging level. (This is labor-intensive but may be cost-effective in the long run.)
2. At box shielding level. (This is the “brute-force” approach, using gaskets, screen meshes, and seam tightening. It is often the only option left when the calendar is the driving force.)

Figure 13.2 shows an example of an EUT violating the RE limit of MIL-STD-461. The initial test plot shows many spectral lines above the limit. When the I/O cables are removed, many of the narrowband emissions (related to a 4 MHz clock) have decreased, but a significant number are still out of spec (see Fig. 13.3).

These two plots will be our trustworthy references in the forthcoming investigations because they tell us what is contributed by the I/O cables and what is due to the box alone (plus eventually the power cord). There is no need to go back to the test range every time to check our progress. A good deal of evaluation can be done right at the workbench, using an EMC current probe and a miniature field probe. Back at the engineering lab, we will first concentrate on reducing the emissions coming through the box alone. It is important to do this first; otherwise, any future progress in cable EMI reduction could be masked by nearby box emissions. The equipment is still stripped of its I/O cables, and a set of heavy tubular ferrites is placed over the power cable, right at its box exit. Then, proceed to Step 6.

### **Step 6**

Before making any changes, the “sniffer” *H*-field probe [3, 4] is brought to 2 cm from the case.<sup>2</sup> All the faces, especially around edges, seams, and apertures, are explored. At each face, the leakage which produces the highest profile on the spectrum analyzer display is retained (see Fig. 13.4).

### **Step 7**

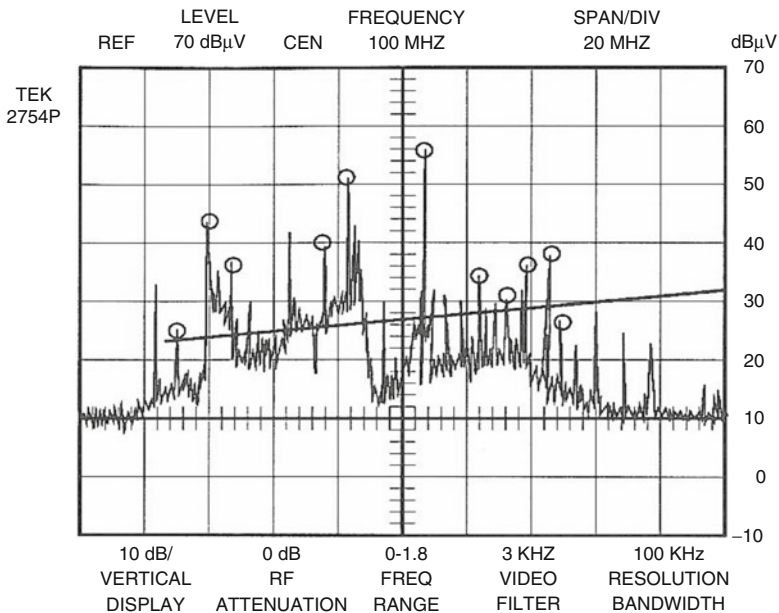
We know that these levels have no absolute meaning but can be related to the specified-distance test for each frequency that was significantly out of spec by  $\Delta$ dB. Therefore, we simply subtract the  $\Delta$ dB from the sniffer probe results. This will produce a kind of broken line which becomes our goal for reducing box emissions, as seen using the *H*-field probe. Below this line, the actual test will be in spec, too. Therefore, PC boards, flat cables, and boxes will be treated until the “sniffer” antenna reveals that we have decreased the emission level by at least the amount that the EUT failed the limit ( $\Delta$ dB). There is no uncertainty: if a close-proximity probe indicates an appropriate reduction in decibels at each of the leaky spots, this reduction will show up in at least the same range of magnitude in the final test.

In our example, after soldering surface-mount decoupling capacitors underneath the clock oscillator and clock drivers, plus adding EMI gaskets to the cover lid, the

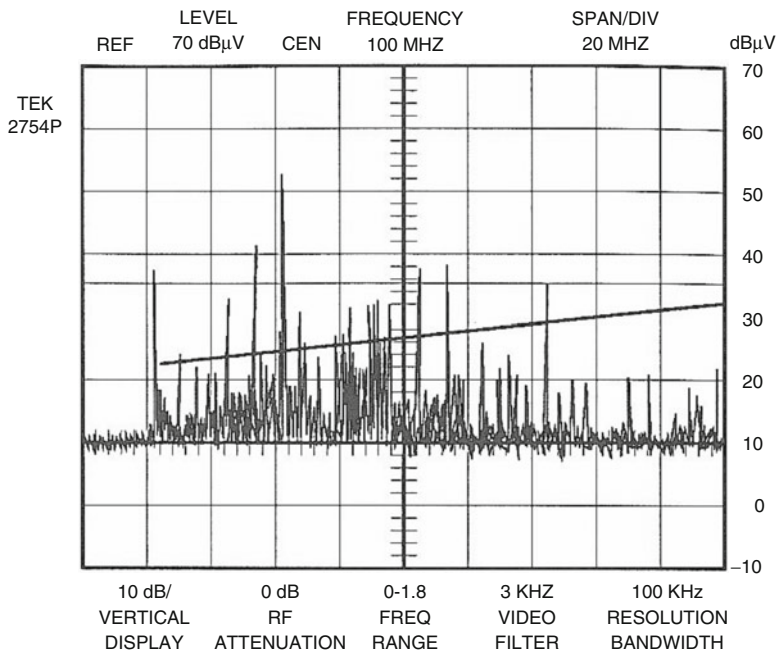
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<sup>2</sup>The absolute value of this distance is not critical. But once it is set, it must be kept rigorously constant across the whole procedure. A distance caliper made by a piece of stiff cardboard or plastic can be stuck on the probe edge to this intent.

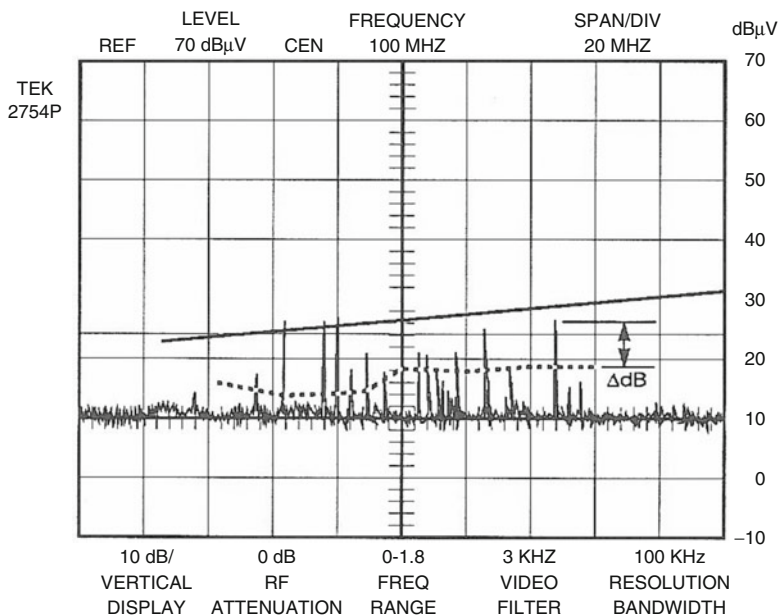
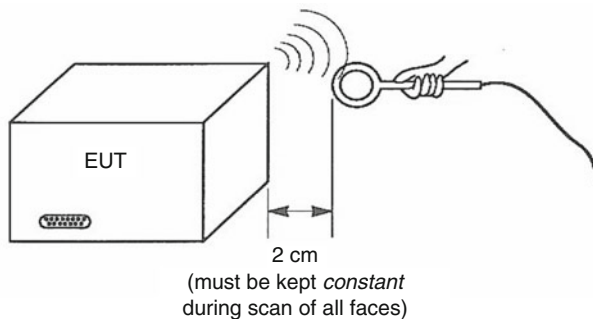




**Fig. 13.2** Actual initial test results with I/O cables in place. *Bullets* are emissions that later were traceable to the cables. Vertical scale corresponds to dB $\mu$ V/m



**Fig. 13.3** Test results of same EUT as in Fig. 13.2, with cables removed. Emissions are caused by box only. Notice that I/O cables removal has caused few box-generated emissions to increase (for instance, here, 56 and 62 MHz). This is generally because the open-ended I/O ports are loading differently the corresponding internal drivers



**Fig. 13.4** Actual readout from the sniffer probe, without cables (the *broken, dotted line* represents the objective)

probe readout was below our translated limit, even on the worst-case side of the EUT. In many cases, it is indiscernible from the noise floor.

**Step 8**

The I/O cables are put back in place and elevated < 5 cm (2 in.) above our workbench ground plane (which can be a simple sheet of aluminum foil) over their entire length or at least 1.50 m, whichever comes first. This standard height is an important detail for the reliability of the measurements, since it stabilizes the CM impedance.

We will now use the EMC current probe to control and reduce the cable contribution to total radiation. The probe readout displayed on the spectrum analyzer shows significant current levels at frequencies where radiated fields were

found (for instance, 82 and 105 MHz on Fig. 13.5). As in the case of the  $H$ -field probe, these probe readings do not represent actual  $E$ -field levels, but they are related. So, for each frequency that was significantly out of spec by  $\Delta\text{dB}$ , we simply subtract  $\Delta\text{dB}$  from the current probe spectral results. The resulting set of values will be our goal for reducing cable CM currents.

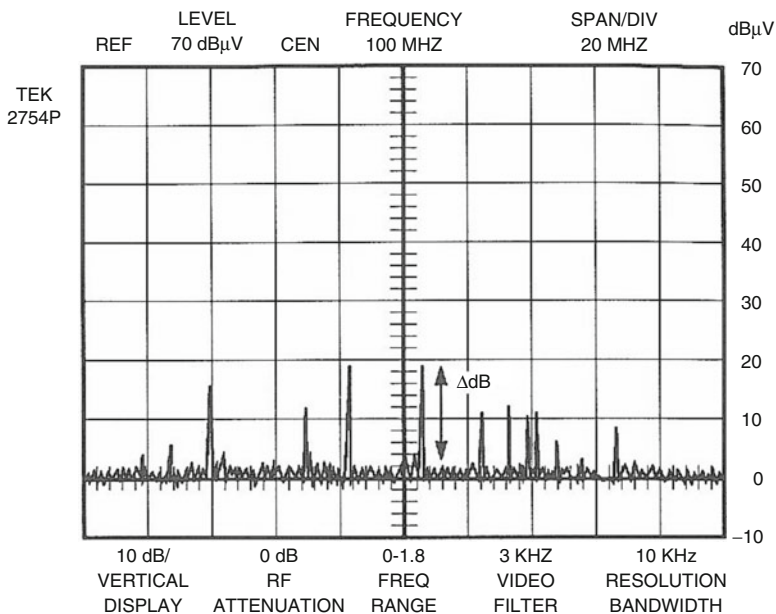
### Step 9

After installing feedthrough filters on the I/O connector pins, improving the power cord attenuation with CM ferrites, and using a shielded power cord, the current spectrum on the I/O cable is reduced by  $> \Delta\text{dB}$ .

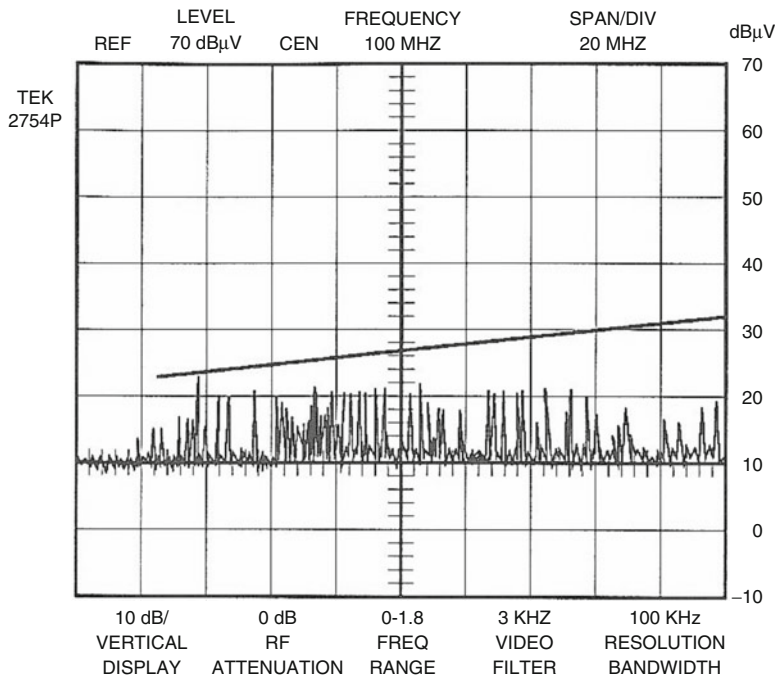
### Step 10

We now have good expectations that the product will meet the specification which is confirmed when the EUT is brought back to the shielded test room (see Fig. 13.6). Two important observations need to be remembered while doing these types of investigations:

1. Our measuring receiver or spectrum analyzer needs a sufficient reserve of dynamic range to let us see the decibel improvement. For instance, the IF bandwidth can be reduced to 10 kHz, even though it requires a slower scan rate, and a 20-30 dB low-noise preamplifier is also recommended. Beware that if the current probe reveals a BB current, a BW correction may be needed to adjust to the FCC or MIL-STD-461 bandwidth.
2. While evaluating the merit of the various fixes, we must ensure that they have not simply shifted the problem, compressing some harmonics but increasing some others.



**Fig. 13.5** Readout from the current probe on I/O cables after the box alone has been fixed. Each prominent current harmonic relates to a certain field level being  $\Delta\text{dB}$  off-specification



**Fig. 13.6** Actual test data. Field radiated by EUT with cables in place, after box and I/O cables have been treated. The unit is now within specifications

### 13.3 APPROXIMATING RADIATED RFI LEVELS FROM I/O CABLE CM CURRENTS (VHF REGION)

In Chap. 2, Equ. (2.27), we gave the far-field, free-space radiation from a cable acting as a dipole below resonance:

$$E \text{ (}\mu\text{V/m)} = 0.63 I(\mu\text{A}) \times \ell \text{ (m)} \times F(\text{MHz})/D$$

where  $D$  is the distance in meter from source to receiving antenna.

For a base-driven monopole (the equivalent model of a typical I/O cable carrying CM currents), when the cable length exceeds  $\lambda/4$  and the height above ground exceeds  $\lambda/8$ , the length  $\ell$  in the equation must be replaced by  $\lambda/4$  (the antenna is electrically “shrinking”): in Equ. (2.28),  $E$  becomes independent of  $F$  and relates only to current  $I$  and distance  $D$ . Therefore, in practical situations of FCC/CISPR 22 radiated testing, under the following test conditions:

- Frequencies above 50 MHz
- Cable length greater than 1.50 m
- Cable height greater than 0.75 m

A simple current criteria for pass/fail forecast can be set, referring to specification limit  $E_L$ :

$$I_{cm} (\mu\text{A}) \leq E_L(\mu\text{V/m}) \times D/60 \quad (13.1)$$

For FCC/CISPR, electronic data processing devices, simply measuring  $I_{cm}$  with a current probe on all I/O cables, and accounting 5 dB margin for ground reflection, if we find, on every spectral line, no more than the following values:

	50-230 MHz	230-400 MHz
<b>For Class A</b>	$I_{cm} \leq 10 \mu\text{A}$ (20 dB $\mu\text{A}$ )	$\leq 20 \mu\text{A}$ (26 dB $\mu\text{A}$ )
<b>For Class B</b>	$I_{cm} \leq 3 \mu\text{A}$ (10 dB $\mu\text{A}$ )	$\leq 6 \mu\text{A}$ (16 dB $\mu\text{A}$ )

then the equipment can be brought to the test site with a high confidence that it will pass (400 MHz is the upper practical range of validity for this method). The current probe must be moved along the 1.50 m cable section that is closer to the EUT box to make sure you do not miss a current standing wave maximum.

If, to the contrary, it is found for Class A:  $I_{cm} > 30 \mu\text{A}$  from 50 to 230 MHz, and  $> 60 \mu\text{A}$  above

Or, for Class B:  $I_{cm} > 10 \mu\text{A}$  from 216 to 230 MHz, and  $> 18 \mu\text{A}$  above

Do not waste time bringing the EUT to a test site: it is almost certain to exceed the limits. If you fail this precompliance CM current test, you will also fail the radiated emission test [4]

Between the two criteria is some latitude for trying our luck, depending on:

- How costly is the engineering effort vs. EMC test lab?
- How critical is our \$/dB optimization (e.g., the cost penalty of a slight overdesign with mass-produced equipment)?

For MIL-STD-461C-RE102, MIL-STD-461F-RE102, or DO-160G, two additional factors are coming into play:

1. Cables are laid at 5 cm above the ground plane, which reduces  $E$  by a  $10 h/\lambda$  factor (Chap. 2, Sect. 2.5).
2. The limit relaxes progressively above 20 MHz (for 461C) or 100 MHz (461E and F).

Entering these variables, and given the 1 m test distance for far-field conditions, the criterion for maximum CM current referred to spec. limit becomes

$$I_{cm} (\mu\text{A}) \leq E_L(\mu\text{V/m}) \times D \times \lambda / (60 \times 10h) \quad (13.2)$$

i.e., after replacing  $\lambda$  by  $300/F(\text{MHz})$ :  $I_{cm} \leq E_L (\mu\text{V/m})/0.1F (\text{MHz})$  or  $I_{cm} (\text{dB}\mu\text{A}) \leq E_L (\text{dB}\mu\text{V/m}) + [20 - 20 \log F]$



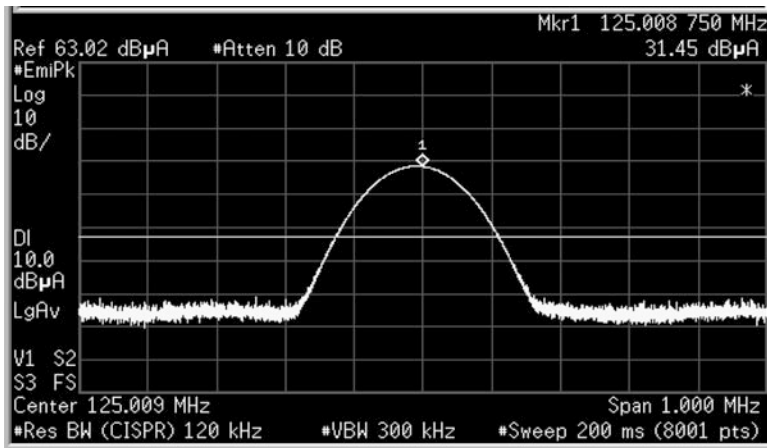
**Fig. 13.7** Example of EMI investigation routine on a computer, installed for radiated emission testing (*top*). After failing the Class B limit, the CM current is checked on the CPU data cable. As a variation of the routine steps, the unit is tightly wrapped in aluminum foil, in order to prevent box leakages from obscuring our diagnosis (photos courtesy of Don Sweeney, D.L.S. Electronic Systems Inc.)

Designating by  $K$  the correction term between brackets, this translates into the following table:

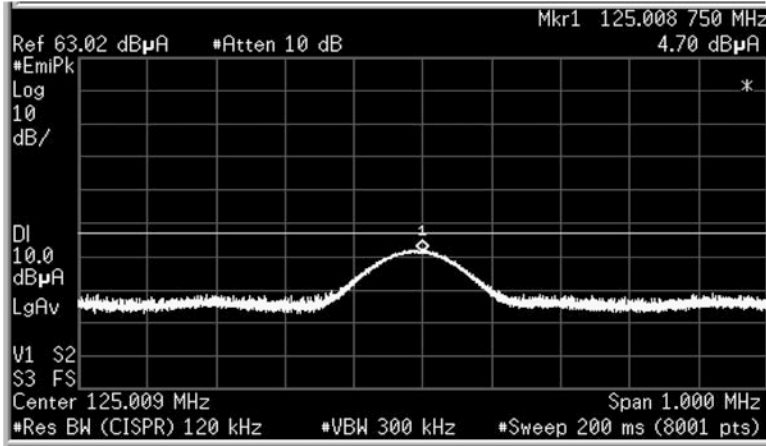
$F(\text{MHz})$	50	75	100	200	300
$K(\text{dB})$	-14	-17	-20	-26	-30
<b>MIL-STD-461C-RE02</b>					
$E_L(\text{dB}\mu\text{V/m})$	25	28	30	34	37
$I_{\text{cm}}(\text{dB}\mu\text{A}) = E - K$	<b>11</b>	<b>11</b>	<b>10</b>	<b>8</b>	<b>7</b>
<b>MIL-STD-461F-RE102</b>					
$E_L(\text{dB}\mu\text{V/m})$	24	24	24	30	34
$I_{\text{cm}}(\text{dB}\mu\text{A}) = E - K$	<b>10</b>	<b>7</b>	<b>4</b>	<b>4</b>	<b>4</b>

For <b>DO-160G</b> category H	108 MHz	320 MHz
For the limits, two most severe notches $E_L(\text{dB}\mu\text{V/m})$	25	38
The corresponding CM current is $I_{\text{cm}}(\text{dB}\mu\text{A}) = E - K$	<b>5</b>	<b>8</b>

We see that, up to <75 MHz and regarding cable radiation only, the criteria for the most severe *MIL-STD-461* limit are quite close to what would be required for FCC 15 and CISPR 22 Class B.



**Fig. 13.8** Here, at one specific frequency where limit is violated, the CM current is exceeding our 10 dBμA Class B criteria by ≈21 dB.



**Fig. 13.9** Following on the procedure, additional CM filtering is installed on the I/O connector. The CM current has been reduced by <20 dB. The radiated check confirms the product is now within limits (photos courtesy of Don Sweeney, D.L.S. Electronic Systems Inc.)

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# Appendix A: The Modified Dipole Model

The practical radiation formulas presented in Chap. 2 and applied from that point onward have been established via the process described in this appendix.

When the source is at a distance  $D < \lambda/2\pi$  (near-field conditions), the  $E/H$  ratio of an electromagnetic field departs from the free-space impedance  $Z_0$ , which is:

$$Z_0 = \sqrt{\mu_0/\epsilon_0}$$

where  $\mu_0 = 4\pi \times 10^{-7}$  Henry/m,  $\epsilon_0 = 1 \times 10^{-9}/36\pi$  F/m

Thus,  $Z_0 = 120\pi$ , or  $377 \Omega$

The near-field  $E/H$  ratio depends on the source impedance but can never exceed  $377 (\lambda/2\pi D)$  nor be less than  $377 (2\pi D/\lambda)$ . The question of how source circuit and the wave impedance are related in the near field is important because the estimation of  $E$  and  $H$  and the shielding effectiveness of barriers are dependent on this relation. The development of a discrete relation between circuit impedance,  $Z_c$ , and wave impedance,  $Z_w$ , in the near field is beyond the scope of this book. However, using the ratio of the source frequency,  $F_x$ , to the near-/far-field transition frequency,  $F_{N-F}$ , mathematical relations are suggested that take into account the impact of actual circuit impedance  $Z_c$  on the wave impedance  $Z_w$  for all conditions in which the radiating circuit dimensions,  $\ell, s \ll \lambda$ . These relations are more realistic with circuits that are neither perfect loops or open dipoles.

**For  $Z_c > Z_0$  (high- $Z$  source):**

$$\begin{aligned} &\text{for } \geq Z_0\lambda/2\pi D > 377, Z_w = Z_0\lambda/2\pi D \\ &\text{for } Z_0\lambda/2\pi D > Z_c > 377, Z_w \approx Z_c \\ &\text{for } Z_c = Z_0, Z_w = Z_0, \text{ at any frequency} \end{aligned}$$

**For  $Z_c < Z_0$  (low- $Z$  source):**

$$\begin{aligned} &\text{for } Z_0 > Z_c > Z_0 2\pi D/\lambda, Z_w = Z_c \\ &\text{for } Z_0 > 7.9 \times F(\text{MHz}) \cdot D > Z_c, Z_w = 7.9 \times F(\text{MHz}) \cdot D \end{aligned}$$

These equations are plotted in Fig. A.2 for several values of common circuit impedances of 50, 100, 300, and 600  $\Omega$ . To the extent that these conditions exist, the finite source circuit impedance, then, does not permit an infinitely high- or null-wave impedance  $E/H$ . Rewriting the former equations in more practical terms, the near-field wave impedance for *any* circuit is

For  $Z_c > 18 \times 10^3/D \cdot F(\text{MHz})$ ,  $Z_w(\Omega) = 18 \times 10^3/D \cdot F$

For  $18 \times 10^3/D \cdot F(\text{MHz}) > Z_c > 7.9 D \times F$ ,  $Z_w(\Omega) = Z_c$

For  $7.9 D \times F \geq Z_c$ ,  $Z_w(\Omega) = 7.9 D \times F$

### Far-Field Value

The  $E$  field radiated by an *isolated wire* carrying a current  $I(\text{A})$  at a distance  $D > \lambda/2\pi$  is

$$E(\text{V/m}) = 60\pi I (\ell/\lambda)/D$$

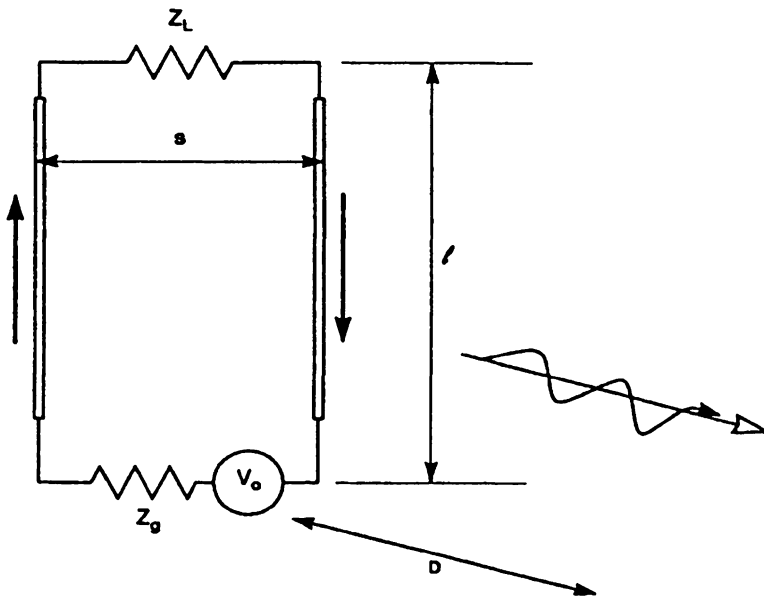


Fig. A.1 The two-dipole model

If, instead, we have two wires carrying equal but opposite currents (Fig. A.1), the radiated field in the plane of the two wires is calculated from the phase lag of the equal and opposite fields:

$$E(\text{V/m}) = 60\pi I (\ell/\lambda) (\sin 2\pi s/\lambda)/D$$

Recognizing that, for small values of “ $x$ ,”  $\sin x \approx x$ , replacing  $\lambda$  by  $300/F(\text{MHz})$  and expressing  $\ell \times s$  in  $\text{cm}^2$

$$E \text{ (}\mu\text{Vm)} = 1.3 \times V (\ell \times s)F^2/(D \times Z_L)$$

$V$  being the drive voltage in volts,  $Z_L$  the load impedance, and  $\ell, s$  the dimension in cm, this is the same expression as the loop model in far-field conditions.

### ***Case of Two Wires, Loaded by $Z_L > 377 \Omega$***

In Sect. 2.3 and Fig. 2.6, we stated that when  $Z_L$  exceeds  $377 \Omega$  the radiated field no longer depends on the terminal load impedance. Using a different approach, Chatterton and Houlden [1] reach a similar conclusion, with a formula for the  $E$  field from any loop, with loads from few ohms to  $\infty$ , for  $\ell, s, D, \lambda$  in meters:

$$E_{V/m} = \frac{\pi \cdot l \cdot s}{D \cdot \lambda^2} V \left[ \sqrt{1 + (Z_0/Z)^2} \right]$$

The bracket term allows an easy entry for math modeling. Replacing  $Z_0$  by  $377 \Omega$  and converting into more practical units give a practical value of  $E$  in far field, for any load impedance:

$$E \text{ (}\mu\text{V/m)} = 0.35 \times 10^{-2} \times V(V)\ell s(\text{cm}^2) F(\text{MHz}) \left[ \sqrt{1 + (Z_0/Z_L)^2} \right] / D(\text{m})$$

If  $Z_L \gg 377 \Omega$ , the field value no longer depends on the load current, but only on the voltage, as shown in curves of Fig. 2.6a, b. Numerous experiments have validated this model, confirming that when a loop is terminated by anything greater than  $\approx 400 \Omega$ , it behaves as an open, folded dipole.

### ***Values at Transition Distance***

Replacing  $F$  by its corresponding value at the near-far transition distance, i.e.,  $F_{N-F}(\text{MHz}) = 300/2\pi D$ , or  $48/D(\text{m})$ :

$$\begin{aligned} E_{\mu\text{V/m}} &= \frac{1.3}{D} \times \frac{V}{Z_L} \times \ell \times s \left( \frac{48}{D} \right)^2 \\ &= \frac{V \times (\ell \times s) \text{ cm}^2}{Z_L} \times \frac{3,000}{D^3} \end{aligned}$$

This new formula is used as the reference value to calculate the near-field terms, since the near-field wave impedance will become asymptotic to the impedance of the source circuit, increasing from  $377 \Omega$  to  $Z_c$  (if  $Z_c > 377 \Omega$ ) for high-impedance circuits or decreasing to  $Z_c$  if  $Z_c < 377 \Omega$ .

**Near-Field Values (i.e.,  $F < F_{N-F}$ )**

The transitional, previous expression of  $E$  is multiplied by:

$F/F_{N-F}$ , if  $Z_c < 377 \times (F/F_{N-F})$ , which indicates a low-impedance near field, or by  $Z_c/377$  if  $Z_c > 377 \times (F/F_{N-F})$ , which indicates a high-impedance near field

Therefore,

1. If  $Z_c < 377 \times F/F_{N-F}$  (low- $Z$  circuit), or  $Z_c < 7.9 F(\text{MHz}) \times D$ , then

$$E \text{ (}\mu\text{V/m)} = 63 \times V \text{ (}\ell \times s) \text{ cm}^2 \times F \text{ (MHz)} / (Z_c \times D^2)$$

2. If  $Z_c > 377 \times F/F_{N-F}$  (high- $Z$  circuit), or  $Z > 7.9 F \times D$ , then

$$E \text{ (}\mu\text{V/m)} = 7.9 \times V \text{ (}\ell \times s) \text{ cm}^2 / D^3$$

Distance  $D$  is in meters.

**Quasi-Static Values for  $E$  or  $H$**

In the near field, field prediction curves of Chap. 2 (Fig. 2.6) show that  $E$  becomes constant for a given drive voltage and distance. This raises the question: what happens to the associated  $H$  field? The previous equations, plus Figs. A.2 and A.3, provide the answer.

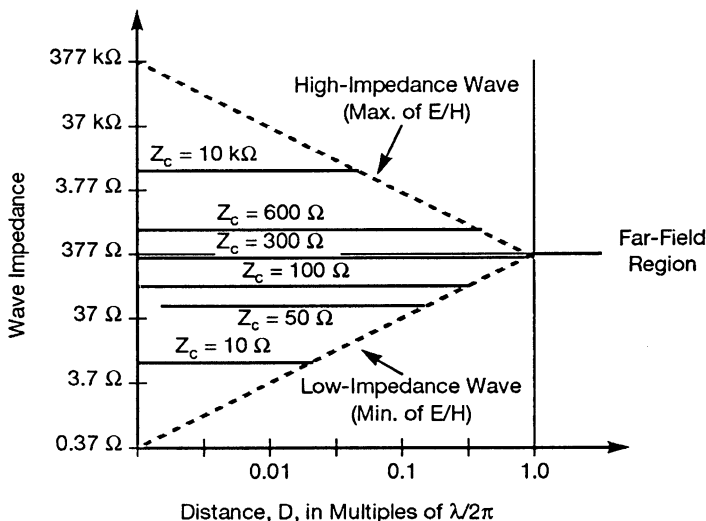


Fig. A.2 Wave impedance vs. circuit impedance

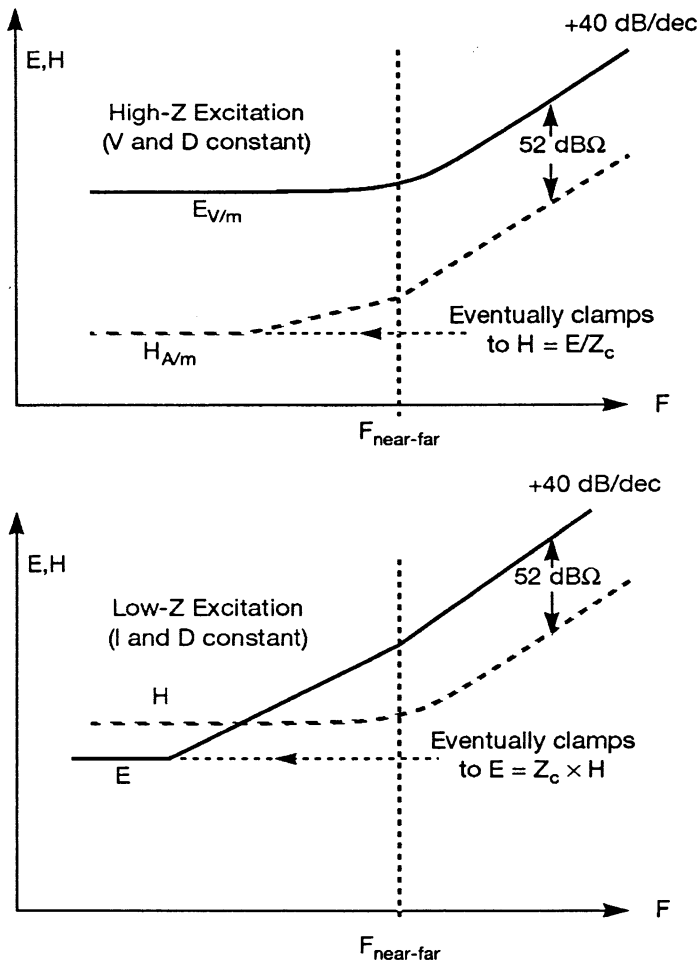


Fig. A.3 Electric and magnetic field trends at very low frequencies (quasi-static)

For a constant voltage excitation, the wave impedance increases when  $F$  decreases below  $F_{N-F}$ , until it reaches  $Z_c$  (including  $Z_c = \infty$ ). This would meet the case of a monopole, or open loop excited in DC, creating a static  $E$  field but no  $H$  field.

Conversely, for a magnetic, low- $Z$  field, the wave impedance decreases when  $F$  decreases below  $F_{N-F}$ , until it reaches  $Z_c$ . Therefore, the associated  $E$  field decreases, but not down to 0, unless  $Z_c = 0$ . This latter would meet the case of a perfectly shorted loop at DC, having no  $E$  field and a static  $H$  field.

## REFERENCE

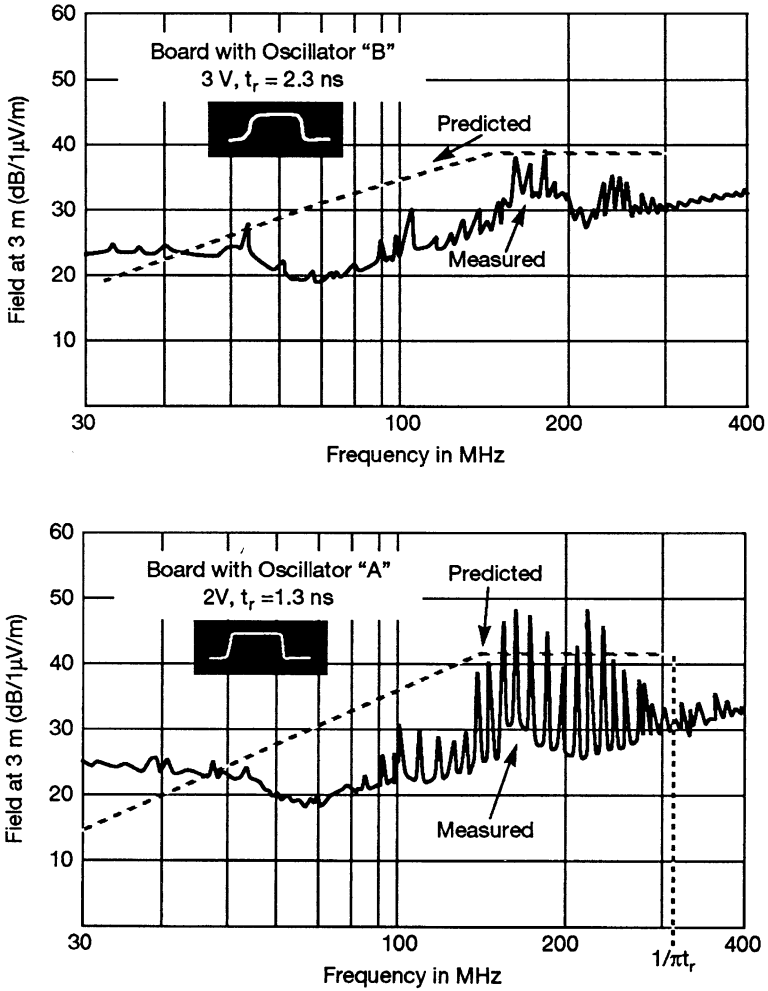
I. P. Chatterton, P. Houlden, *EMC Theory to Practical Design* (Wiley, England, 1992)

## Appendix B: Some Validation Results Supporting the Simplified Radiation Model

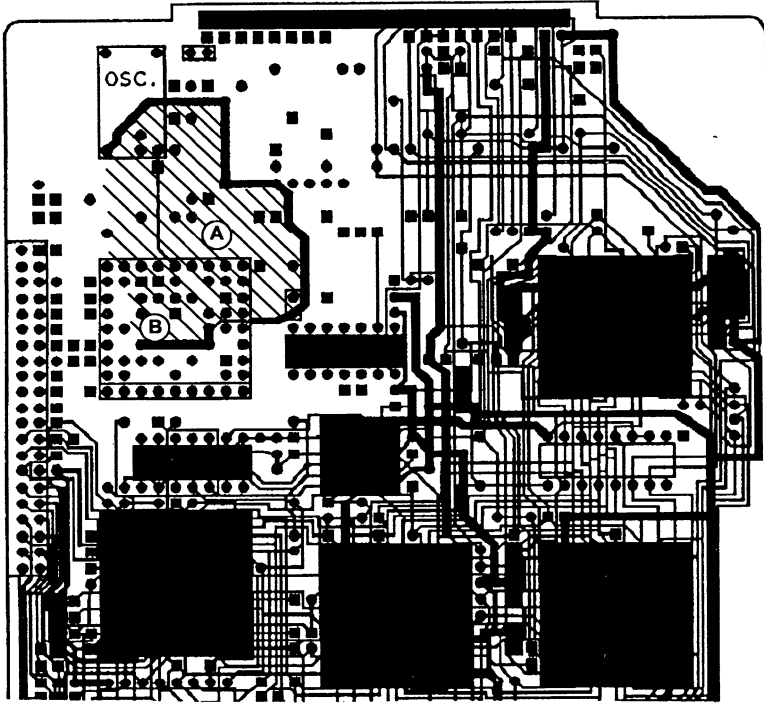
Several validation measurements performed by the author on simple circuits, as well as other measurements reported in the literature, give an indication of the error margin incurred. The compilation of about 60 radiated test results, compared to the predicted results per this book's method, showed a mean of differences of 8.5 dB.

Figures B.1 and B.2 show the results for a personal computer single-layer/double-sided board radiation and a backplane with 10-MHz clock runs, both measured on calibrated FCC test sites. Interestingly, in Fig. B.2, the influence of changing from a clock oscillator supplied by source A to one provided by source B, with slightly different rise times, is clearly visible.

Figure B.3 shows another validation result for a prototype PCB (not shielded) at 3 m distance.



**Fig. B.1** Measured vs. predicted radiated emissions from a PCB, on a 3-m test site per FCC Part 15J (from Bush, D. "Radiation from a P.C. Board oscillator," IEEE/EMC Symposium 1981)



OSC. = 7.5 MHz Clock  
A = Loop Area, 6.5 cm<sup>2</sup>  
B = Driver Module

Fig. B.2 The double-sided, single-layer PCB responsible for radiated spectrum in Fig. B.1



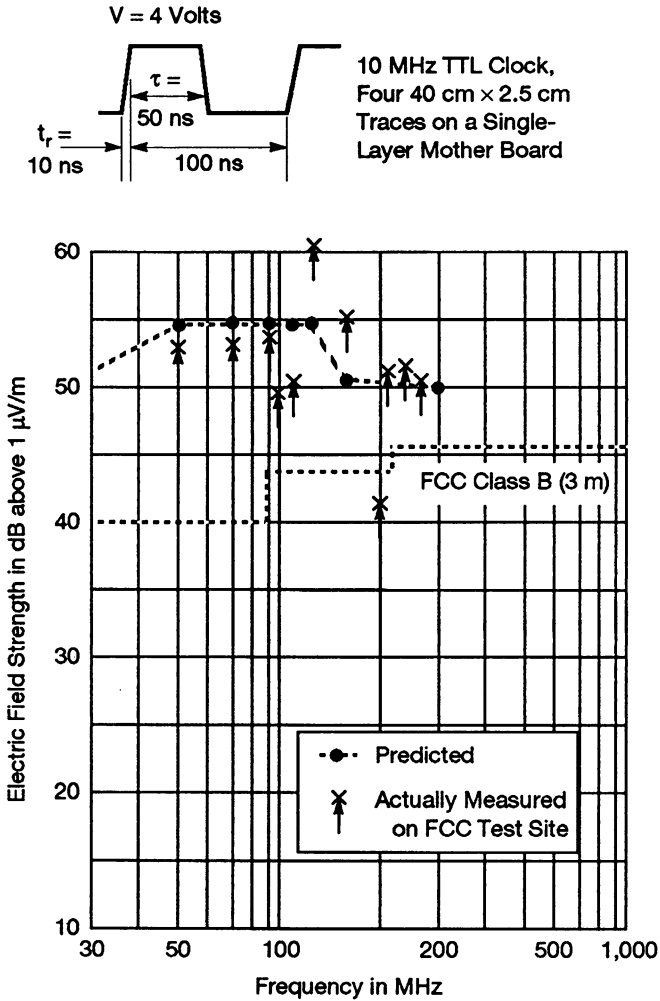


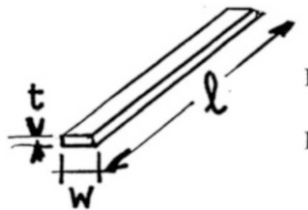
Fig. B.3 Measured vs. predicted radiated emissions from PCB traces

# Appendix C: Inductances and Capacitances of PCB Traces

The following formulas and curves, essentially derived from the remarkable work by C. Walker (Capacitance, Inductance and Crosstalk Analysis, Artech House, 1990), are useful for most calculations regarding EMI coupling in PCBs. When it was necessary for simplification, formulas have been rounded within +1-5%.

## Isolated Trace

Although a completely isolated trace is an academic configuration, the following formula gives the exact value of inductance  $L$  when the associated trace or plane is extremely far (in practice, at a distance greater than the length  $\ell$ ). Notice that in this case, strictly speaking, no linear value in nH/cm can be given since  $L$  will depend on the  $\ell/w$  ratio. The 10 nH/cm value we have been using in many calculations is a close approximation, not an exact value.



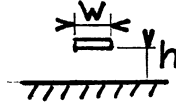
$$L(\text{nH}) = 2 \ell(\text{cm}) \left[ \log_n \left( \frac{2 \ell}{w + t} \right) + 0.5 + 0.2 \left( \frac{w + t}{\ell} \right) \right]$$

where  $\ell$ ,  $w$  and  $t$  in same units  
 $\log_n$  is the natural logarithm

Since very often  $\ell/w > 3$  and  $w/t > 3$ , formula simplifies as:

$$L(\text{nH}) = 2 \ell(\text{cm}) \left[ \log_n \left( \frac{2\ell}{w} \right) + 0.5 \right]$$

**Trace Above a Ground Plane (Microstrip),  
Epoxy Dielectric ( $\epsilon_r = 4.5$ )**

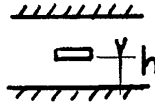


$$L_o \text{ nH/cm} = 2 \log_n \frac{(6h)}{t + 0.8w}$$

$$C_o \text{ pF/cm} = \frac{1.55}{\log_n \frac{(6h)}{t + 0.8w}}$$

$$Z_o = 38.5 \log_n \frac{(6h)}{t + 0.8w}$$

**Strip-Line, Epoxy Dielectric ( $\epsilon_r = 4.5$ )**



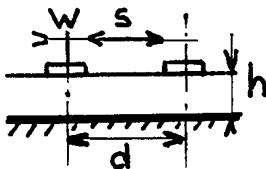
$$L_o \text{ nH/cm} = 2 \log_n \frac{(38h)}{t + 0.8w}$$

$$C_o \text{ pF/cm} = \frac{2.5}{\log_n \frac{(3.8h)}{t + 0.8w}}$$

Close approximation :  $C_o \text{ pF/cm} = 0.76 (\ell + w/h)$

$$Z_o = 28.3 \log_n \frac{(3.8h)}{t + 0.8w}$$

**Mutual Capacitance, Microstrip Traces**



Exact formula :  $C_{1-2}(\text{pF/m}) = 0.7\epsilon_r \cdot K_L K_c (w/h)^2 \log_n [1 + (2h/d)^2]$  in practice, for  $\epsilon_r = 4.5$  and length in cm:

$$C_{1-2}(\text{pF/cm}) = 0.031 K_L K_c (w/h)^2 \log_n [1 + (2h/d)^2]$$

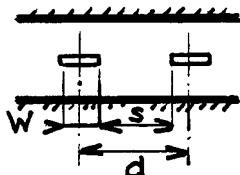
$K_L, K_c$  are the fringing terms given by complex formulas. The product  $K_L \times K_c$  has the following values:

$h/w$	0.5	1	2	3	5	8	10
$w/h$	2	1	0.5	0.3	0.2	0.12	0.1
$K_L \times K_c$	3	6.5	13	24	48	96	130

**Mutual Inductance, Microstrip Traces**

$$M_{1-2}(\text{nH/cm}) = 4 (h/d)^2$$

**Mutual Capacitance, Strip-Line Traces**



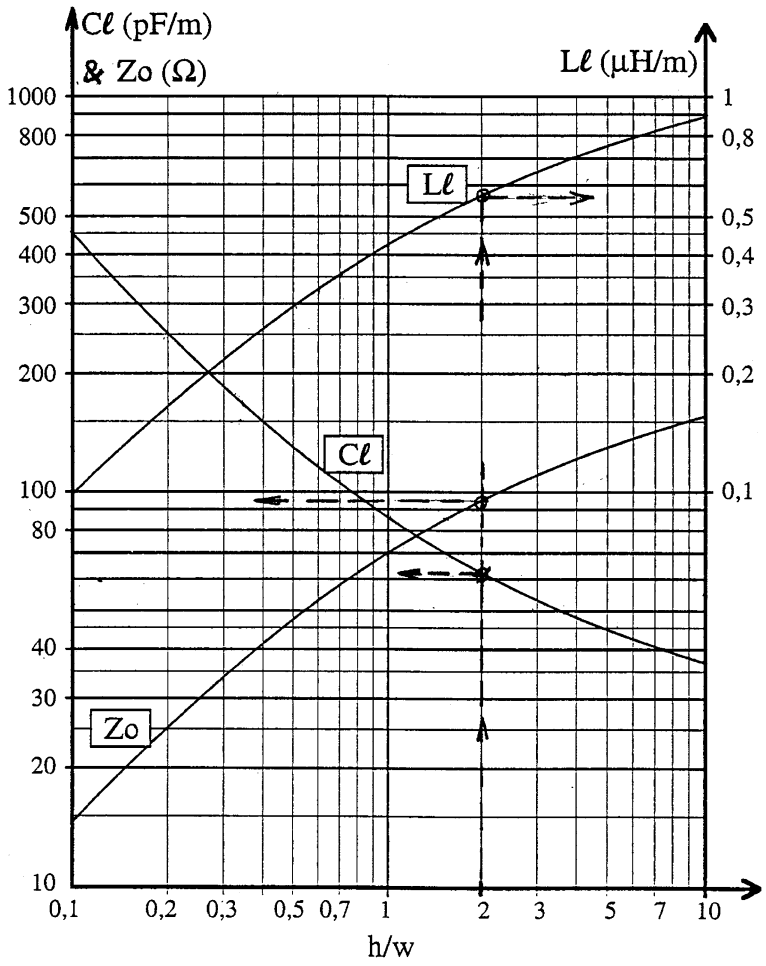
$$C_{1-2}(\text{pF/cm}) = 0.126\epsilon_r [(h + w)/d]^2$$

If “s” is used instead of “d”:

$$C_{1-2}(\text{pF/cm}) = 0.126\epsilon_r [(h + w)/(s + w)]^2$$

**Mutual Inductance, Strip-Line Traces**

$$M_{1-2}(\text{nH/cm}) = (h/d)^2$$



**Fig. C.1** Inductance ( $L$ ), capacitance ( $C$ ), and characteristic impedance for traces above ground plane. Values given for epoxy dielectric.

Example, as shown:  $w = 0.3$ ,  $h = 0.6$ ,  $h/w = 2$ .  
 $L$ (right scale) =  $0.55 \mu\text{H/m} = 5.5 \text{ nH/cm}$ ,  $C$ (left scale) =  $60 \text{ pF/m} = 0.6 \text{ pF/cm}$ ,  
 $Z_0$ (left) =  $95 \Omega$

# Appendix D: A Few Equivalent Circuits for Component Modeling via SPICE, MicroCap, or Similar Simulation Tools

## *Inductor (Wound)*

Example, typical values for a 50  $\mu\text{H}$  power line filter choke:

$$C_p = 30 \text{ pF}, R_s = 0.01 \text{ } \Omega, R_p = 10 \text{ k}\Omega$$

## *Ferrite Bead*

$L_p$ ,  $R_s$ , and  $C_p$  depend on material, number of turns, and wire insulation diameter.

Example, typical large bead, FAIR-RITE Material #43

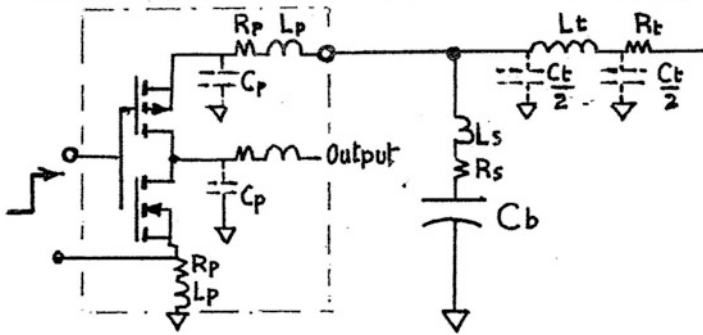
$$L = 0.3 \text{ } \mu\text{H (1 tum)} \times N^2, R_p = 300 \text{ } \Omega, C_p = 3\text{-}5 \text{ pF}$$

## *Capacitor*

Example, 10-100 nF, ceramic, bypass type:

$$R_s = 0.2 \text{ } \Omega, L_s = 6 \text{ nH (discrete), } 2 \text{ nH (SMT)}$$

### Complete Digital IC Power Supply Circuit



$L_t, R_t, C_t =$  PCB trace parameters

Typical values:

$L_t = 10 \text{ nH/cm}$  (no Gnd plane)  
 $= 5 \text{ nH/cm}$  (with Gnd plane)

$R_t = 0.01 \text{ } \Omega/\text{cm}$

$C_t = 0.5\text{-}0.8 \text{ pF/cm}$

$R_p, L_p, C_p =$  package leads, typical values:

	Surface mount	DIP
$L_p$ (nH)	2.5-5	5-15
$R_p$ ( $\Omega$ )	0.1	0.1
$C_p$ (pF)	0.5-1.2	1-3

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